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November 2013

FDN338P

P-Channel 2.5V Specified PowerTrench MOSFET

General Description

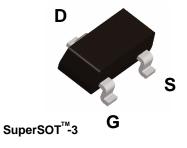
This P-Channel 2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

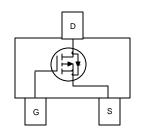
Applications

- Battery management
- Load switch
- Battery protection

Features

- -1.6 A, -20 V. $R_{DS(ON)} = 115 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 155 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$
- SuperSOTTM -3 provides low R_{DS(ON)} and 30% higher power handling capability than SOT23 in the same footprint





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-20	V
V _{GSS}	Gate-Source Voltage	±8	V
I _D	Drain Current - Continuous	-1.6	Α
	- Pulsed	-5	1
P _D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	1
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Marking and Ordering Information

9	•	9		
Device Marking	Device	Reel Size	Tape width	Quantity
338	FDN338P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			I	I	
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20			V
ΔBV _{DSS} ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		-16		mV/°C
loss	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
GSSF	Gate-Body Leakage, Forward	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
GSSR	Gate-Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.4	-0.8	-1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		2.7		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$\begin{split} &V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A} \\ &V_{GS} = -2.5 \text{ V}, I_D = -1.3 \text{ A} \\ &V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A}, T_J = 125 ^{\circ}\text{C} \end{split}$		88 117 116	115 155 165	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	- 5			Α
g FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -1.6 \text{ A}$		6		S
Dvnamic	Characteristics			I		
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		451		pF
Coss	Output Capacitance	f = 1.0 MHz		75		pF
C _{rss}	Reverse Transfer Capacitance			33		pF
Switchin	g Characteristics (Note 2)			I	I	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_D = -1 \text{ A},$		10	20	ns
t _r	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		11	20	ns
t _{d(off)}	Turn-Off Delay Time			16	29	ns
t _f	Turn-Off Fall Time			6.5	13	ns
Qq	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -1.6 \text{ A},$		4.4	6.2	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		1.1		nC
Q _{gd}	Gate-Drain Charge			0.7		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings		•	•	
ls	Maximum Continuous Drain–Source				-0.42	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -0.42 \text{(Note 2)}$		-0.7	-1.2	V

Notes:

^{1.} $R_{\theta,UA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta,UC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.

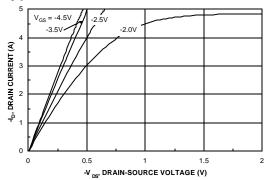


b) 270°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%

Typical Characteristics



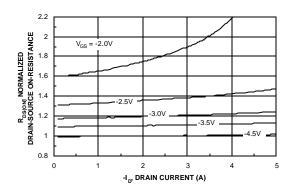
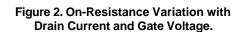
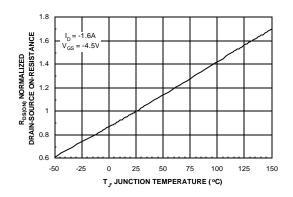


Figure 1. On-Region Characteristics.





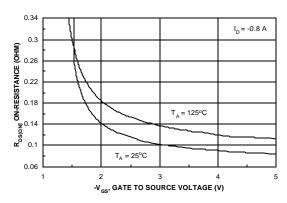
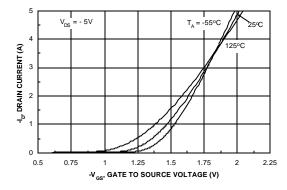


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



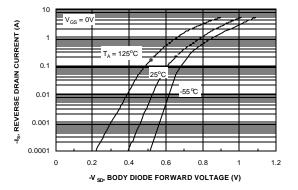
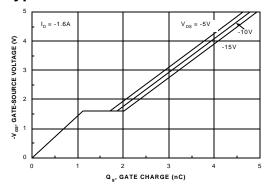


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



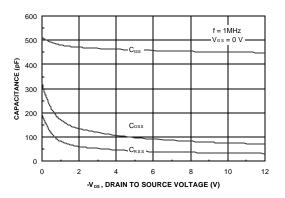
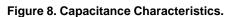
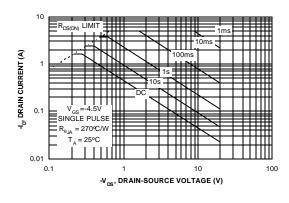


Figure 7. Gate Charge Characteristics.





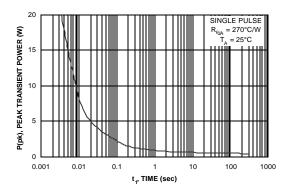


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

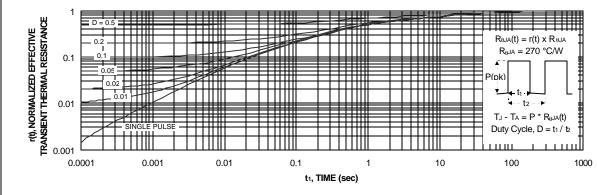


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.





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