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# MC14555B, MC14556B

## Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary−to−hexadecimal (1−of−16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

### Features
- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

**PIN ASSIGNMENTS**



| MC14555B | | | | MC14556B | | |
|---|---|---|---|---|---|---|
| $\overline{E}_A$ [ 1 • | 16 ] $V_{DD}$ | | | $\overline{E}_A$ [ 1 • | 16 ] $V_{DD}$ | |
| $A_A$ [ 2 | 15 ] $\overline{E}_B$ | | | $A_A$ [ 2 | 15 ] $\overline{E}_B$ | |
| $B_A$ [ 3 | 14 ] $A_B$ | | | $B_A$ [ 3 | 14 ] $A_B$ | |
| $Q0_A$ [ 4 | 13 ] $B_B$ | | | $\overline{Q0}_A$ [ 4 | 13 ] $B_B$ | |
| $Q1_A$ [ 5 | 12 ] $Q0_B$ | | | $\overline{Q1}_A$ [ 5 | 12 ] $\overline{Q0}_B$ | |
| $Q2_A$ [ 6 | 11 ] $Q1_B$ | | | $\overline{Q2}_A$ [ 6 | 11 ] $\overline{Q1}_B$ | |
| $Q3_A$ [ 7 | 10 ] $Q2_B$ | | | $\overline{Q3}_A$ [ 7 | 10 ] $\overline{Q2}_B$ | |
| $V_{SS}$ [ 8 | 9 ] $Q3_B$ | | | $V_{SS}$ [ 8 | 9 ] $\overline{Q3}_B$ | |

**MARKING DIAGRAMS**



SOIC−16
```
1455xBG
AWLYWW
```

SOEIAJ−16
```
MC1455xB
ALYWG
```

| x | = 5 or 6 |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G | = Pb−Free Package |

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage Range | $V_{DD}$ | −0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | $V_{in}$, $V_{out}$ | −0.5 to $V_{DD}$ + 0.5 | V |
| Input or Output Current (DC or Transient) per Pin | $I_{in}$, $I_{out}$ | ±10 | mA |
| Power Dissipation, per Package (Note 1) | $P_D$ | 500 | mW |
| Ambient Temperature Range | $T_A$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Lead Temperature (8−Second Soldering) | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.
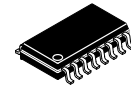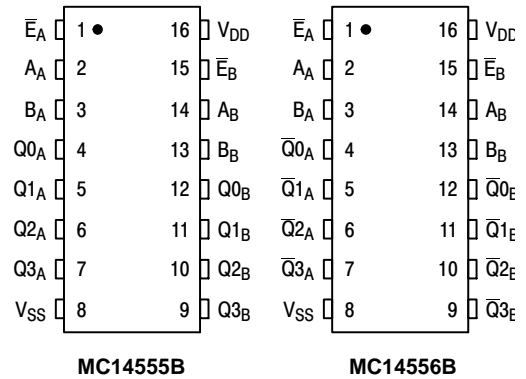
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC14555B, MC14556B

## TRUTH TABLE

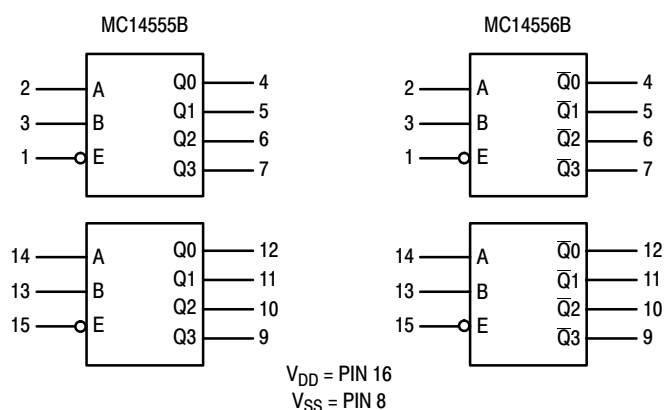| Inputs | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Enable | Select | | MC14555B | | | | MC14556B | | | |
| $\overline{E}$ | B | A | Q3 | Q2 | Q1 | Q0 | $\overline{Q3}$ | $\overline{Q2}$ | $\overline{Q1}$ | $\overline{Q0}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

X = Don't Care

## BLOCK DIAGRAM



$V_{DD}$ = PIN 16
$V_{SS}$ = PIN 8

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$)

| Characteristic | | Symbol | $V_{DD}$ Vdc | − 55°C Min | − 55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level $V_{in}$ = $V_{DD}$ or 0 | | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| "1" Level $V_{in}$ = 0 or $V_{DD}$ | | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| | | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage "0" Level ($V_O$ = 4.5 or 0.5 Vdc) ($V_O$ = 9.0 or 1.0 Vdc) ($V_O$ = 13.5 or 1.5 Vdc) | | $V_{IL}$ | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| | | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| | | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| "1" Level ($V_O$ = 0.5 or 4.5 Vdc) ($V_O$ = 1.0 or 9.0 Vdc) ($V_O$ = 1.5 or 13.5 Vdc) | | $V_{IH}$ | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| | | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| | | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current ($V_{OH}$ = 2.5 Vdc) Source ($V_{OH}$ = 4.6 Vdc) ($V_{OH}$ = 9.5 Vdc) ($V_{OH}$ = 13.5 Vdc) | | $I_{OH}$ | 5.0 | −3.0 | – | −2.4 | −4.2 | – | −1.7 | – | mAdc |
| | | | 5.0 | −0.64 | – | −0.51 | −0.88 | – | −0.36 | – | |
| | | | 10 | −1.6 | – | −1.3 | −2.25 | – | −0.9 | – | |
| | | | 15 | −4.2 | – | −3.4 | −8.8 | – | −2.4 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink ($V_{OL}$ = 0.5 Vdc) ($V_{OL}$ = 1.5 Vdc) | | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| | | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| | | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance, ($V_{in}$ = 0) | | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | | $I_{DD}$ | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | μAdc |
| | | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | |
| | | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | |
| Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | | $I_T$ | 5.0 | $I_T$ = (0.85 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| | | | 10 | $I_T$ = (1.70 μA/kHz) f + $I_{DD}$ | | | | | | | |
| | | | 15 | $I_T$ = (2.60 μA/kHz) f + $I_{DD}$ | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF: $I_T(C_L)$ = $I_T$(50 pF) + ($C_L$ − 50) Vfk where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time<br>$t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns<br>$t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns<br>$t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | $t_{TLH}$, $t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 100<br>50<br>40 | 200<br>100<br>80 | ns |
| Propagation Delay Time – A, B to Output<br>$t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 135 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 62 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 45 ns | $t_{PLH}$, $t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 220<br>95<br>70 | 440<br>190<br>140 | ns |
| Propagation Delay Time – E to Output<br>$t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 115 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 52 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 40 ns | $t_{PLH}$, $t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 200<br>85<br>65 | 400<br>170<br>130 | ns |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



All 8 outputs connect to respective $C_L$ loads.
f in respect to a system clock.
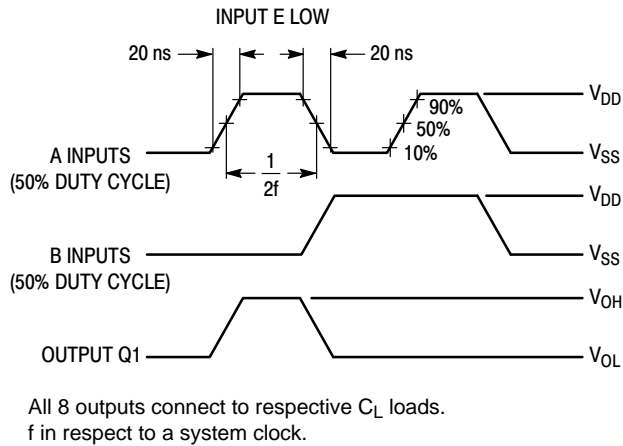
**Figure 1. Dynamic Power Dissipation Signal Waveforms**
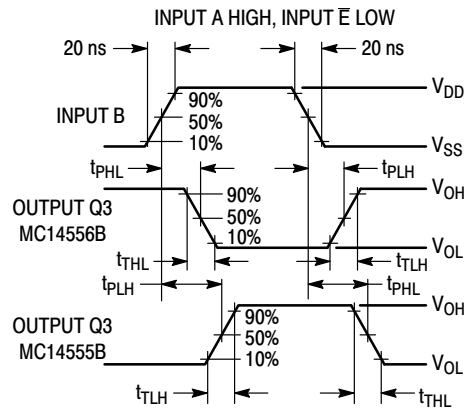


**Figure 2. Dynamic Signal Waveforms**

**LOGIC DIAGRAM**
(1/2 of Dual)
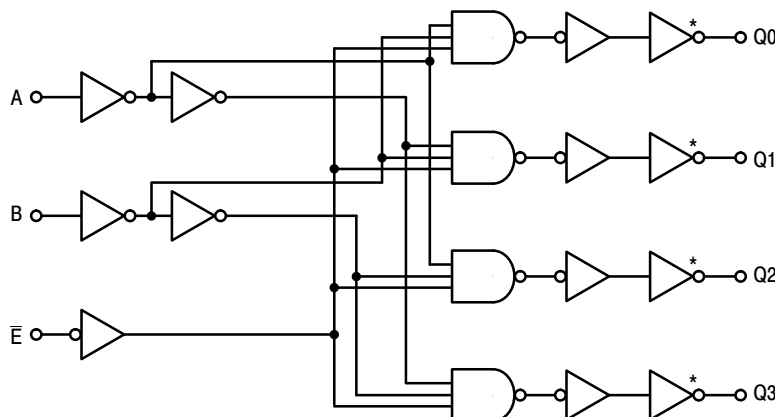


*Eliminated for MC14555B

**ORDERING INFORMATION**

| Device | Package | Shipping[†] |
|---|---|---|
| MC14555BDG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC14555BDR2G | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |
| NLV14555BDR2G* | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |
| MC14555BFELG | SOEIAJ−16<br>(Pb−Free) | 2000 / Tape & Reel |
| MC14556BDR2G | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |
| NLV14556BDR2G* | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

## PACKAGE DIMENSIONS

**SOIC–16**
CASE 751B–05
ISSUE K
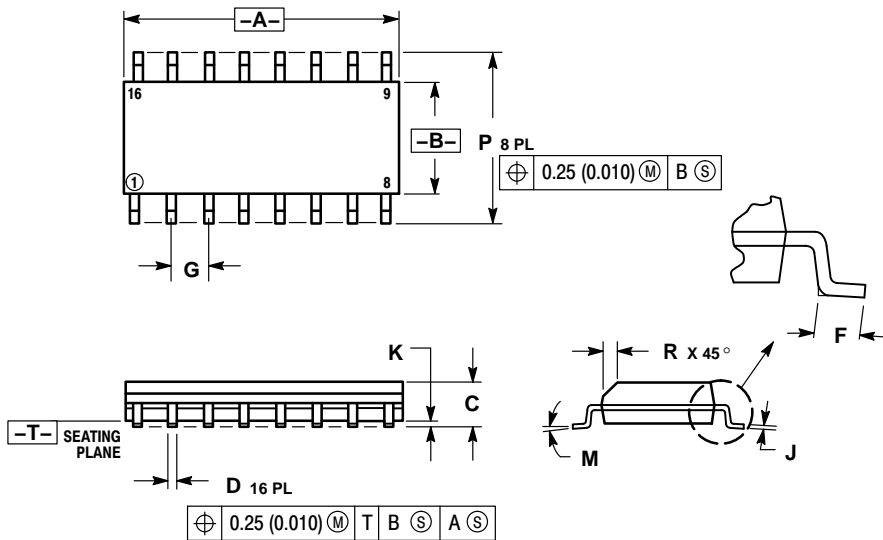
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ 0.25 (0.010) Ⓜ B Ⓢ

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## SOLDERING FOOTPRINT

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH
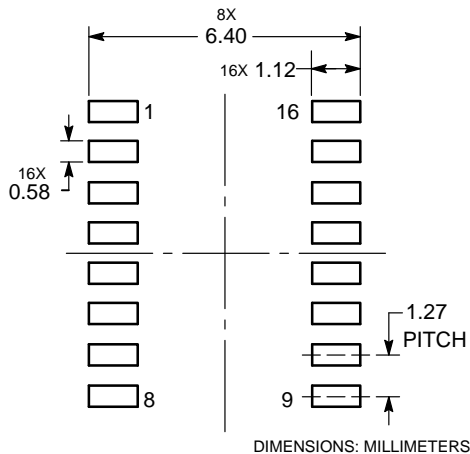
DIMENSIONS: MILLIMETERS

## PACKAGE DIMENSIONS

**SOEIAJ−16**
CASE 966
ISSUE A
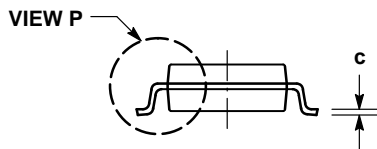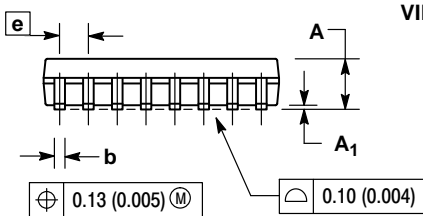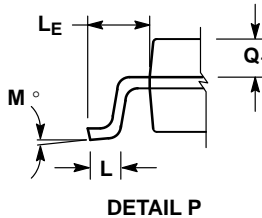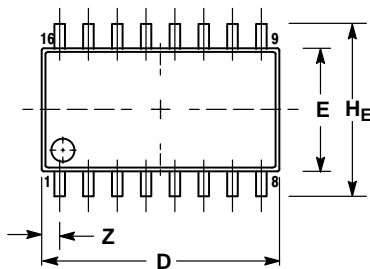
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |