MC1496, MC1496B

Balanced Modulators/ Demodulators

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See ON Semiconductor Application Note AN531 for additional design information.

Features

- Excellent Carrier Suppression −65 dB typ @ 0.5 MHz
  −50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection −85 dB Typical
- This Device Contains 8 Active Transistors
- Pb−Free Package is Available*

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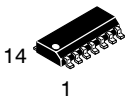
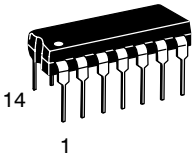
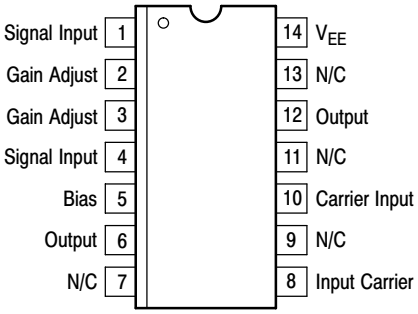


SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

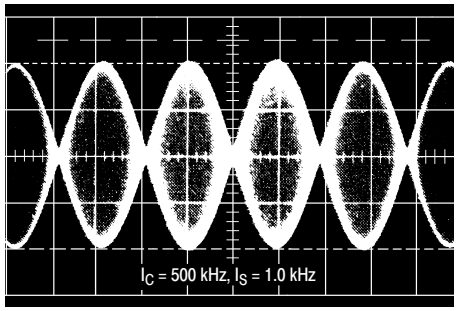


Figure 1. Suppressed Carrier Output Waveform

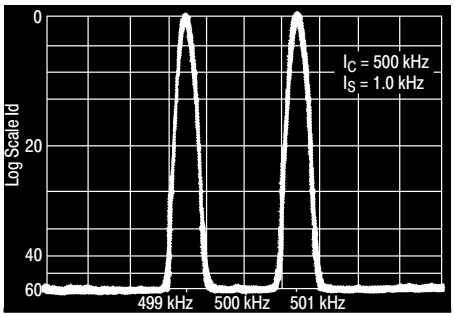


Figure 2. Suppressed Carrier Spectrum

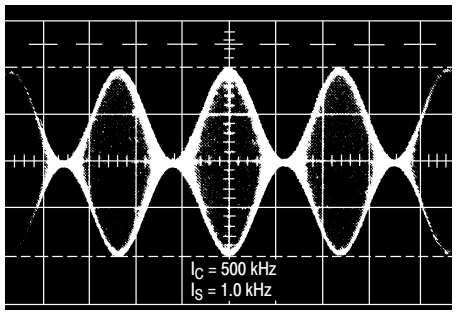


Figure 3. Amplitude Modulation Output Waveform

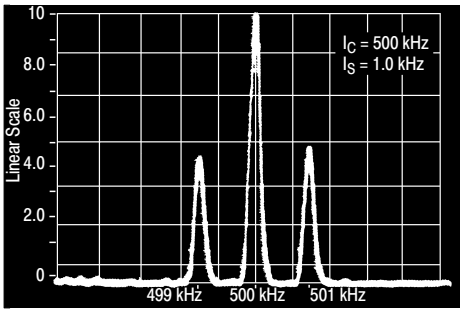


Figure 4. Amplitude−Modulation Spectrum

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6−V8, V10−V1, V12−V8, V12−V10, V8−V4, V8−V1, V10−V4, V6−V10, V2−V5, V3−V5)	ΔV	30	Vdc
Differential Input Signal	V8 − V10 V4 − V1	+5.0 ±(5 + I5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction−to−Air Plastic Dual In−Line Package	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range MC1496 MC1496B	T_A	0 to +70 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM)	ESD	 2000 400	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = −8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = T_{low} to T_{high}, all input and output characteristics are single−ended, unless otherwise noted.) (Note 1)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough	5	1	V_{CFT}				μVrms
V_C = 60 mVrms sine wave and f_C = 1.0 kHz				–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	
V_C = 300 mVpp square wave:							mVrms
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	200	
Carrier Suppression	5	2	V_{CS}				dB
f_S = 10 kHz, 300 mVrms							
f_C = 500 kHz, 60 mVrms sine wave				40	65	–	
f_C = 10 MHz, 60 mVrms sine wave				–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω)	8	8	BW_{3dB}				MHz
Carrier Input Port, V_C = 60 mVrms sine wave				–	300	–	
f_S = 1.0 kHz, 300 mVrms sine wave							
Signal Input Port, V_S = 300 mVrms sine wave				–	80	–	
$\|V_C\|$ = 0.5 Vdc							
Signal Gain (V_S = 100 mVrms, f = 1.0 kHz; $\|V_C\|$= 0.5 Vdc)	10	3	A_{VS}	2.5	3.5	–	V/V
Single−Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–					
Parallel Input Resistance			r_{ip}	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	pF
Single−Ended Output Impedance, f = 10 MHz	6	–					
Parallel Output Resistance			r_{op}	–	40	–	kΩ
Parallel Output Capacitance			c_{oo}	–	5.0	–	pF
Input Bias Current	7	–					μA
$I_{bS} = \frac{I1 + I4}{2}$; $I_{bC} = \frac{I8 + I10}{2}$			I_{bS} I_{bC}	– –	12 12	30 30	
Input Offset Current	7	–	$\|I_{ioS}\|$	–	0.7	7.0	μA
I_{ioS} = I1−I4; I_{ioC} = I8−I10			$I_{ioC}\|$	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	7	–	$\|TC_{Iio}\|$	–	2.0	–	nA/°C
Output Offset Current (I6−I9)	7	–	$\|I_{oo}\|$	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	7	–	$\|TC_{Ioo}\|$	–	90	–	nA/°C
Common−Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	Vpp
Common−Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$= 0.5 Vdc	9	–	ACM	–	−85	–	dB
Common−Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_{out}	–	8.0	–	Vpp
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	Vpp
Power Supply Current I6 +I12	7	6	I_{CC}	–	2.0	4.0	mAdc
I14			I_{EE}	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	mW

1. T_{low} = 0°C for MC1496 T_{high} = +70°C for MC1496
= −40°C for MC1496B = +125°C for MC1496B

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal−input transistor pair − or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input−signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single−ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I5(\text{mA})}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors “on” and two transistors “off” (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_S \leq I5\ R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common−mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage−current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, P_D = 2 I5 (V6 − V14) + I5)V5 − V14 where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$I5 = I6 = I12,$$
$$I_B << I_C \text{ for all transistors}$$

then :

$$R5 = \frac{V - - \phi}{I5} - 500\ \Omega$$

where: R5 is the resistor between Pin 5 and ground
ϕ = 0.75 at T_A = +25°C

The MC1496 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common−Mode Quiescent Output Voltage

$$V6 = V12 = V+ - I5\ R_L$$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector−base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V6, V12) - (V8, V10)] \geq 2\text{ Vdc}$$
$$30\text{ Vdc} \geq [(V8, V10) - (V1, V4)] \geq 2.7\text{ Vdc}$$
$$30\text{ Vdc} \geq [(V1, V4) - (V5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V6 = V12,\ V8 = V10,\ V1 = V4$$

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \Bigg| V_o = 0$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \Bigg| V_c = 0.5 \text{ Vdc}, V_o = 0$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

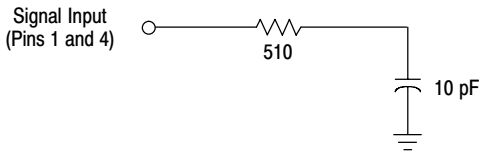
The output signal is taken from Pins 6 and 12 either balanced or single−ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single−ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source−tuned circuits that cause the oscillation.



An alternate method for low−frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

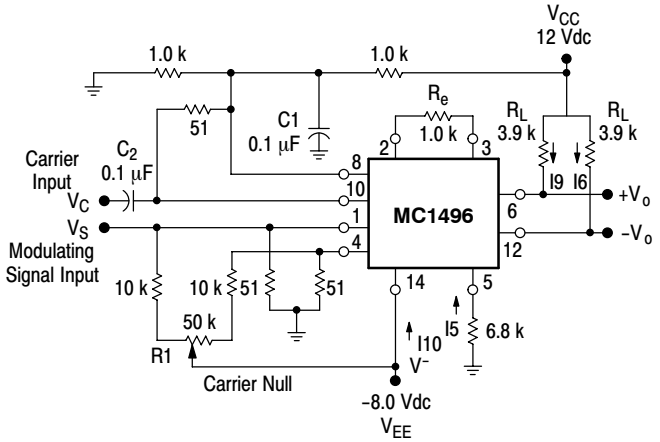
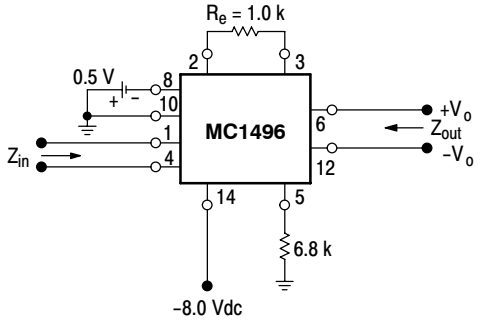


Figure 5. Carrier Rejection and Suppression



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

Figure 6. Input−Output Impedance

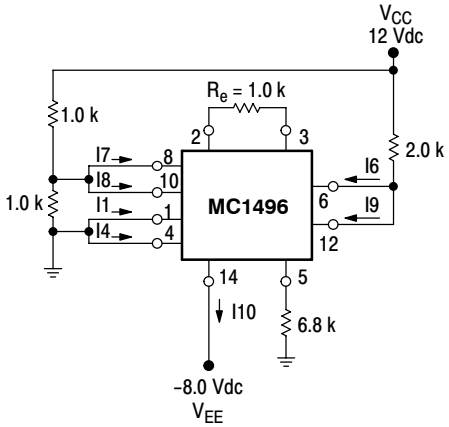


Figure 7. Bias and Offset Currents

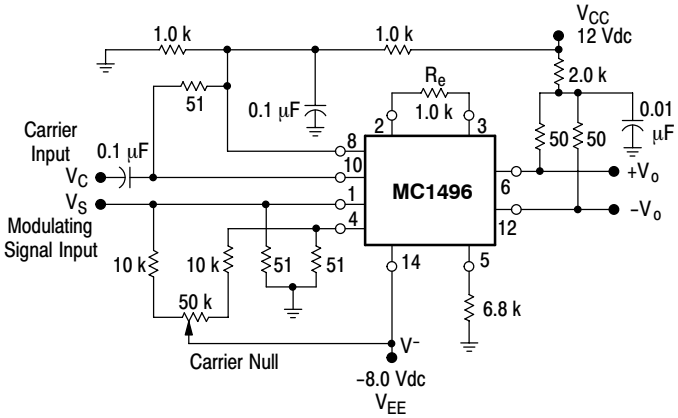


Figure 8. Transconductance Bandwidth

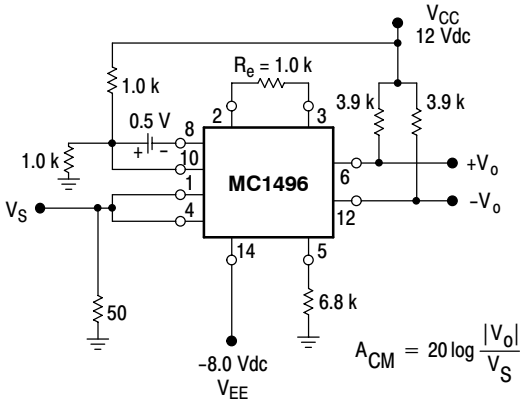


Figure 9. Common Mode Gain

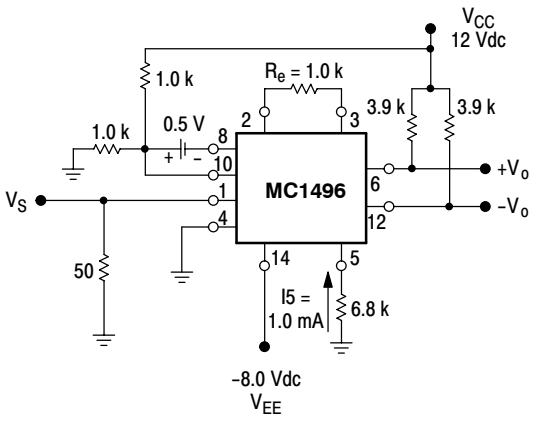


Figure 10. Signal Gain and Output Swing

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

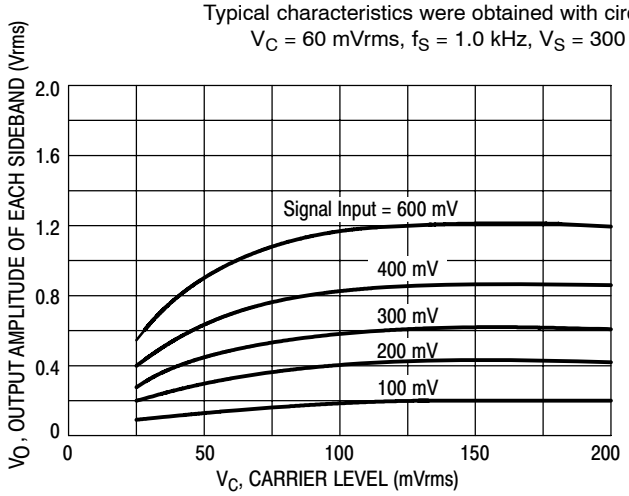


Figure 11. Sideband Output versus Carrier Levels

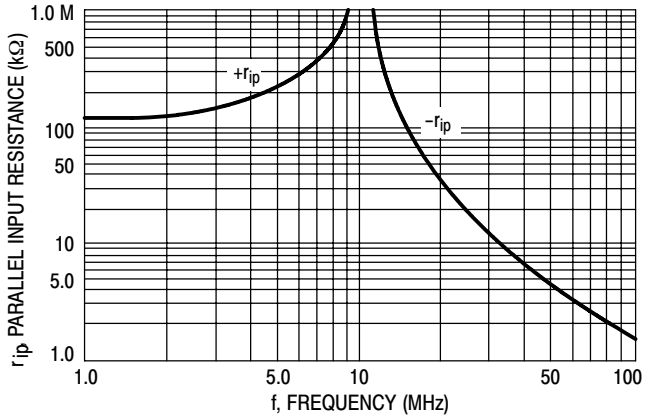


Figure 12. Signal−Port Parallel−Equivalent Input Resistance versus Frequency

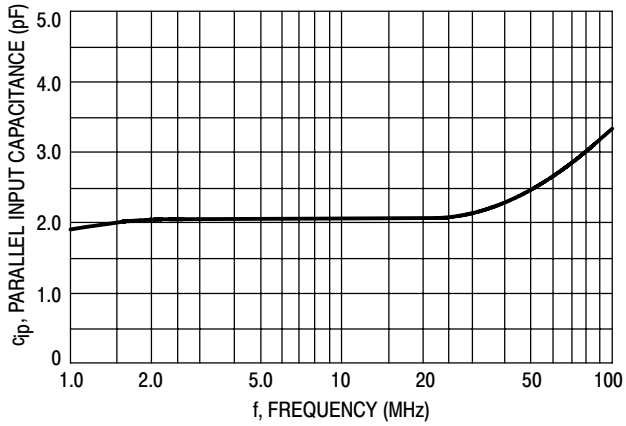


Figure 13. Signal−Port Parallel−Equivalent Input Capacitance versus Frequency

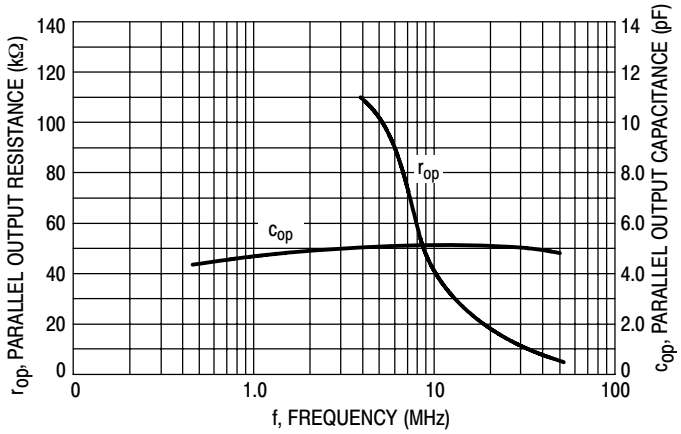


Figure 14. Single−Ended Output Impedance versus Frequency

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

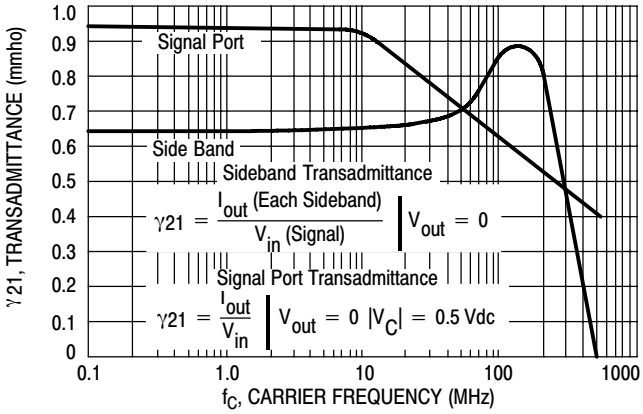


Figure 15. Sideband and Signal Port Transadmittances versus Frequency

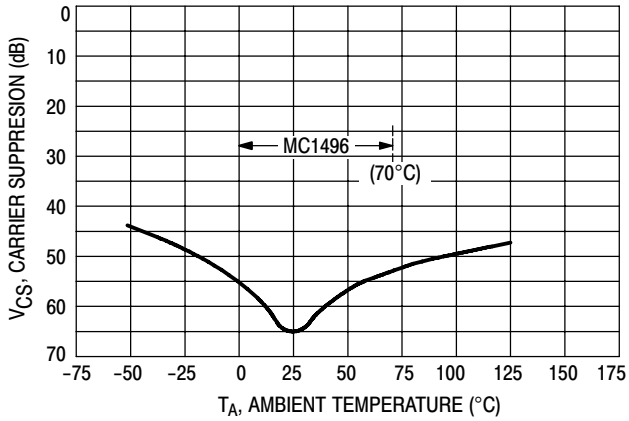


Figure 16. Carrier Suppression versus Temperature

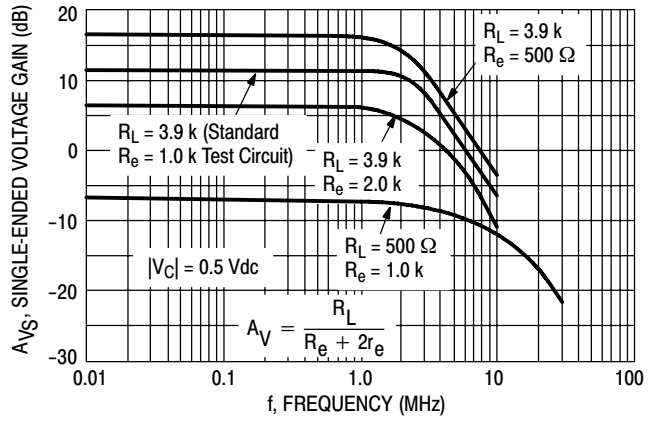


Figure 17. Signal−Port Frequency Response

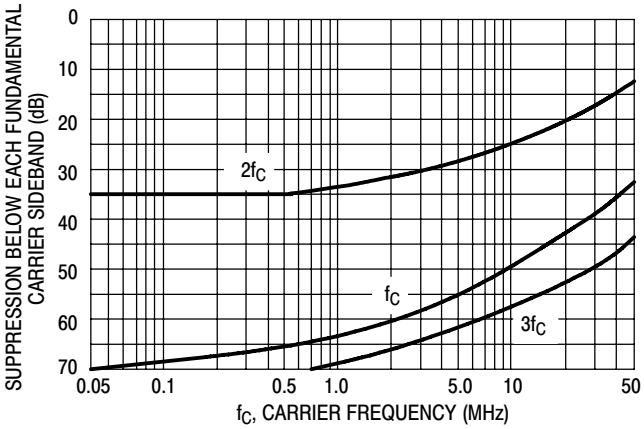


Figure 18. Carrier Suppression versus Frequency

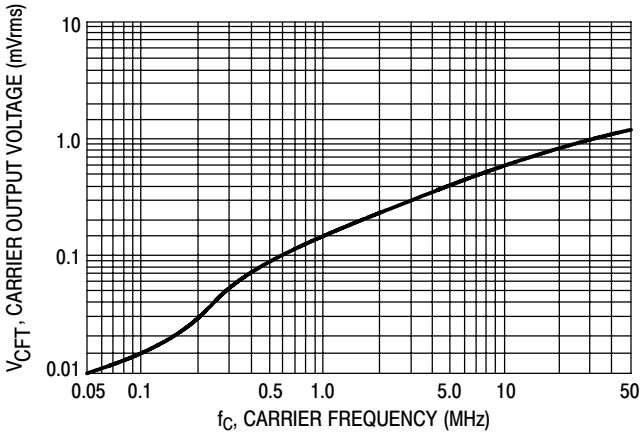


Figure 19. Carrier Feedthrough versus Frequency

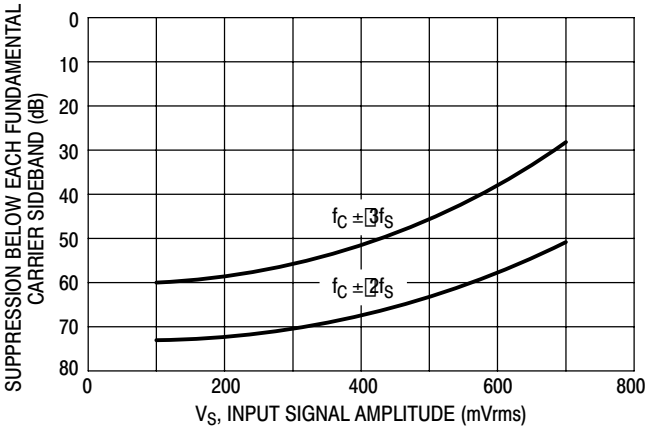


Figure 20. Sideband Harmonic Suppression versus Input Signal Level

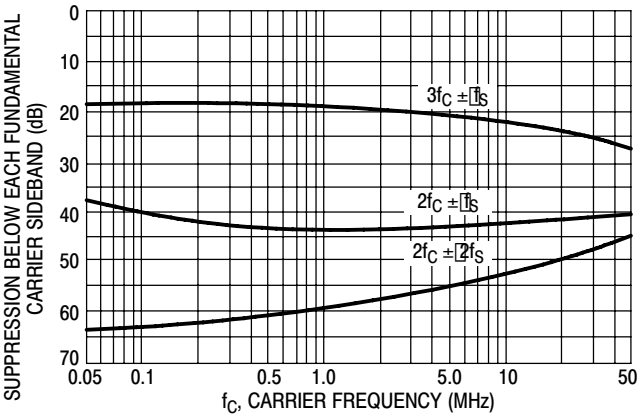


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

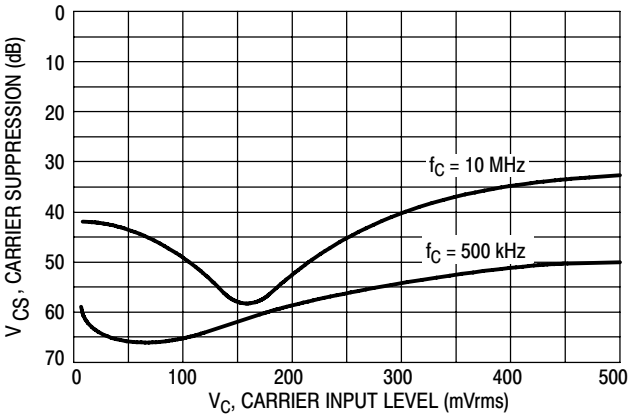


Figure 22. Carrier Suppression versus Carrier Input Level

OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross−coupled so that full−wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low−level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high−level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I5)\ (R_E)\ \text{volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

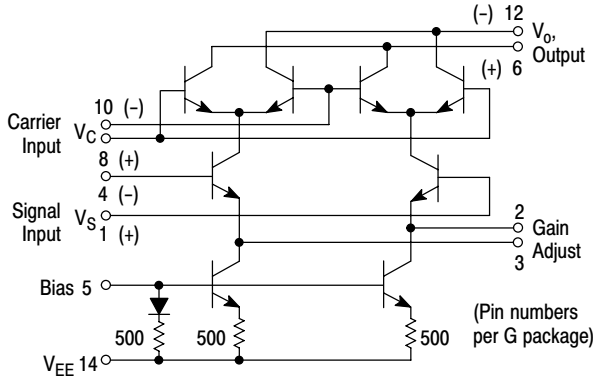


Figure 23. Circuit Schematic

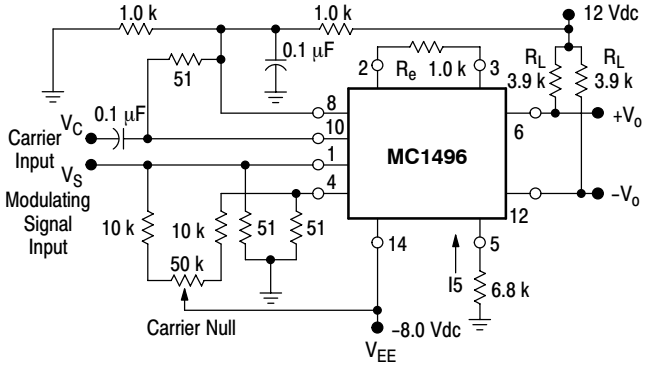


Figure 24. Typical Modulator Circuit

Table 1. Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low−level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High−level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low−level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High−level ac	$\frac{0.637\ R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

2. Low−level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
3. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude ofeach of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
4. All gain expressions are for a single−ended output. For a differential output connection, multiply each expression by two.
5. R_L = Load resistance.
6. R_E = Emitter resistance between Pins 2 and 3.
7. r_e = Transistor dynamic emitter resistance, at 25°C; $re \approx \frac{26\ mV}{I_5\ (mA)}$
8. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low−level modulating signal input and the following carrier input conditions:

1) Low−level dc
2) High−level dc
3) Low−level ac
4) High−level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 25 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 26 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 26 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 27.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 28).

This product detector has a sensitivity of 3.0 μV and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on Pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may

be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 29 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 30 and 31 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High−level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

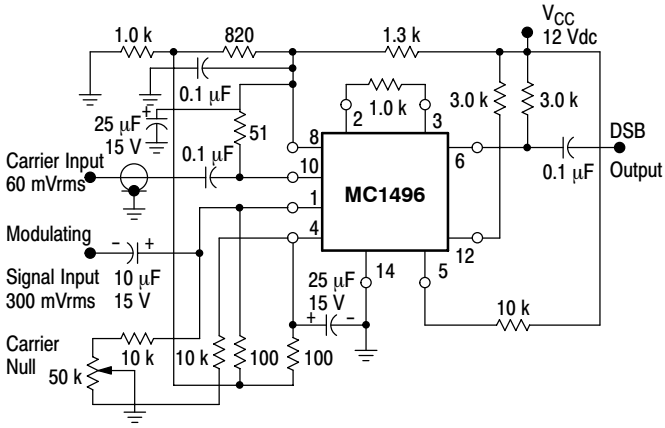


Figure 25. Balanced Modulator (12 Vdc Single Supply)

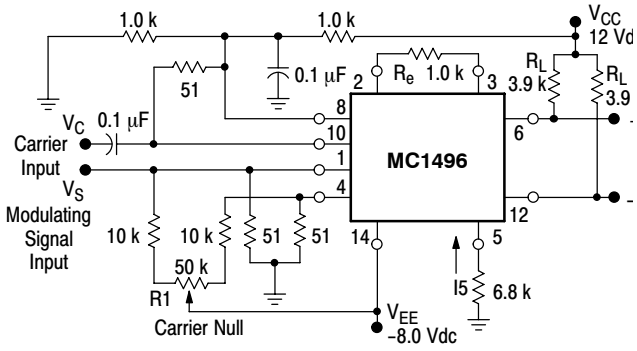


Figure 26. Balanced Modulator−Demodulator

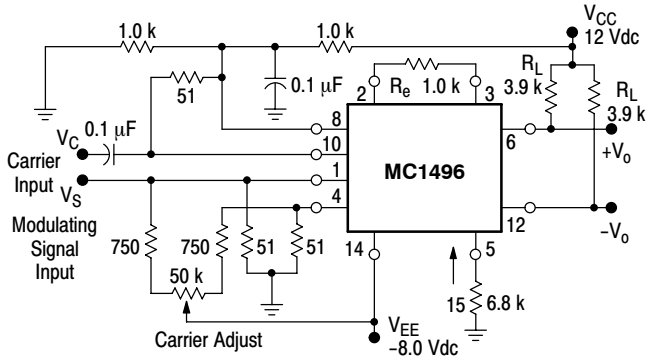


Figure 27. AM Modulator Circuit

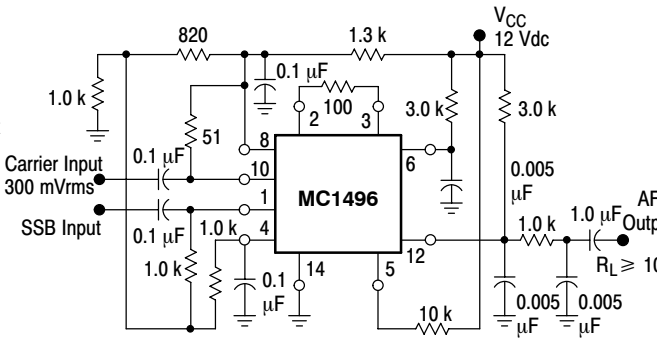
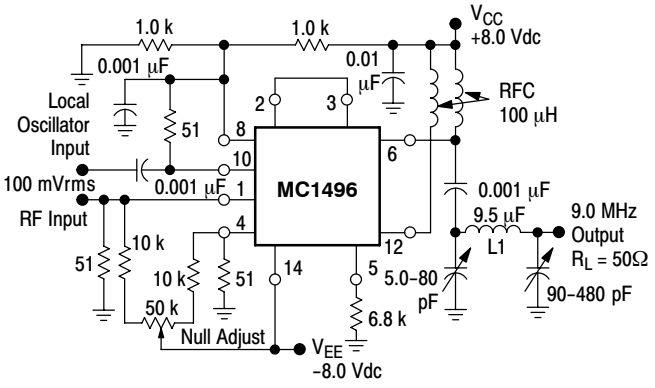


Figure 28. Product Detector (12 Vdc Single Supply)



L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44–6 Toroid Core.

Figure 29. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)

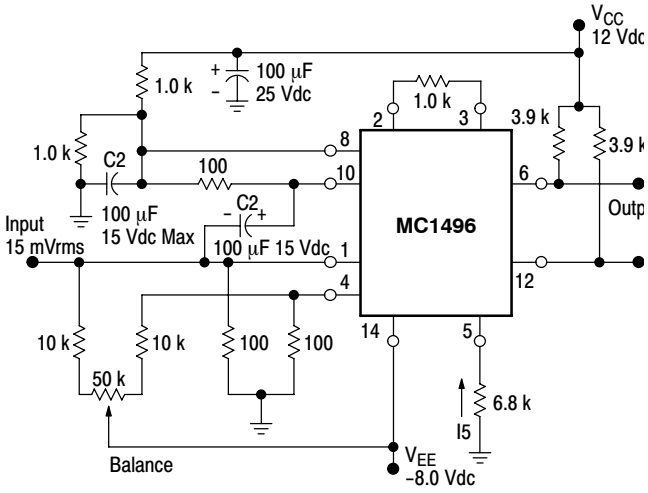
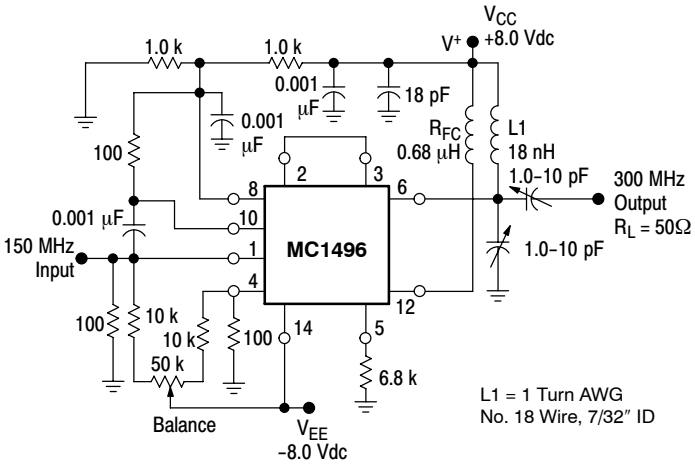
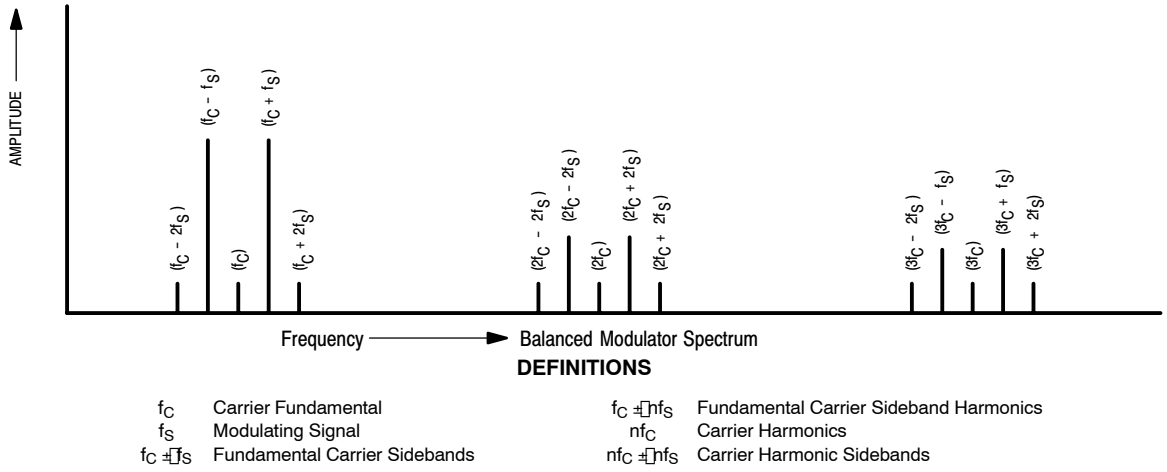


Figure 30. Low–Frequency Doubler



L1 = 1 Turn AWG No. 18 Wire, 7/32″ ID

Figure 31. 150 to 300 MHz Doubler



DEFINITIONS

f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands

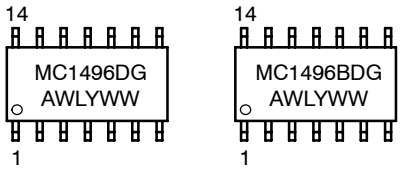
ORDERING INFORMATION

Device	Package	Shipping†
MC1496D	SOIC−14	55 Units/Rail
MC1496DG	SOIC−14 (Pb−Free)	
MC1496DR2	SOIC−14	2500 Tape & Reel
MC1496DR2G	SOIC−14 (Pb−Free)	
MC1496P	PDIP−14	25 Units/Rail
MC1496PG	PDIP−14 (Pb−Free)	
MC1496P1	PDIP−14	
MC1496P1G	PDIP−14 (Pb−Free)	
MC1496BD	SOIC−14	55 Units/Rail
MC1496BDG	SOIC−14 (Pb−Free)	
MC1496BDR2	SOIC−14	2500 Tape & Reel
MC1496BDR2G	SOIC−14 (Pb−Free)	
MC1496BP	PDIP−14	25 Units/Rail
MC1496BPG	PDIP−14 (Pb−Free)	

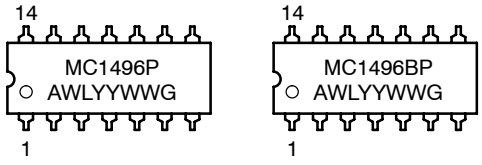
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

SOIC−14
D SUFFIX
CASE 751A



PDIP−14
P SUFFIX
CASE 646



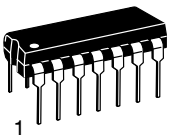
A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb−Free Package

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015



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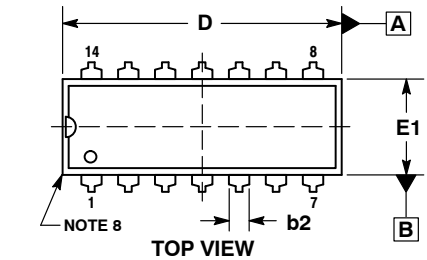
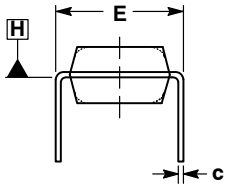
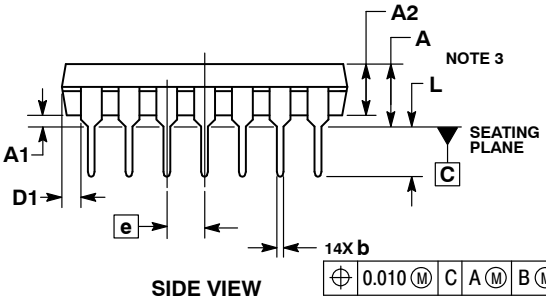


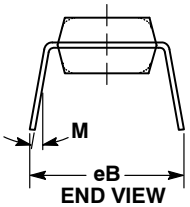
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

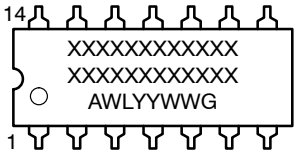


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42428B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	PDIP−14		PAGE 1 OF 2

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
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3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

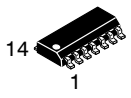
STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

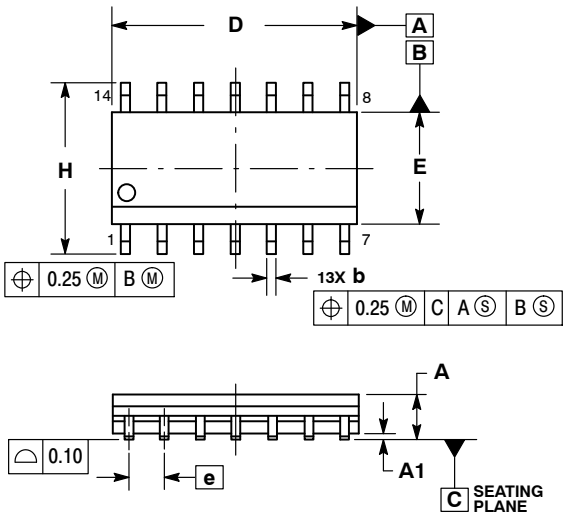
ON Semiconductor®

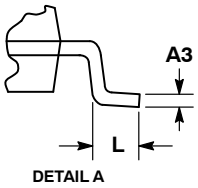


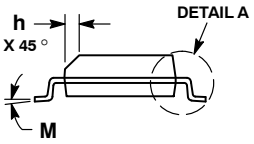
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



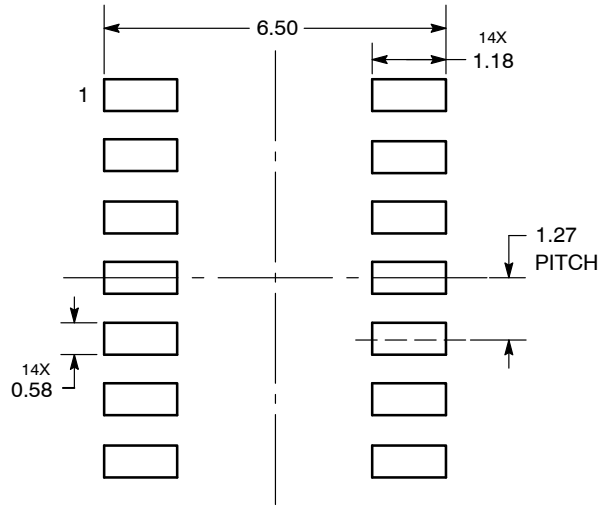




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

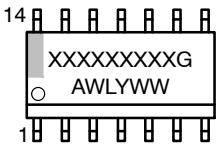
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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