

# 74LV164

## 8-bit serial-in/parallel-out shift register

Rev. 6 — 15 September 2021

Product data sheet

### 1. General description

The 74LV164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transition of the clock input (CP). A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs.

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess  $V_{CC}$ .

### 2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- CMOS low power dissipation
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce):  $< 0.8$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot):  $> 2$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Gated serial data inputs
- Asynchronous master reset
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from  $-40$  °C to  $+80$  °C and from  $-40$  °C to  $+125$  °C.

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV164D	$-40$ °C to $+125$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164PW	$-40$ °C to $+125$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ	$-40$ °C to $+125$ °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

### 4. Functional diagram

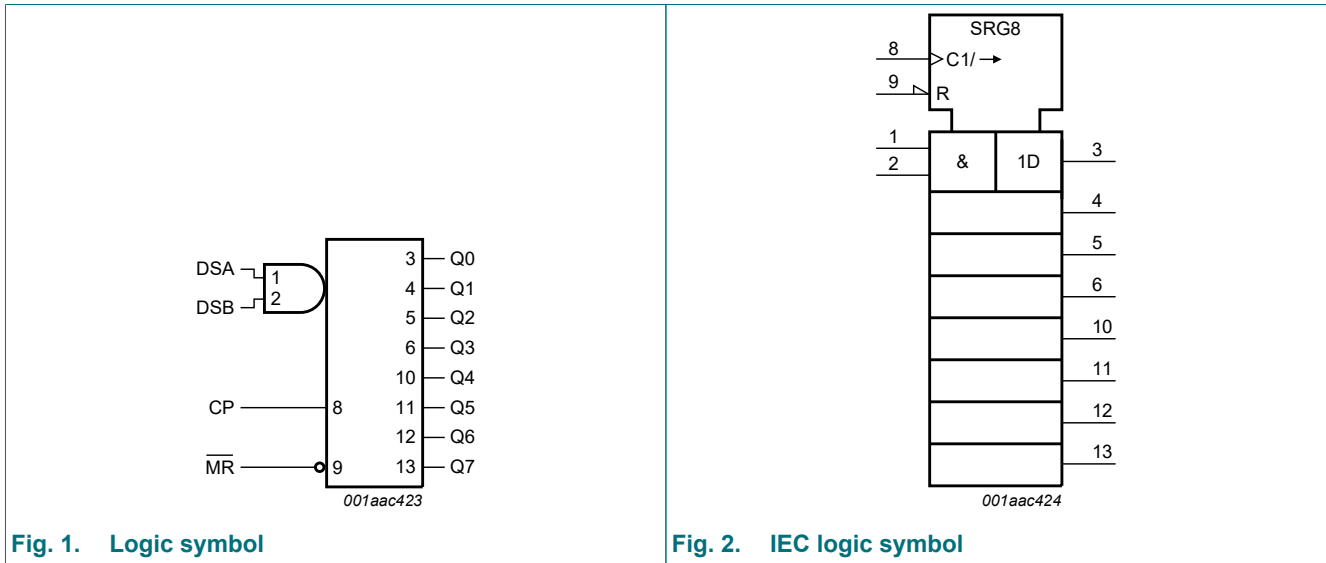


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

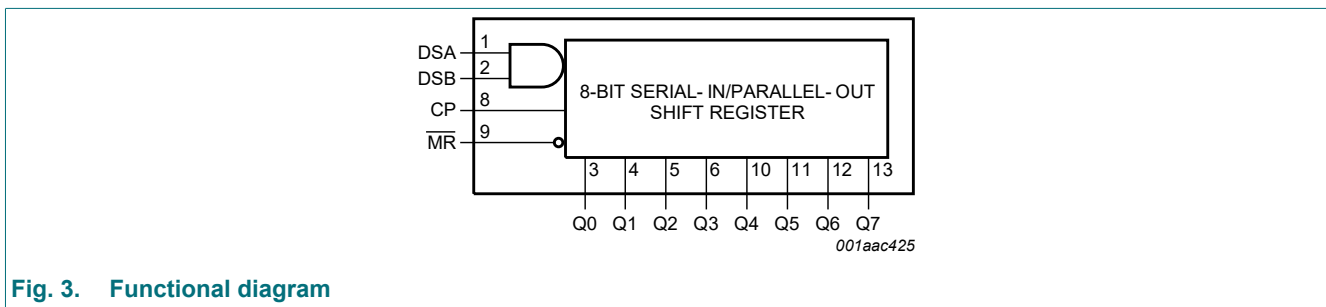


Fig. 3. Functional diagram

### 5. Pinning information

#### 5.1. Pinning

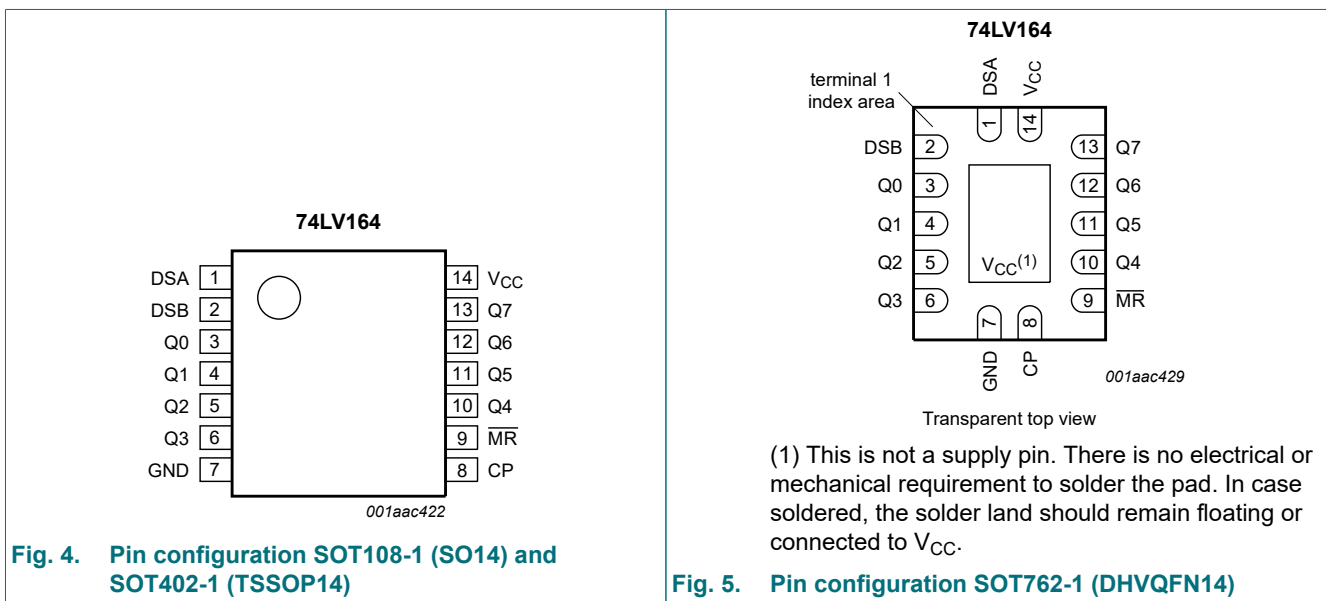


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{\text{MR}}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition;  
↑ = LOW-to-HIGH clock transition.*

Operating mode	Input				Output	
	$\overline{\text{MR}}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 50$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
 For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.  
 For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	[1]	1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to $2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to $2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to $5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

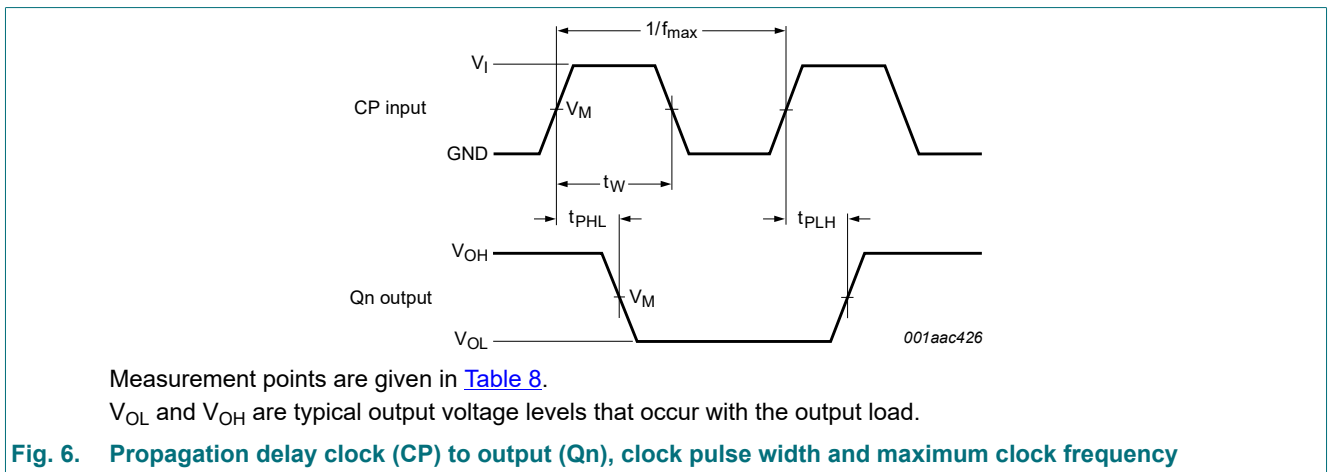
$GND = 0\text{ V}$ ; For test circuit see [Fig. 9](#).

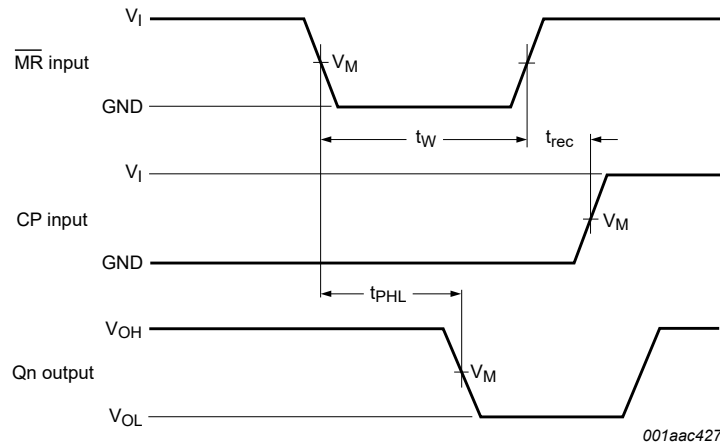
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Fig. 6</a> [2]						
		$V_{CC} = 1.2\text{ V}$	-	75	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	26	39	-	49	ns
		$V_{CC} = 2.7\text{ V}$	-	19	29	-	36	ns
		$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	12	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	14	23	-	29	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	-	12	19	-	24	ns
$t_{PHL}$	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see <a href="#">Fig. 7</a>						
		$V_{CC} = 1.2\text{ V}$	-	75	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	26	39	-	49	ns
		$V_{CC} = 2.7\text{ V}$	-	19	29	-	36	ns
		$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	12	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	14	23	-	29	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	-	12	19	-	24	ns
$t_W$	pulse width	CP; see <a href="#">Fig. 6</a>						
		$V_{CC} = 2.0\text{ V}$	34	9	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	6	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	20	5	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	13	4	-	16	-	ns
		$\overline{MR}$ ; <a href="#">Fig. 7</a>						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	20	6	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	13	5	-	16	-	ns
$t_{rec}$	recovery time	$\overline{MR}$ to CP; see <a href="#">Fig. 7</a>						
		$V_{CC} = 1.2\text{ V}$	-	30	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	19	10	-	24	-	ns
		$V_{CC} = 2.7\text{ V}$	14	8	-	18	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	11	6	-	14	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	8	5	-	10	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Fig. 8</a>						
		$V_{CC} = 1.2\text{ V}$	-	15	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	22	5	-	26	-	ns
		$V_{CC} = 2.7\text{ V}$	16	4	-	19	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	13	3	-	15	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]	9	2	-	10	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>h</sub>	hold time	Dn to CP; see Fig. 8						
		V <sub>CC</sub> = 1.2 V	-	-10	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	5	-3	-	5	-	ns
		V <sub>CC</sub> = 2.7 V	5	-2	-	5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [3]	5	-2	-	5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [3]	5	-1	-	5	-	ns
f <sub>max</sub>	maximum frequency	see Fig. 6						
		V <sub>CC</sub> = 2.0 V	14	40	-	12	-	MHz
		V <sub>CC</sub> = 2.7 V	19	58	-	16	-	MHz
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	78	-	-	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V [3]	24	70	-	20	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V [3]	36	100	-	30	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	40	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V  
 N = number of inputs switching  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

### 10.1. Waveforms and test circuit

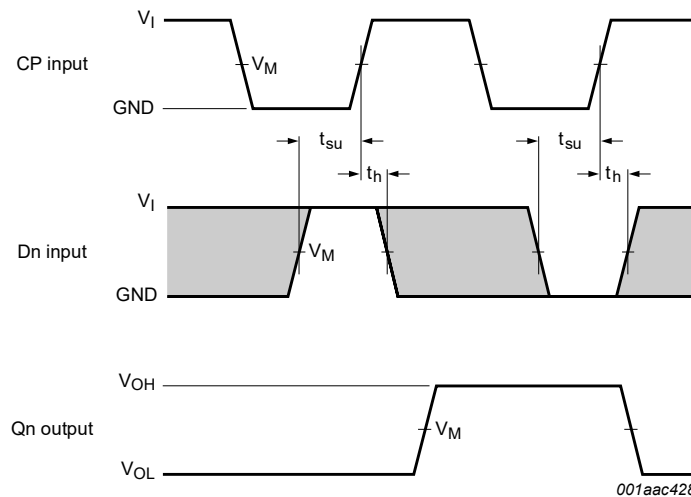




Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 7. Pulse width master reset ( $\overline{MR}$ ), propagation delay master reset ( $\overline{MR}$ ) to output ( $Q_n$ ) and the master reset ( $\overline{MR}$ ) to clock (CP) recovery time**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

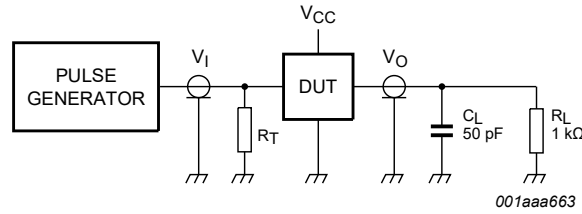
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 8. Data set-up and hold times inputs ( $D_n$ ) to clock (CP)**

**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$





Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig. 9. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		Test
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
1.2 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.0 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF, 15 pF	1 kΩ	$t_{PHL}, t_{PLH}$
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$

### 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

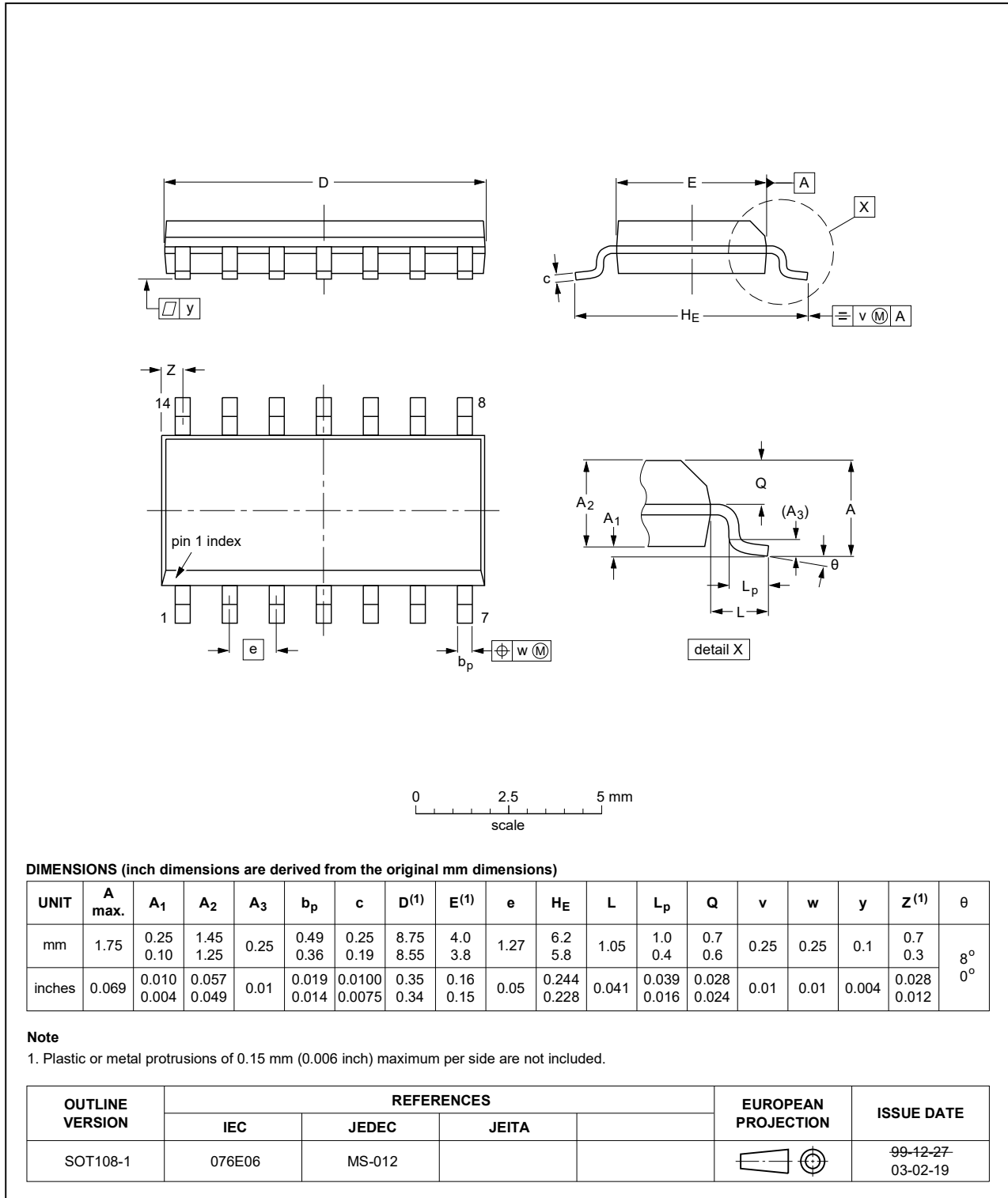


Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

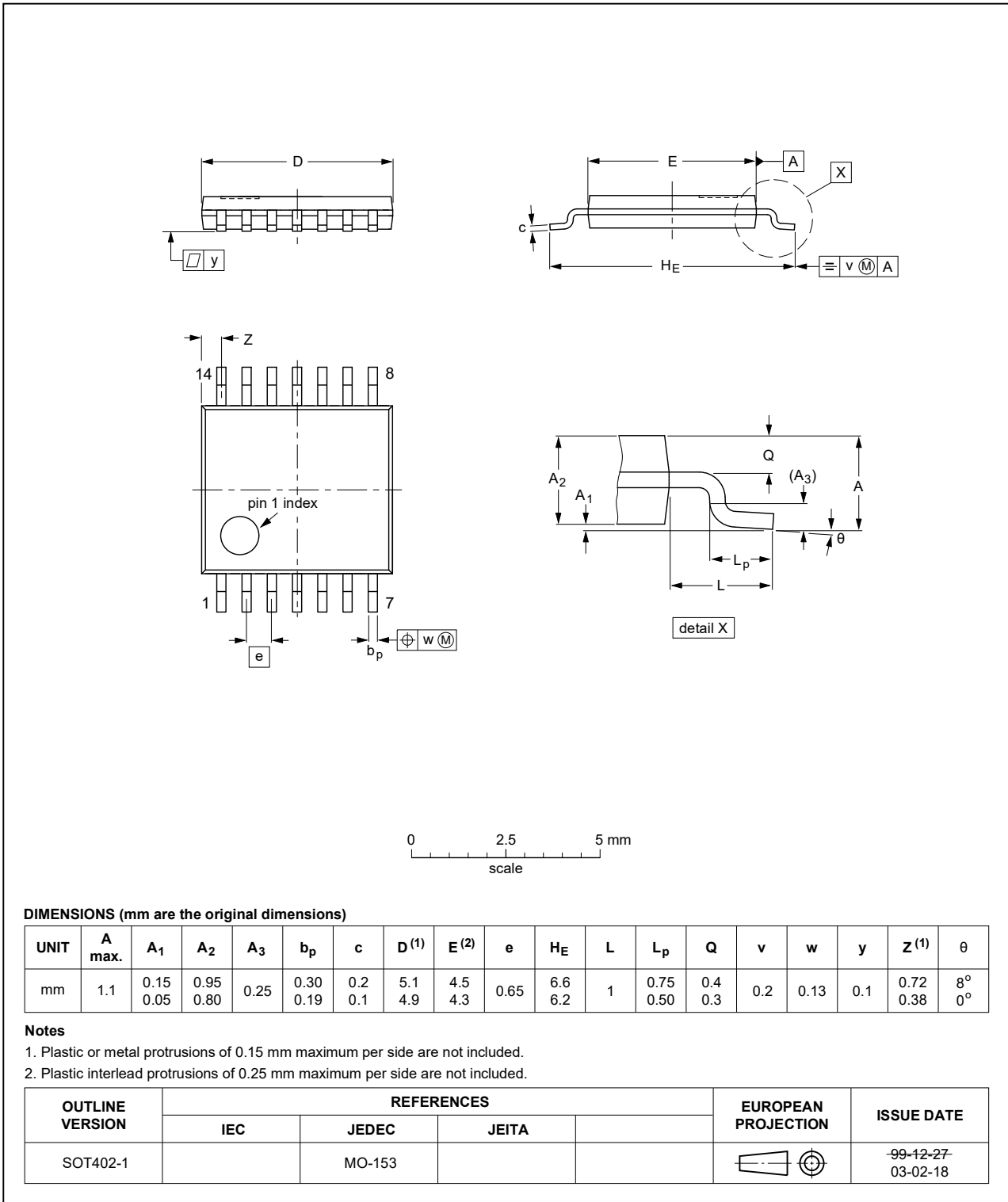


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

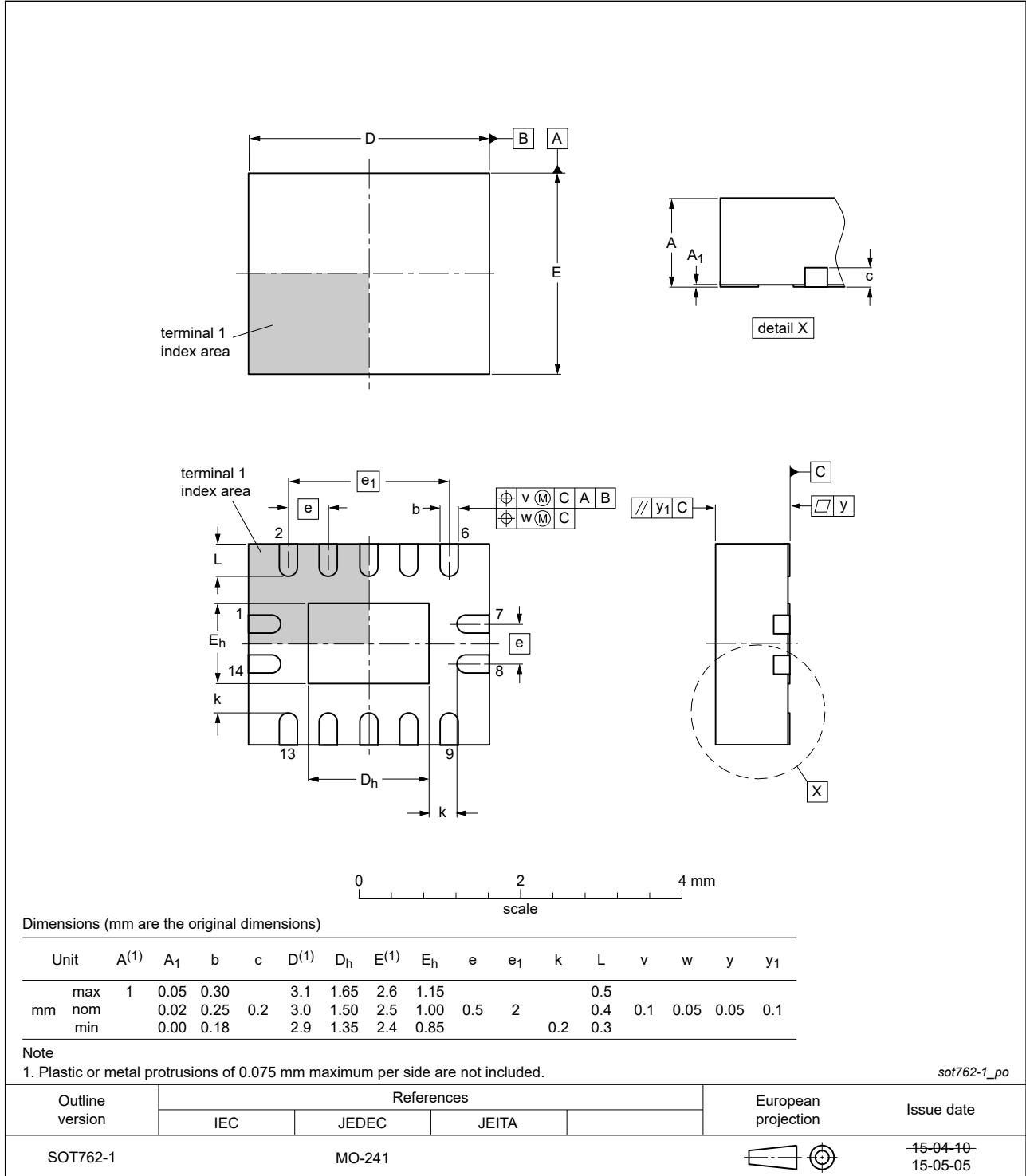


Fig. 12. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV164 v.6	20210915	Product data sheet	-	74LV164 v.5
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV164DB (SOT337-1/SSPO14) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
74LV164 v.5	20200915	Product data sheet	-	74LV164 v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74LV164 v.4	20151209	Product data sheet	-	74LV164 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV164N (SOT27-1) removed.</li> </ul>			
74LV164 v.3	20050204	Product data sheet	-	74LV164 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors</li> <li>Added: type number 74LV164BQ (DHSVQFN14 package).</li> </ul>			
74LV164 v.2	19980507	Product specification	-	74LV164 v.1
74LV164 v.1	19970328	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 15 September 2021

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