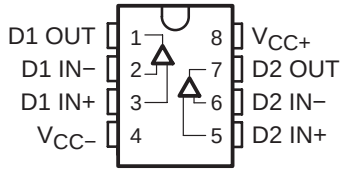
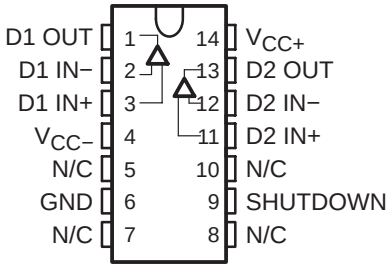
- **Remote Terminal ADSL Line Driver**
  - **Ideal for Both Full Rate ADSL and G.Lite**
  - **Compatible With 1:2 Transformer Ratio**
- **Wide Supply Voltage Range +5 V to +14 V**
  - **Ideal for Single Supply +12-V Operation**
- **Low 2.1 pA/$\sqrt{\text{Hz}}$ Noninverting Current Noise**
  - **Reduces Noise Feedback Through Hybrid Into Downstream Channel**
- **Wide Output Swing**
  - **18.4 Vpp Differential Output Voltage, $R_L$ = 50 Ω, 12-V Single Supply**
- **High Output Current**
  - **275 mA (typ)**
- **High Speed**
  - **100 MHz (−3 dB, G=1, 12-V Single Supply)**
  - **600 V/μs Slew Rate (G = 4, 12-V Single Supply)**
- **Low Distortion, Single-Ended, G = 4**
  - **−72 dBc (250 kHz, 2 Vpp, 25 Ω load)**
  - **−78 dBc (250 kHz, 2 Vpp, 100 Ω load)**
- **Low Power Shutdown (THS6093)**
  - **300 μA Total Standby Current**
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

**THS6092**
**SOIC (D) AND**
**SOIC PowerPAD™ (DDA) PACKAGE**
**(TOP VIEW)**

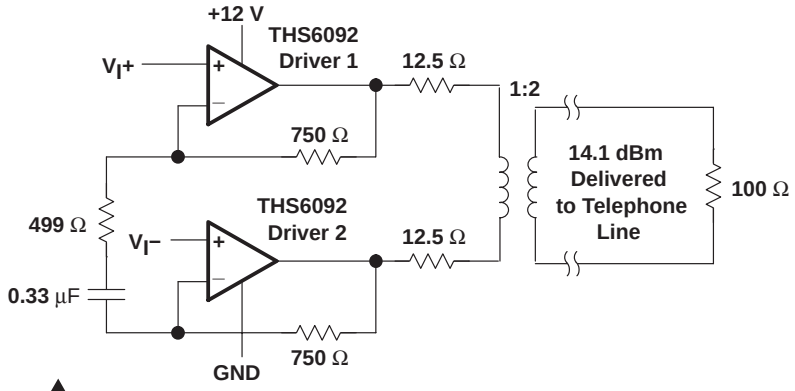



**THS6093**
**SOIC (D) AND**
**TSSOP PowerPAD™ (PWP) PACKAGE**
**(TOP VIEW)**




## description

The THS6092/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from a single +12-V supply voltage while drawing only 7.3 mA of supply current per channel. It offers low –72 dBc total harmonic distortion driving a 25-Ω load (2 Vpp). The THS6092/3 offers a high 18.4-Vpp differential output swing across a 50-Ω load from a single +12-V supply. The THS6093 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6092/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ package.




**RELATED PRODUCTS**

| DEVICE | DESCRIPTION |
|---|---|
| THS6042/3 | 350-mA, ±12 ADSL CPE line driver |
| THS6052/3 | 175-mA, ±12 V ADSL CPE line driver |
| OPA2677 | 380-mA, +12 V ADSL CPE line driver |
| THS6062 | Low noise ADSL receiver |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICE | | | | EVALUATION MODULES |
|---|---|---|---|---|---|
| | SOIC-8† (D) | SOIC-8† PowerPAD (DDA) | SOIC-14† (D) | TSSOP-14† PowerPAD (PWP) | |
| 0°C to 70°C | THS6092CD | THS6092CDDA | THS6093CD | THS6093CPWP | THS6092EVM THS6093EVM |
| −40°C to 85°C | THS6092ID | THS6092IDDA | THS6093ID | THS6093IPWP | — |

† All packages are available taped and reeled. Add an R-suffix to the device type (i.e., THS6092IDR).

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC+}$ to $V_{CC-}$ . . . . . 14.7 V
Input voltage . . . . . ± $V_{CC}$
Output current (see Note 1) . . . . . 350 mA
Differential input voltage . . . . . ± 3 V
Maximum junction temperature . . . . . 150°C
Total power dissipation at (or below) 25°C free-air temperature . . . . . See Dissipation Ratings Table
Operating free-air temperature, $T_A$: Commercial . . . . . 0°C to 70°C
Industrial . . . . . −40°C to 85°C
Storage temperature, $T_{stg}$ : Commercial . . . . . −65°C to 125°C
Industrial . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6092 and THS6093 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

**DISSIPATION RATING TABLE**

| PACKAGE | $\theta_{JA}$ | $\theta_{JC}$ | $T_A$ = 25°C§ POWER RATING | $T_A$ = 70°C§ POWER RATING | $T_A$ = 85°C§ POWER RATING |
|---|---|---|---|---|---|
| D-8 | 95°C/W‡ | 38.3°C/W‡ | 1.1 W | 0.63 W | 0.47 W |
| DDA | 45.8°C/W | 9.2°C/W | 2.3 W | 1.31 W | 0.98 W |
| D-14 | 66.6°C/W‡ | 26.9°C/W‡ | 1.6 W | 0.90 W | 0.68 W |
| PWP | 37.5°C/W | 1.4°C/W | 2.8 W | 1.60 W | 1.20 W |

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the $\Theta_{JA}$ is168°C/W for the D−8 package and 122.3°C/W for the D−14 package.

§ Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC+}$ to $V_{CC-}$ | Dual supply | ±2.5 | | ±7 | V |
| | Single supply | +5 | | +14 | |
| Operating free-air temperature, $T_A$ | C-suffix | 0 | | 70 | °C |
| | I-suffix | −40 | | 85 | |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC+}$ = 12 V, $V_{CC-}$ = GND, $R_{FEEDBACK}$ = 750 Ω, $R_L$ = 25 Ω (unless otherwise noted)

### dynamic performance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| BW | Small-signal bandwidth (−3 dB) G=1 | $V_{CC}$ = 12 V | | 100 | | MHz |
| | | $V_{CC}$ = 5 V | | 90 | | |
| SR | Slew rate (see Note 2) | $V_{CC}$ = 12 V | | 600 | | V/μs |
| | | $V_{CC}$ = 5 V | | 400 | | |

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

### noise/distortion performance

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion (single-ended configuration) | | Gain = 4, $R_L$ = 25 Ω, $V_{CC}$ = 5 V, f = 250 kHz | $V_{O(pp)}$ = 2 V | | −70 | | dBc |
| | | | Gain = 4, $R_L$ = 25 Ω, $V_{CC}$ = 12 V, f = 250 kHz | $V_{O(pp)}$= 2 V | | −72 | | |
| | | | | $V_{O(pp)}$= 7 V | | −68 | | |
| $V_n$ | Input voltage noise | | $V_{CC}$ = 12 V, 5 V, f = 10 kHz | | | 2.1 | | nV/√Hz |
| $I_n$ | Input current noise | +Input | $V_{CC}$ = 12 V, 5 V, f = 10 kHz | | | 2.1 | | pA/√Hz |
| | | −Input | | | | 10.9 | | |
| $X_T$ | Crosstalk | | f = 250 kHz, G = 4, $V_O$ = 2 Vpp, $R_L$= 25 Ω | $V_{CC}$ = 5 V | | −65 | | dBc |
| | | | | $V_{CC}$ = 12 V | | −63 | | |

### dc performance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | $V_{CC}$ = 12 V, 5 V | $T_A$ = 25°C | | 6 | 16 | mV |
| | | | $T_A$ = full range | | | 21 | |
| | Differential offset voltage | | $T_A$ = 25°C | | 1 | 6 | |
| | | | $T_A$ = full range | | | 8 | |
| | Offset drift | | $T_A$ = full range | | 20 | | μV/°C |
| $I_{IB}$ | − Input bias current | $V_{CC}$ = 12 V, 5 V | $T_A$ = 25°C | | 3 | 10 | μA |
| | | | $T_A$ = full range | | | 12 | |
| | + Input bias current | | $T_A$ = 25°C | | 1 | 6 | |
| | | | $T_A$ = full range | | | 7 | |
| | Differential input bias current | | $T_A$ = 25°C | | 3 | 10 | |
| | | | $T_A$ = full range | | | 12 | |
| $Z_{OL}$ | Open loop transimpedance | $R_L$ = 1 kΩ | $V_{CC}$ = 12 V, 5 V | | 0.9 | | MΩ |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC+}$ = 12 V, $V_{CC-}$ = GND, $R_{FEEDBACK}$ = 750 Ω, $R_L$ = 25 Ω (unless otherwise noted) (continued)

### input characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ICR}$ | Input common-mode voltage range | $V_{CC}$ = 5 V | $T_A$ = 25°C | 1.5 to 3.5 | 1.1 to 3.9 | | V |
| | | | $T_A$ = full range | 1.6 to 3.4 | | | |
| | | $V_{CC}$ = 12 V | $T_A$ = 25°C | 2.3 to 9.7 | 1.8 to 10.2 | | |
| | | | $T_A$ = full range | 2.4 to 9.6 | | | |
| CMRR | Common-mode rejection ratio | $V_{CC}$ = 5 V | $T_A$ = 25°C | 56 | 63 | | dB |
| | | | $T_A$ = full range | 54 | | | |
| | | $V_{CC}$ = 12 V | $T_A$ = 25°C | 50 | 56 | | |
| | | | $T_A$ = full range | 48 | | | |
| $R_I$ | Input resistance | + Input | | | 1 | | MΩ |
| | | −Input | | | 15 | | Ω |
| $C_I$ | Input capacitance | | | | 2 | | pF |

### output characteristics

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage swing | Single ended 100 mV overdrive | $R_L$ = 25 Ω | $V_{CC}$ = 5 V | 1.4 to 3.6 | 1.1 to 3.9 | | V |
| | | | | $V_{CC}$ = 12 V | 1.9 to 10.1 | 1.4 to 10.6 | | |
| | | | $R_L$ = 100 Ω | $V_{CC}$ = 5 V | 1.3 to 3.7 | 1.05 to 3.95 | | |
| | | | | $V_{CC}$ = 12 V | 1.5 to 10.5 | 1.1 to 10.9 | | |
| $I_O$ | Output current | | $R_L$ = 3.6 Ω, | $V_{CC}$ = 5 V | | 240 | | mA |
| | | | $R_L$ = 10 Ω, | $V_{CC}$ = 12 V | 240 | 275 | | |
| $I_{SC}$ | Short-circuit current | | $R_L$ = 0 Ω, | $V_{CC}$ = 12 V | | 325 | | mA |
| | Output resistance | | Open loop | | | 15 | | Ω |

### power supply

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating range | Dual supply | | | ±2.25 | | ±7 | V |
| | | Single supply | | | 4.5 | | 14 | |
| $I_{CC}$ | Quiescent current (each driver) | | $V_{CC}$ = 5 V | $T_A$ = 25°C | | 6.7 | 8.8 | mA |
| | | | | $T_A$ = full range | | | 10 | |
| | | | $V_{CC}$ = 12 V | $T_A$ = 25°C | | 7.3 | 9.5 | mA |
| | | | | $T_A$ = full range | | | 10.5 | |
| PSRR | Power supply rejection ratio | | $V_{CC}$ = 5 V | $T_A$ = 25°C | -54 | −58 | | dB |
| | | | | $T_A$ = full range | -46 | − | | |
| | | | $V_{CC}$ = 12 V | $T_A$ = 25°C | -58 | −70 | | |
| | | | | $T_A$ = full range | -50 | | | |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC+}$ = 12 V, $V_{CC-}$ = GND, $R_{FEEDBACK}$ = 750 Ω, $R_L$ = 25 Ω (unless otherwise noted) (continued)

### shutdown characteristics (THS6093 only)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL(SHDN)}$ | Shutdown pin voltage for power up | $V_{CC}$ = 12 V, GND = 6 V (GND Pin as Reference) | | | 0.8 | V |
| $V_{IH(SHDN)}$ | Shutdown pin voltage for power down | $V_{CC}$ = 12 V, GND = 6 V (GND Pin as Reference) | 2 | | | V |
| $I_{CC(SHDN)}$ | Total quiescent current when in shutdown state | $V_{SHDN}$ = 8 V, $V_{GND}$ = 6 V, $V_{CC}$ = 12 V | | 0.3 | 0.7 | mA |
| $t_{DIS}$ | Disable time (see Note 3) | $V_{CC}$ = 12 V | | 0.2 | | µs |
| $t_{EN}$ | Enable time (see Note 3) | $V_{CC}$ = 12 V | | 0.5 | | µs |
| $I_{IL(SHDN)}$ | Shutdown pin input bias current for power up | $V_{SHDN}$ = 6 V, $V_{GND}$ = 6 V, $V_{CC}$ = 12 V | | 40 | 100 | µA |
| $I_{IH(SHDN)}$ | Shutdown pin input bias current for power down | $V_{SHDN}$ = 9.3 V, $V_{GND}$ = 6 V, $V_{CC}$ = 12 V | | 50 | 100 | µA |

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

## APPLICATION INFORMATION

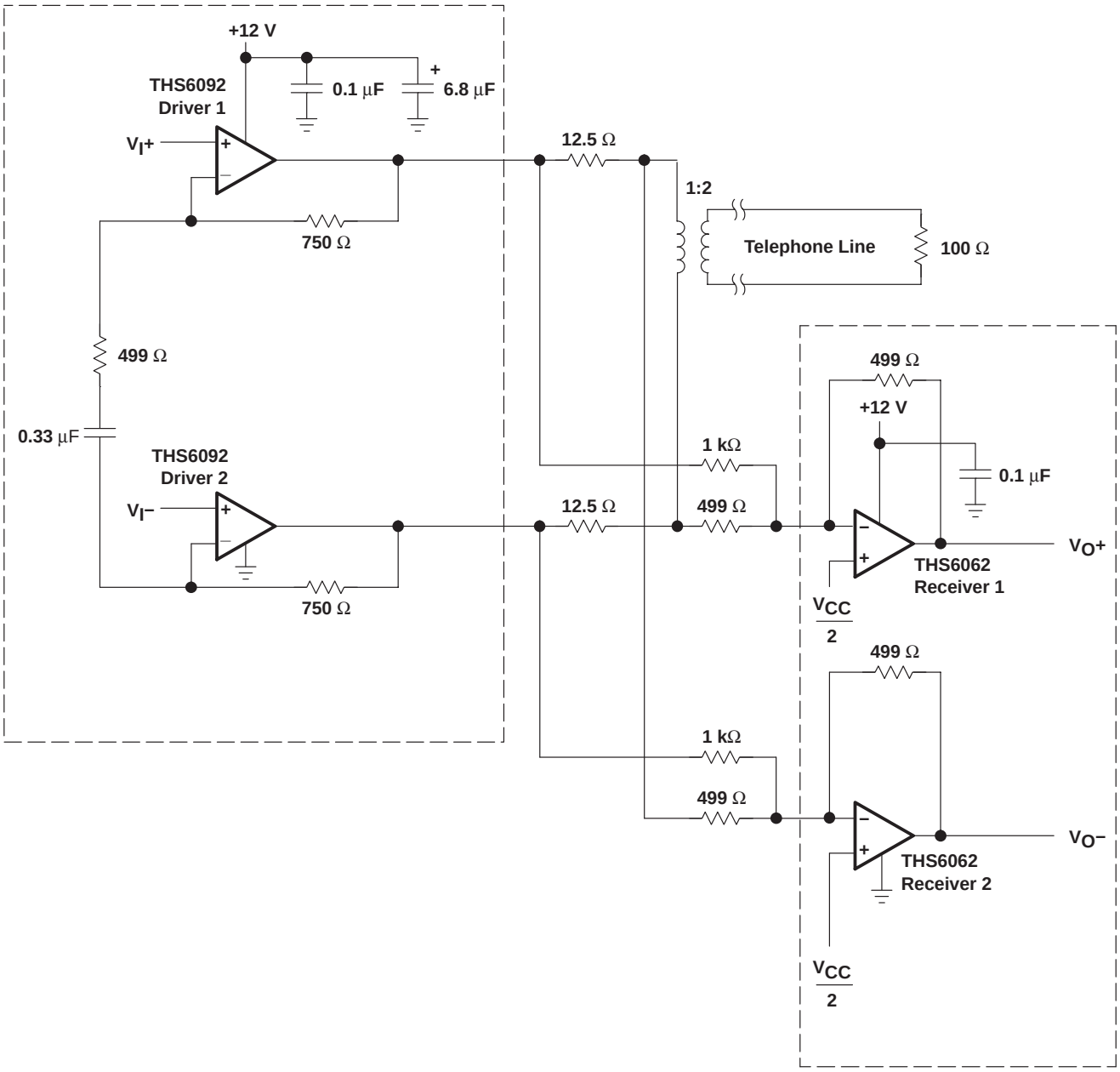



**Figure 1. THS6092 ADSL Application With 1:2 Transformer Ratio**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| THS6092ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 6092I | Samples |
| THS6092IDDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | 6092I | Samples |
| THS6093CPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | HS6093C | Samples |
| THS6093IPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS6093I | Samples |
| THS6093IPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS6093I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

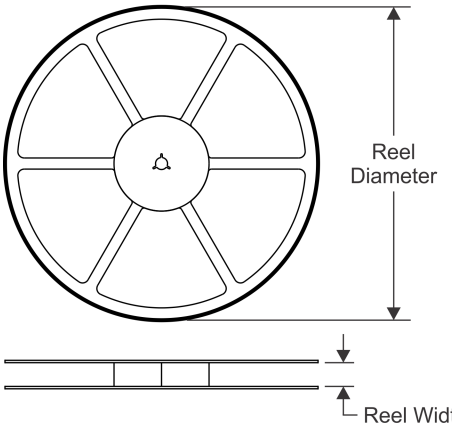
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

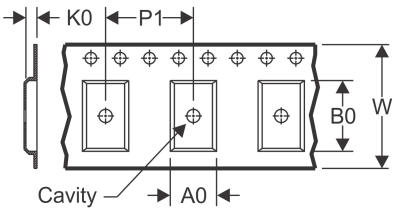
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

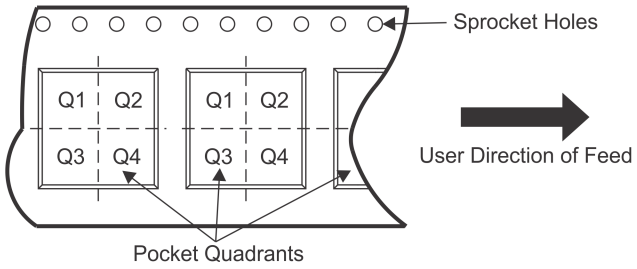



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

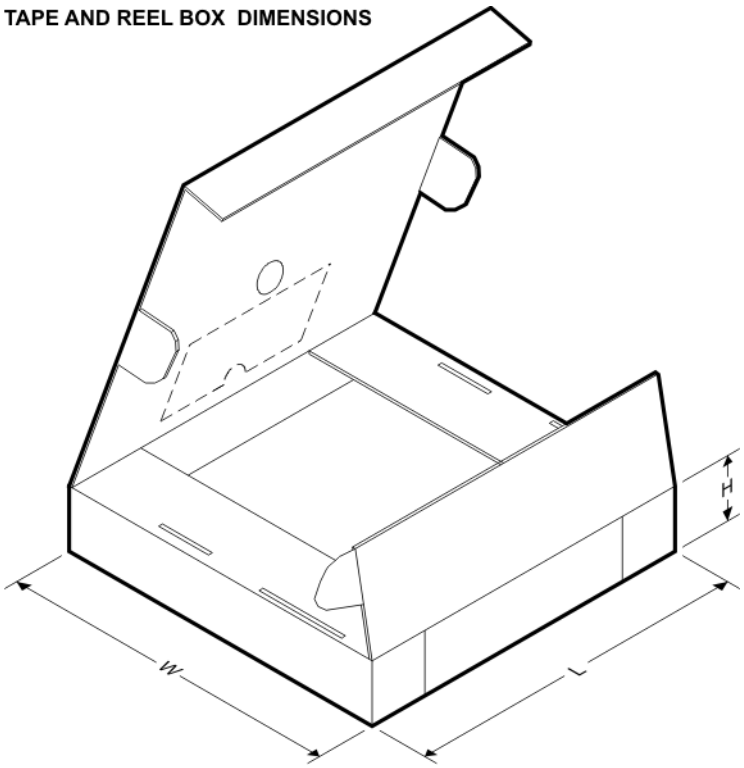
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS6092IDDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS6093CPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| THS6093IPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

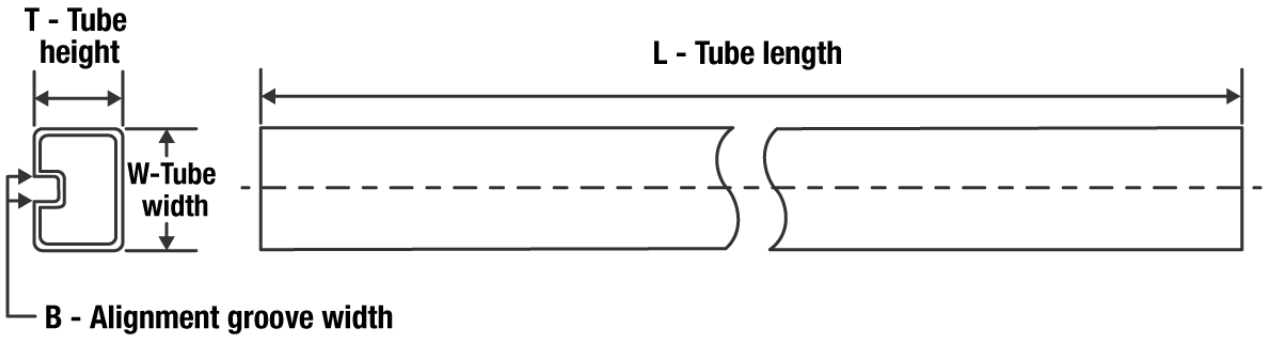
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS6092IDDAR | SO PowerPAD | DDA | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| THS6093CPWPR | HTSSOP | PWP | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| THS6093IPWPR | HTSSOP | PWP | 14 | 2000 | 350.0 | 350.0 | 43.0 |

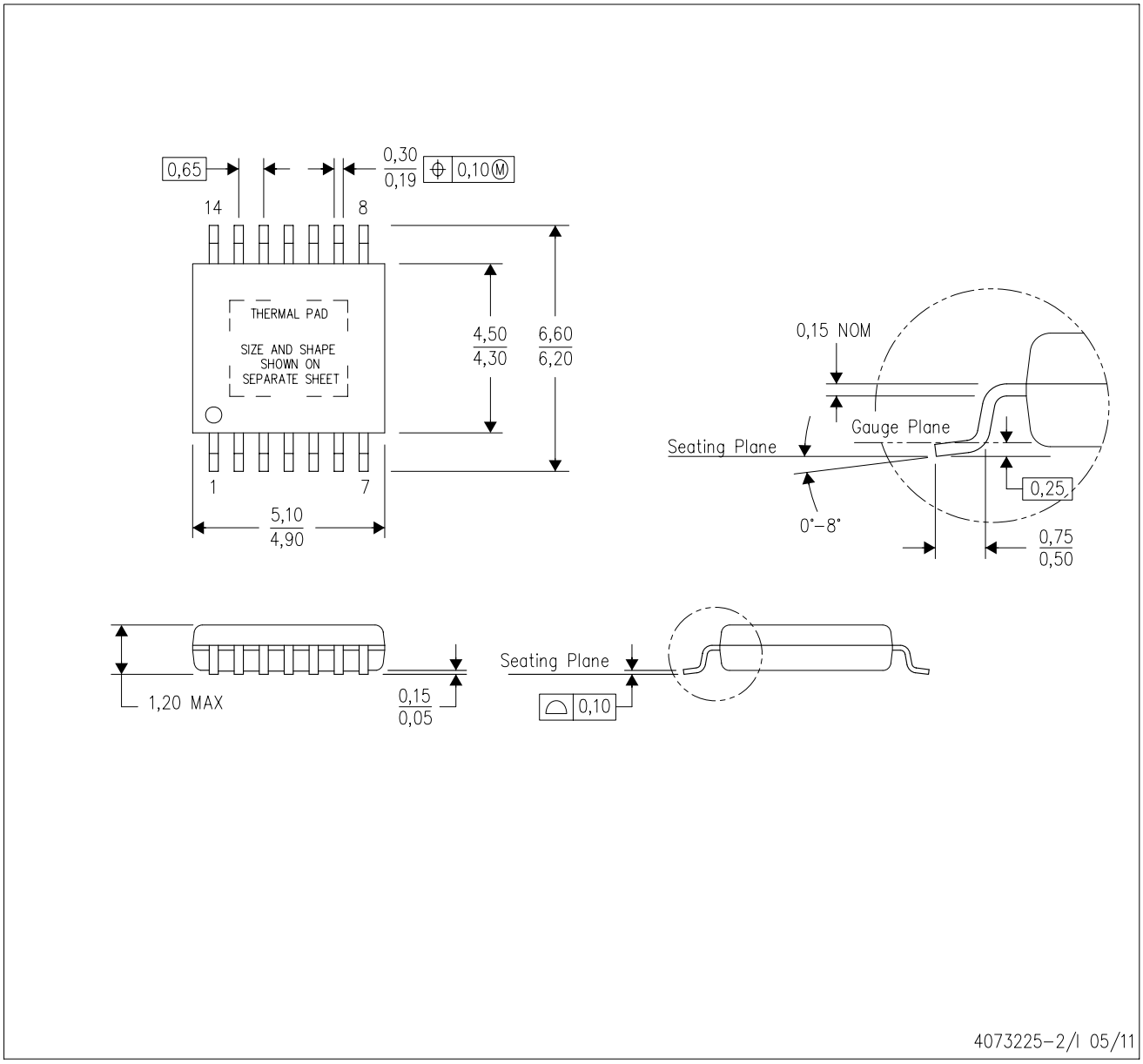
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| THS6092ID | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| THS6093IPWP | PWP | HTSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

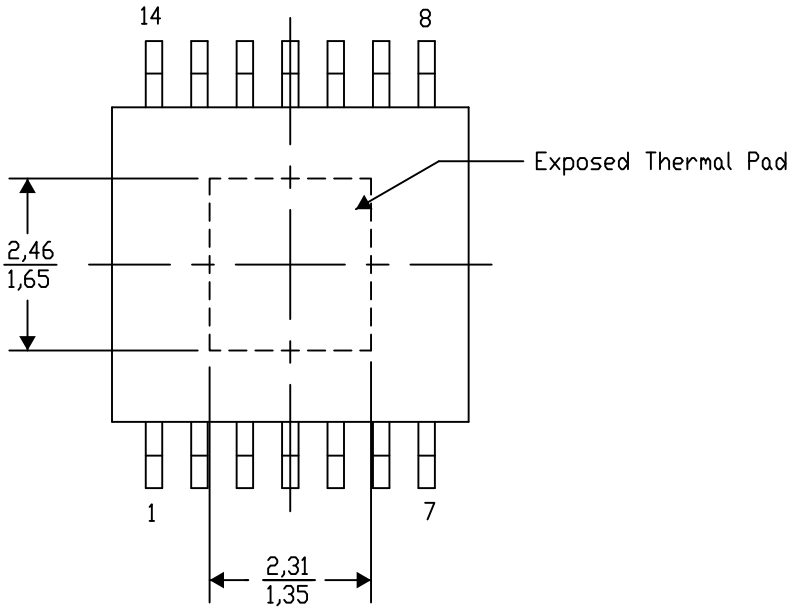
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

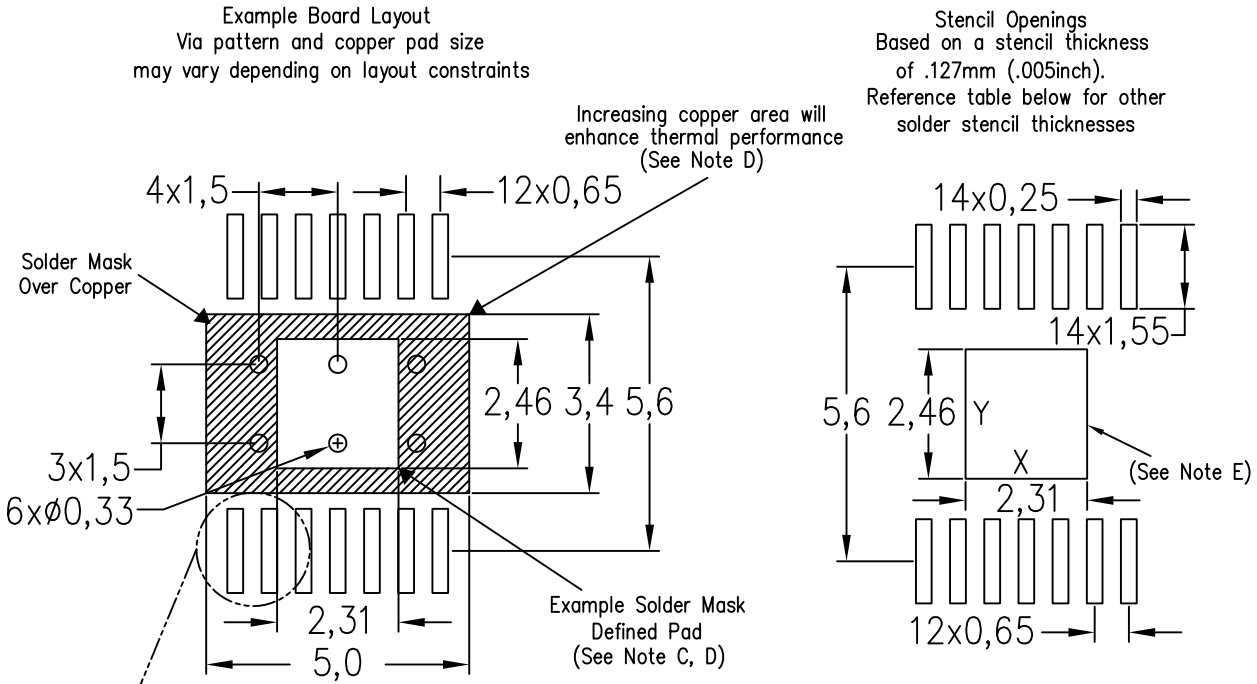
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

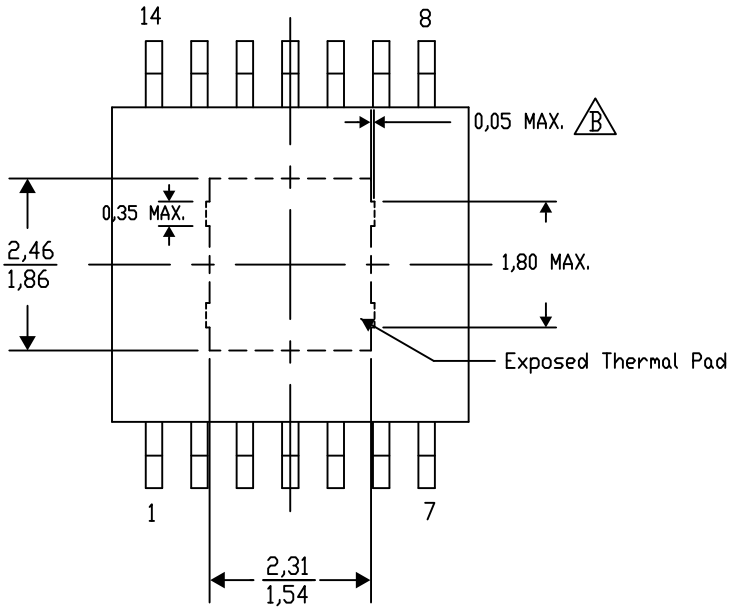
# PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

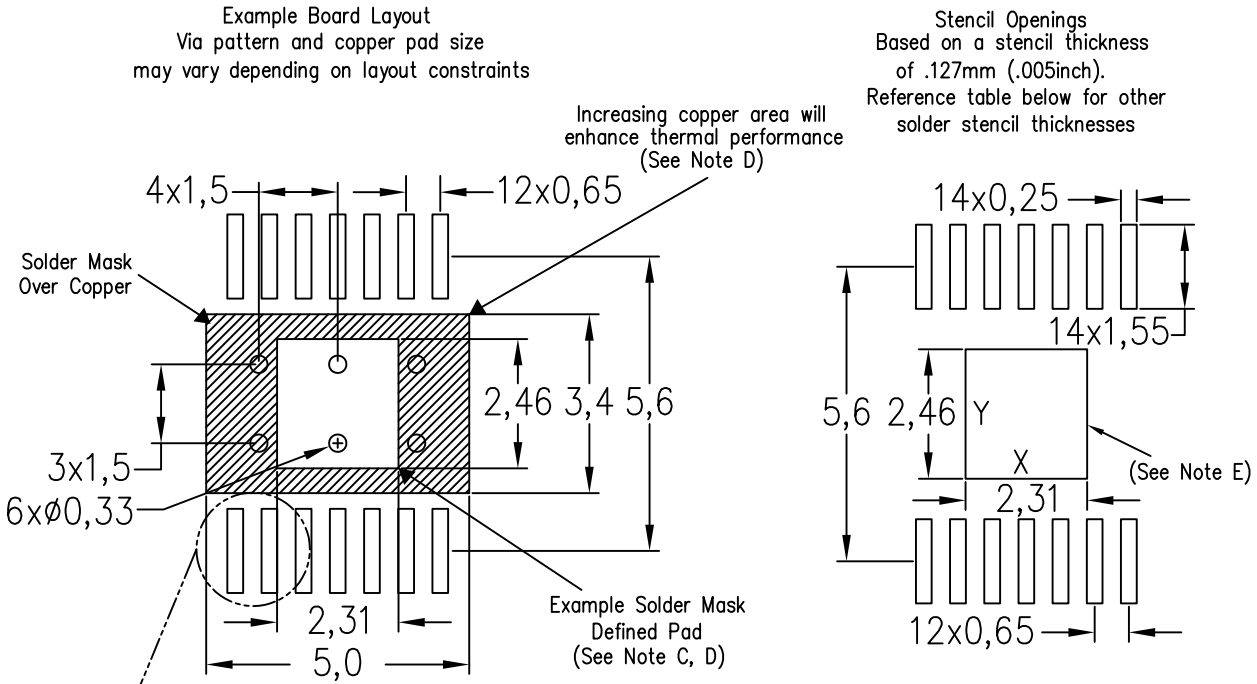
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



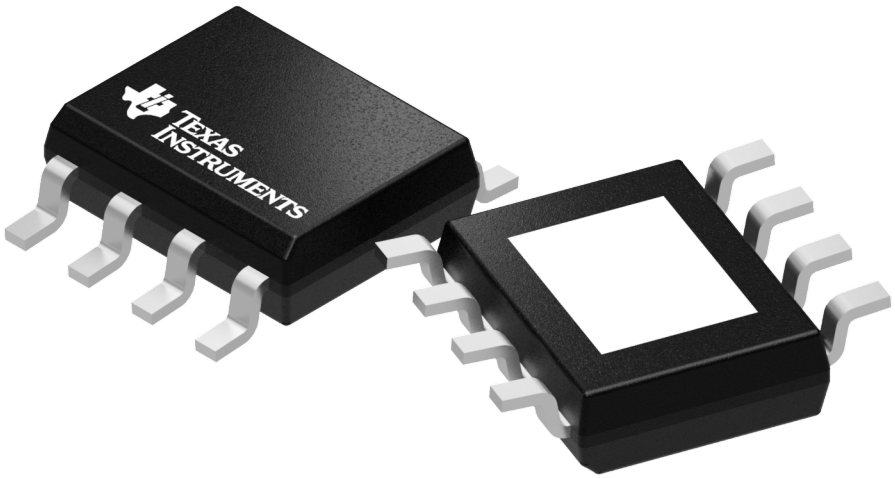

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

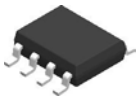
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

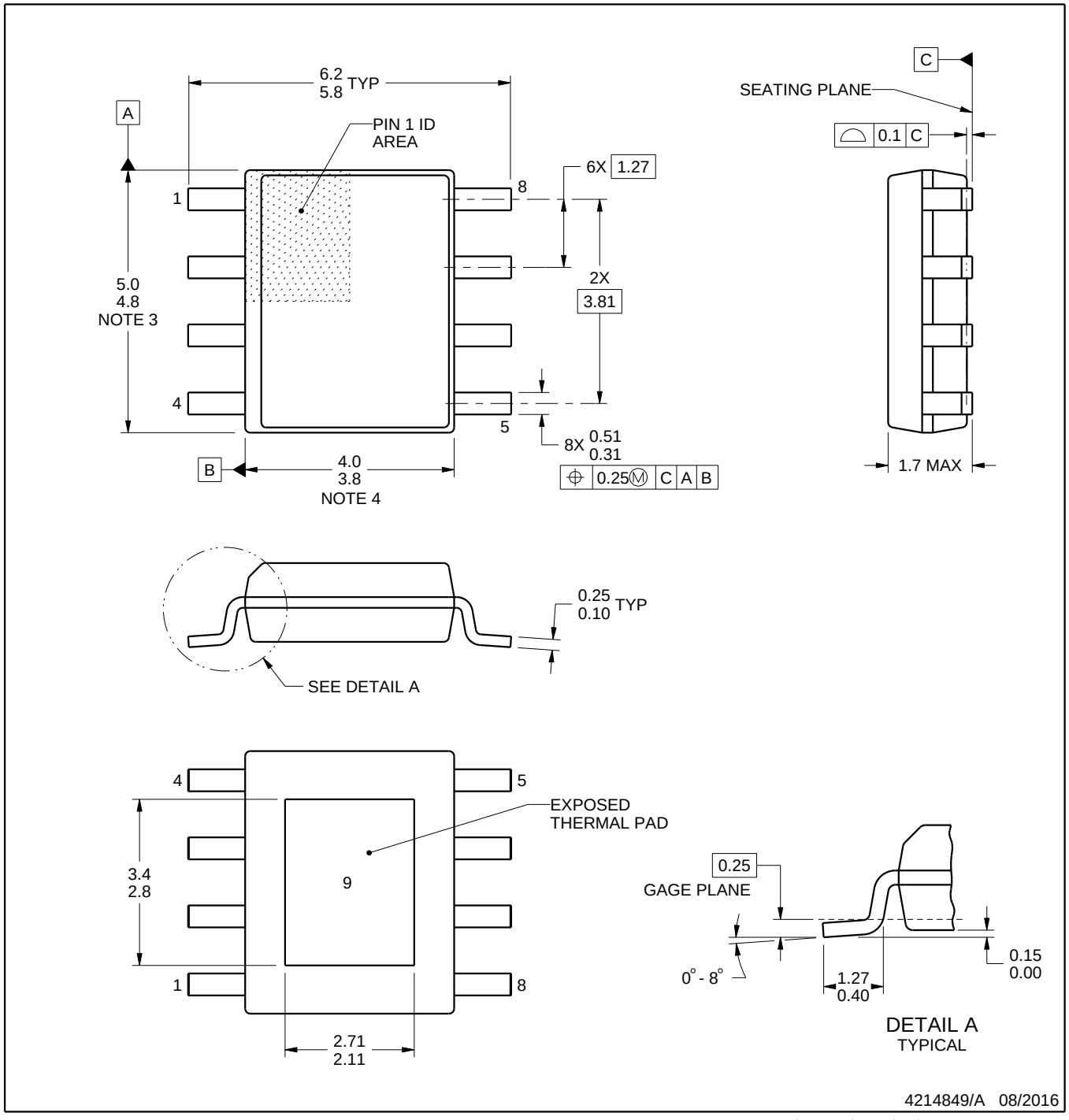


# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

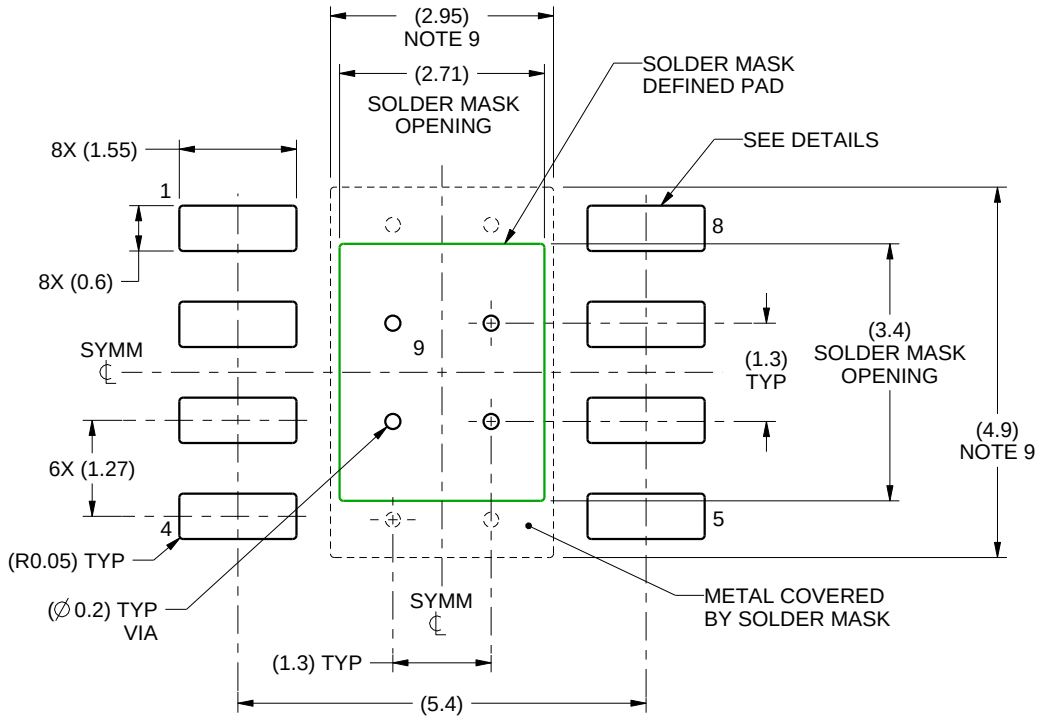
PLASTIC SMALL OUTLINE



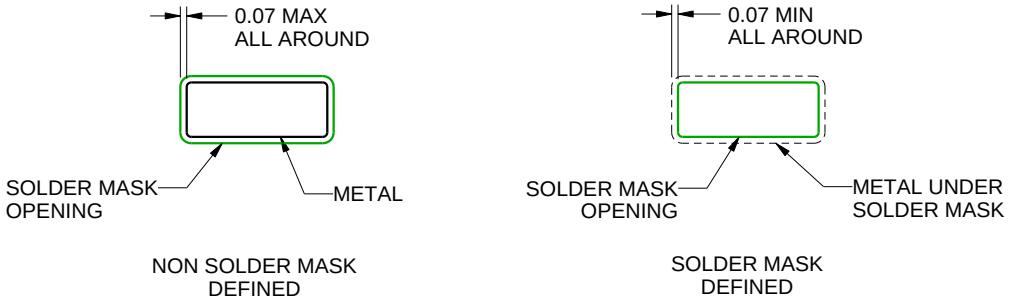

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

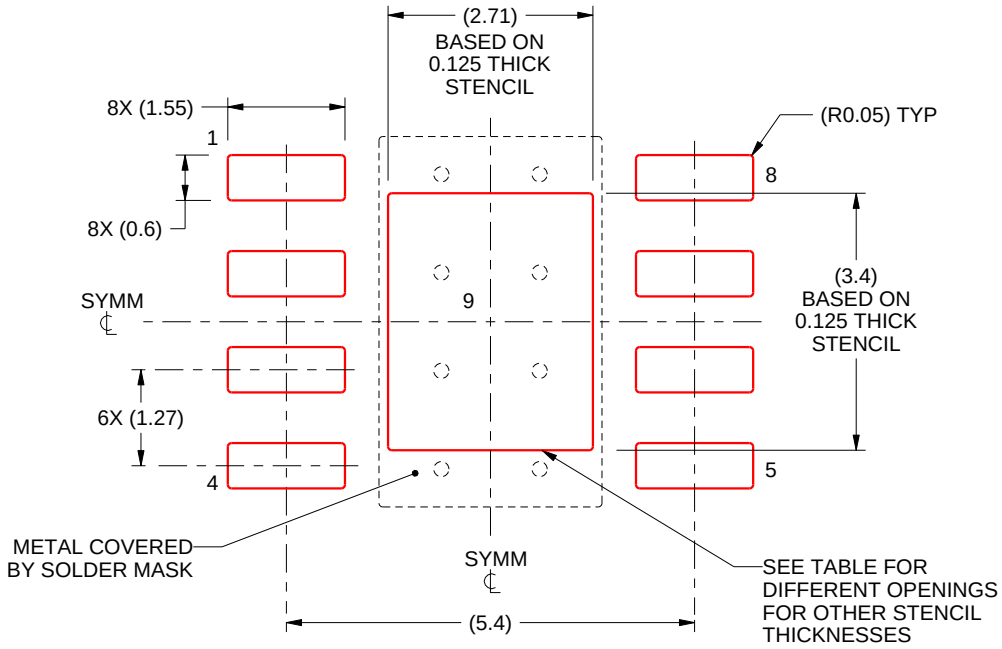
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



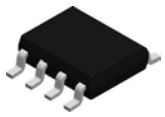

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

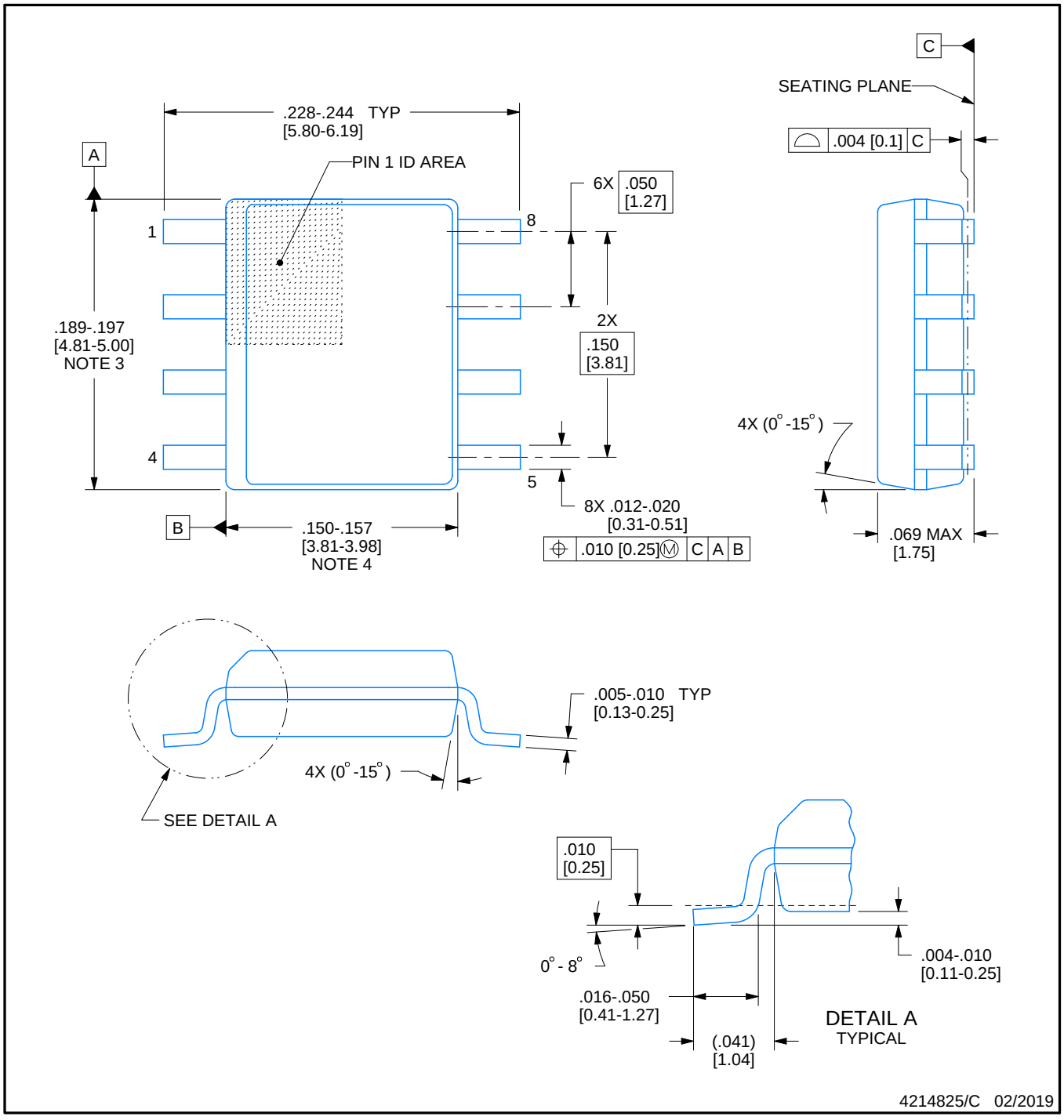


# PACKAGE OUTLINE

## D0008A

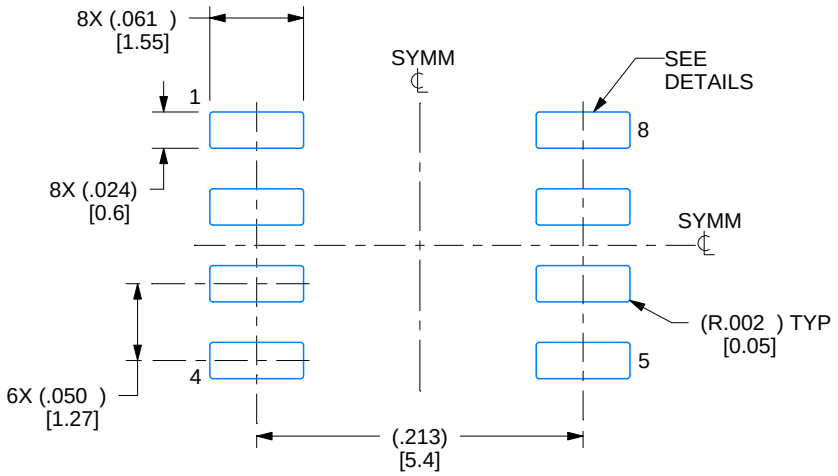
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

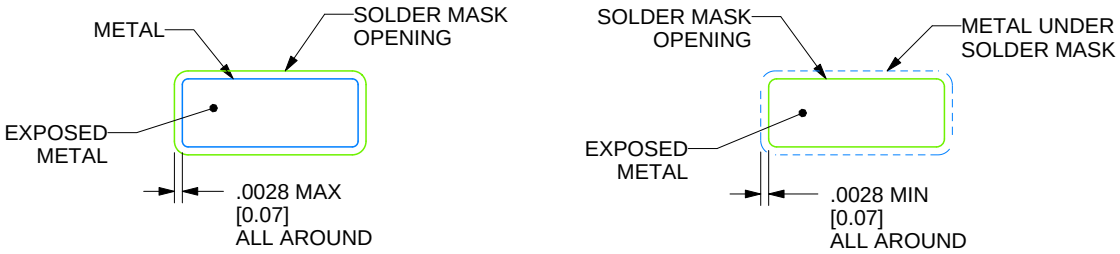



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

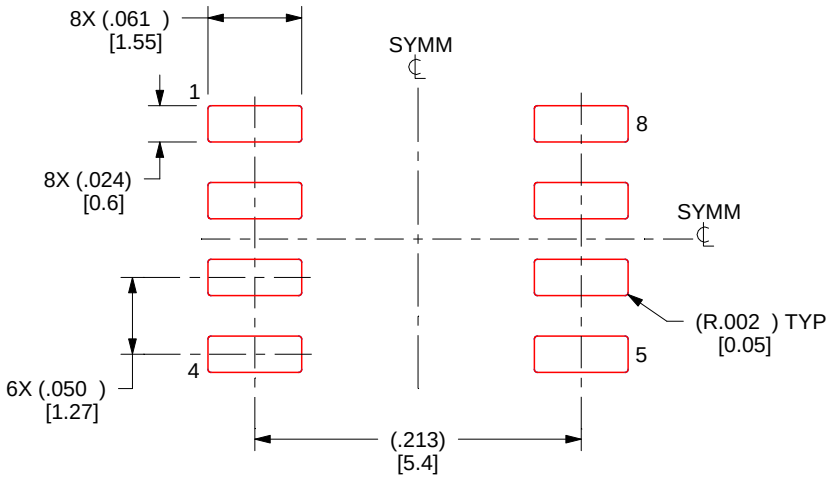
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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