

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

MC14511B

BCD-to-Seven Segment Latch/Decoder/Driver

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (\overline{LT}), blanking (\overline{BI}), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
I	DC Current Drain per Input Pin	10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Operating Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
I_{OHmax}	Maximum Output Drive Current (Source) per Output	25	mA
P_{OHmax}	Maximum Continuous Output Power (Source) per Output (Note 3)	50	mA

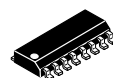
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C to 125°C
3. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$



ON Semiconductor®

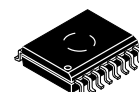
<http://onsemi.com>



SOIC-16
D SUFFIX
CASE 751B



SOEIAJ-16
F SUFFIX
CASE 966

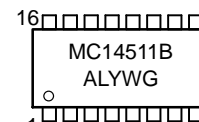


SO-16 WB
DW SUFFIX
CASE 751G

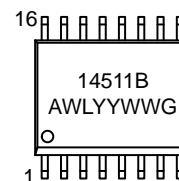
MARKING DIAGRAMS



SOIC-16



SOEIAJ-16



SO-16 WB

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

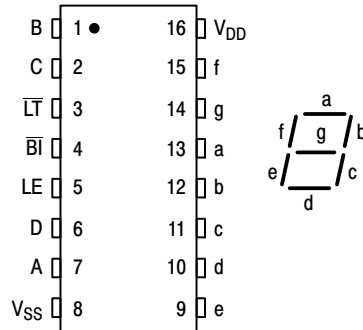
MC14511B

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

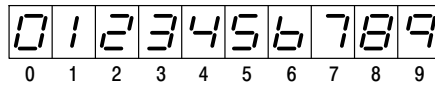
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	1	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

* Depends upon the BCD code previously applied when LE = 0

MC14511B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ (Note 4)	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
			10	–	0.05	–	0	0.05	–	0.05		
			15	–	0.05	–	0	0.05	–	0.05		
	V _{in} = 0 or V _{DD}	"1" Level	V _{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc
				10	9.1	–	9.1	9.58	–	9.1	–	
				15	14.1	–	14.1	14.59	–	14.1	–	
Input Voltage # (V _O = 3.8 or 0.5 Vdc) (V _O = 8.8 or 1.0 Vdc) (V _O = 13.8 or 1.5 Vdc)	"0" Level	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc	
			10	–	3.0	–	4.50	3.0	–	3.0		
			15	–	4.0	–	6.75	4.0	–	4.0		
	(V _O = 0.5 or 3.8 Vdc) (V _O = 1.0 or 8.8 Vdc) (V _O = 1.5 or 13.8 Vdc)	"1" Level	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
				10	7.0	–	7.0	5.50	–	7.0	–	
				15	11	–	11	8.25	–	11	–	
Output Drive Voltage (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA)	Source	V _{OH}	5.0	4.1	–	4.1	4.57	–	4.1	–	Vdc	
				–	–	–	4.24	–	–	–		
				3.9	–	3.9	4.12	–	3.5	–		
				–	–	–	3.94	–	–	–		
				3.4	–	3.4	3.70	–	3.0	–		
				–	–	–	3.54	–	–	–		
			10	9.1	–	9.1	9.58	–	9.1	–	Vdc	
				–	–	–	9.26	–	–	–		
				9.0	–	9.0	9.17	–	8.6	–		
				–	–	–	9.04	–	–	–		
				8.6	–	8.6	8.90	–	8.2	–		
				–	–	–	8.70	–	–	–		
			15	14.1	–	14.1	14.59	–	14.1	–	Vdc	
				–	–	–	14.27	–	–	–		
				14	–	14	14.18	–	13.6	–		
–	–	–		14.07	–	–	–					
13.6	–	13.6		13.95	–	13.2	–					
–	–	–		13.70	–	–	–					
Output Drive Current (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	Sink	I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc	
			10	1.6	–	1.3	2.25	–	0.9	–		
			15	4.2	–	3.4	8.8	–	2.4	–		
			–	–	–	–	–	–	–	–		
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc		
Input Capacitance	C _{in}	–	–	–	–	5.0	7.5	–	–	pF		
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc		
		10	–	10	–	0.010	10	–	300			
		15	–	20	–	0.015	20	–	600			
Total Supply Current (Notes 5 & 6) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}							μAdc		
		10	I _T = (3.8 μA/kHz) f + I _{DD}									
		15	I _T = (5.7 μA/kHz) f + I _{DD}									

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

MC14511B

SWITCHING CHARACTERISTICS (Note 7) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{TLH} = (0.20 \text{ ns/pF}) C_L + 15 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	40 30 25	80 60 50	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	t_{THL}	5.0 10 15	– – –	125 75 65	250 150 130	ns
Data Propagation Delay Time $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	– – – – – – –	640 250 175 720 290 200	1280 500 350 1440 580 400	ns
Blank Propagation Delay Time $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 585 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 187.5 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 142.5 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	– – – – – – –	600 200 150 485 200 160	750 300 220 970 400 320	ns
Lamp Test Propagation Delay Time $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15	– – – – – – –	313 125 90 313 125 90	625 250 180 625 250 180	ns
Setup Time	t_{su}	5.0 10 15	100 40 30	– – –	– – –	ns
Hold Time	t_h	5.0 10 15	60 40 30	– – –	– – –	ns
Latch Enable Pulse Width	t_{WL}	5.0 10 15	520 220 130	260 110 65	– – –	ns

7. The formulas given are for the typical characteristics only.

MC14511B

Input LE low, and Inputs D, $\overline{B1}$ and \overline{LT} high.
 f in respect to a system clock.
 All outputs connected to respective C_L loads.

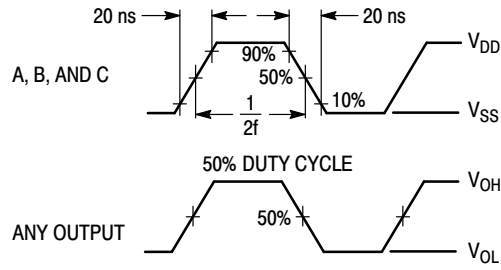
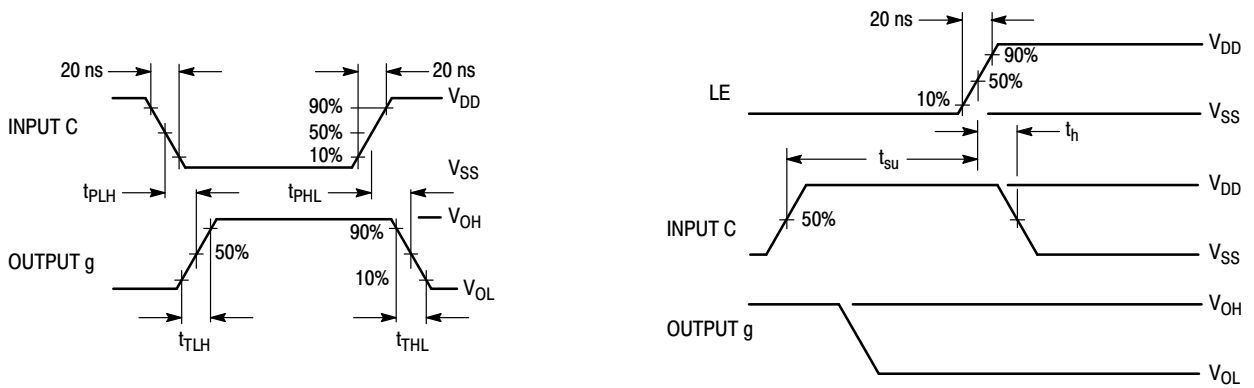
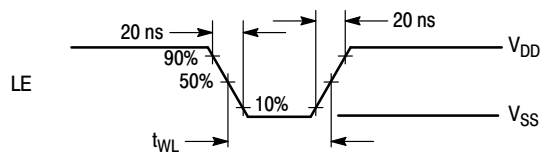


Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{B1}$ and \overline{LT} high.

(b) Input D low, Inputs A, B, $\overline{B1}$ and \overline{LT} high.



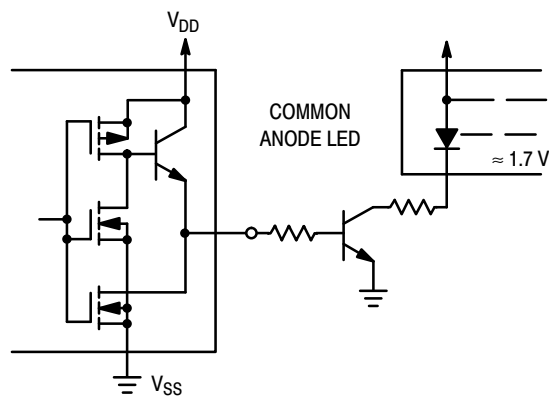
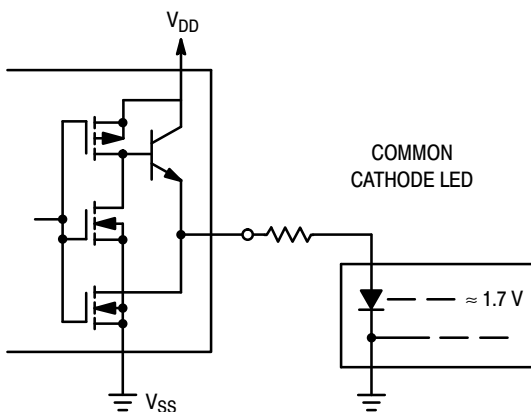
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

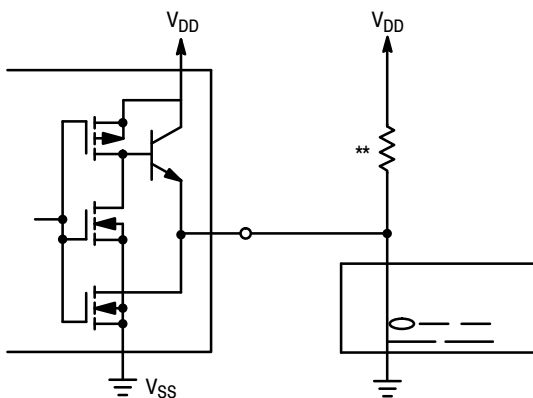
MC14511B

CONNECTIONS TO VARIOUS DISPLAY READOUTS

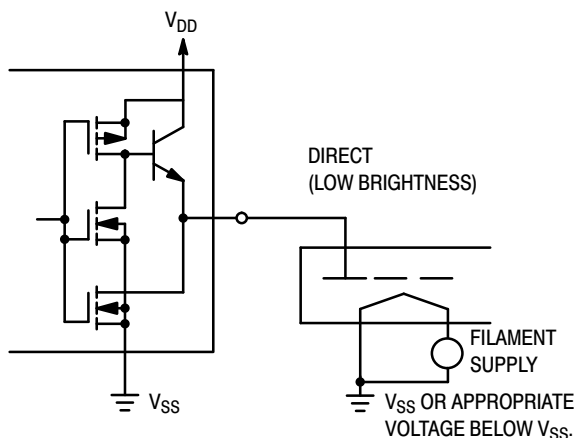
LIGHT EMITTING DIODE (LED) READOUT



INCANDESCENT READOUT

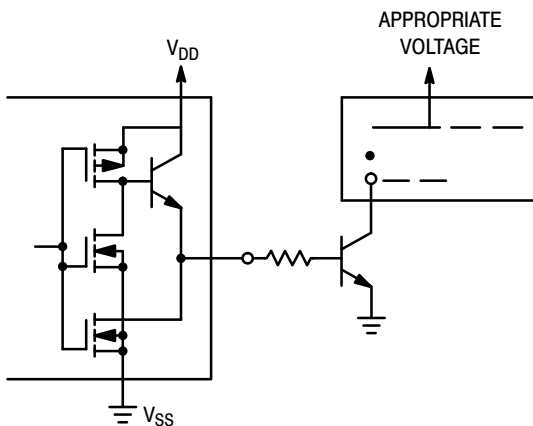


FLUORESCENT READOUT

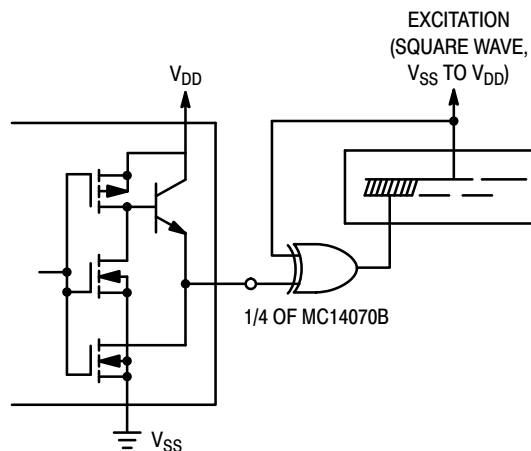


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



LIQUID CRYSTAL (LCD) READOUT



** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct DC drive of LCD's not recommended for life of LCD readouts.

MC14511B

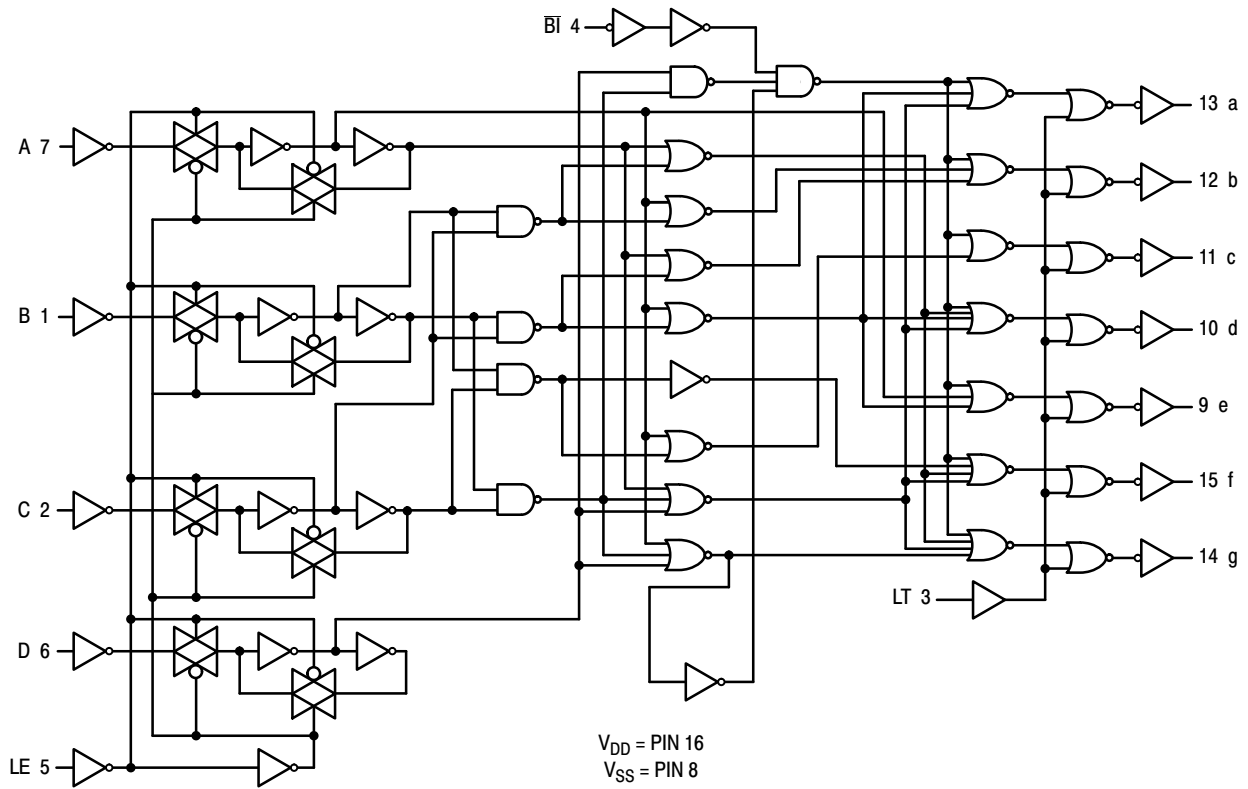


Figure 3. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC14511BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14511BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14511BDWR2G	SO-16 WB (Pb-Free)	1000 / Tape & Reel
NLV14511BDWR2G*	SO-16 WB (Pb-Free)	1000 / Tape & Reel
MC14511BFG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC14511BFELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel

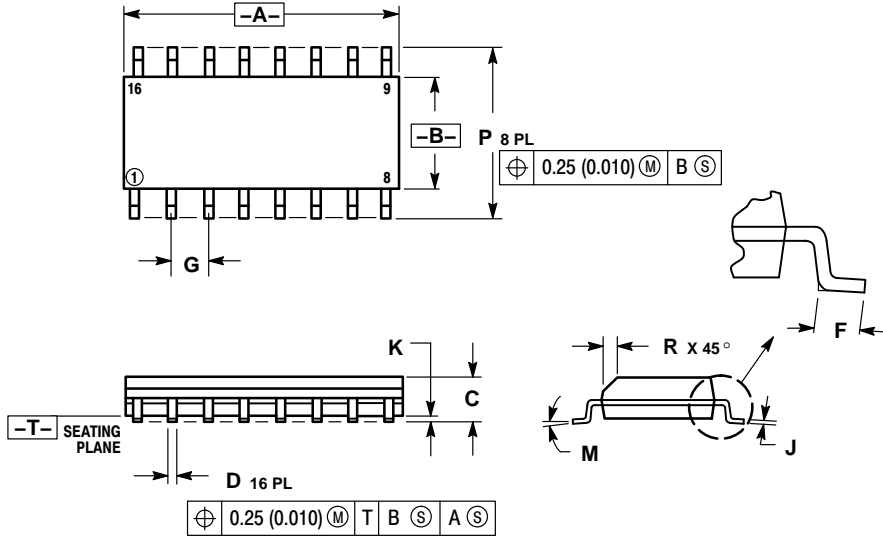
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14511B

PACKAGE DIMENSIONS

SOIC-16
 PLASTIC SOIC PACKAGE
 CASE 751B-05
 ISSUE K

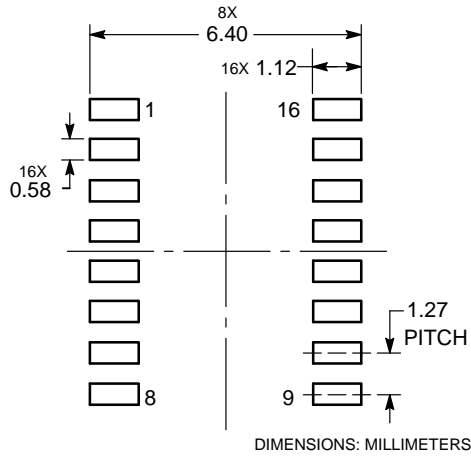


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

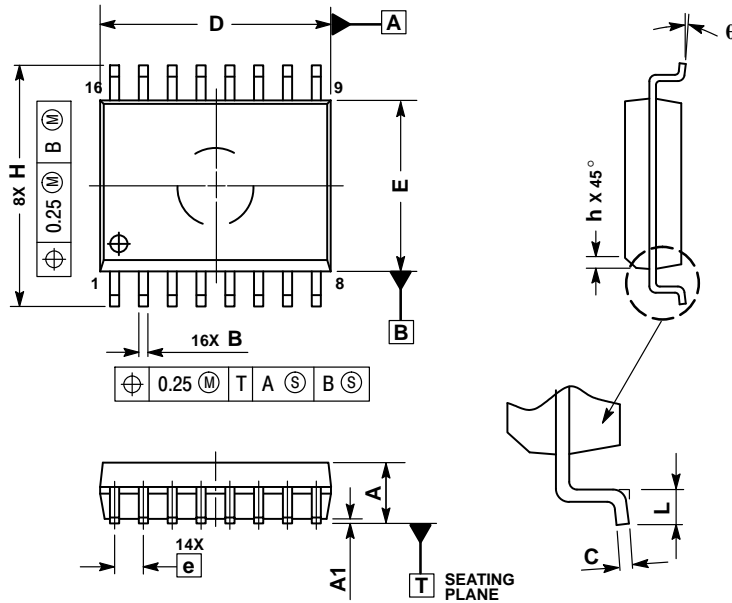
SOLDERING FOOTPRINT



MC14511B

PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751G-03
ISSUE D

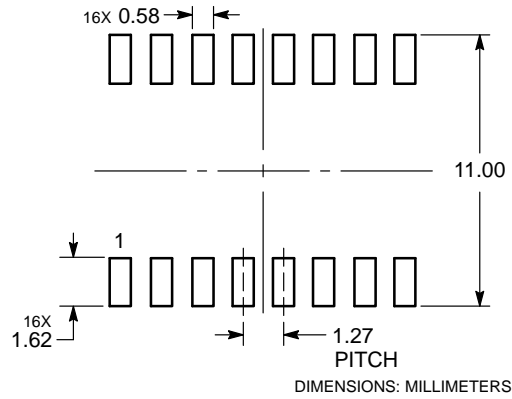


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

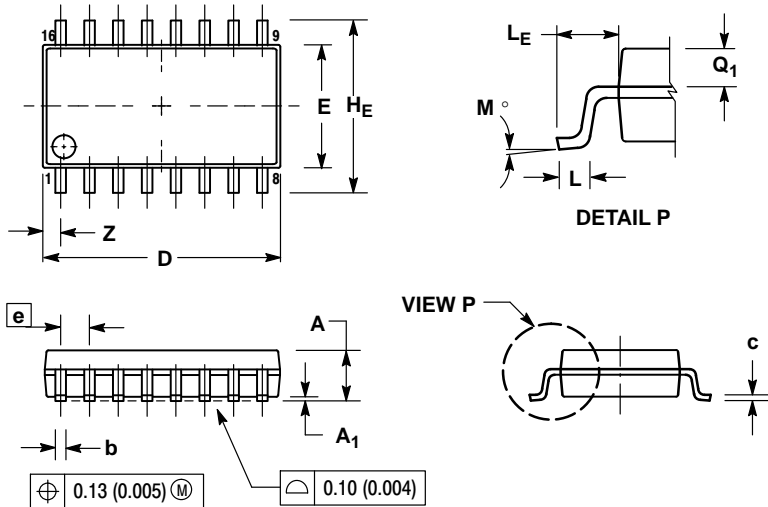
SOLDERING FOOTPRINT



MC14511B

PACKAGE DIMENSIONS


SOEIAJ-16
CASE 966
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative