

# 74LV14

## Hex inverting Schmitt trigger

Rev. 9 — 14 September 2021

Product data sheet

## 1. General description

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The 74LV14 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC14 and 74HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger input. It is capable of transforming slowly-changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the input hysteresis voltage  $V_H$ .

## 2. Features and benefits

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- Wide supply voltage range from 1.0 V to 5.5 V
- CMOS low power dissipation
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce  $< 0.8$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot:  $> 2$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C

## 3. Applications

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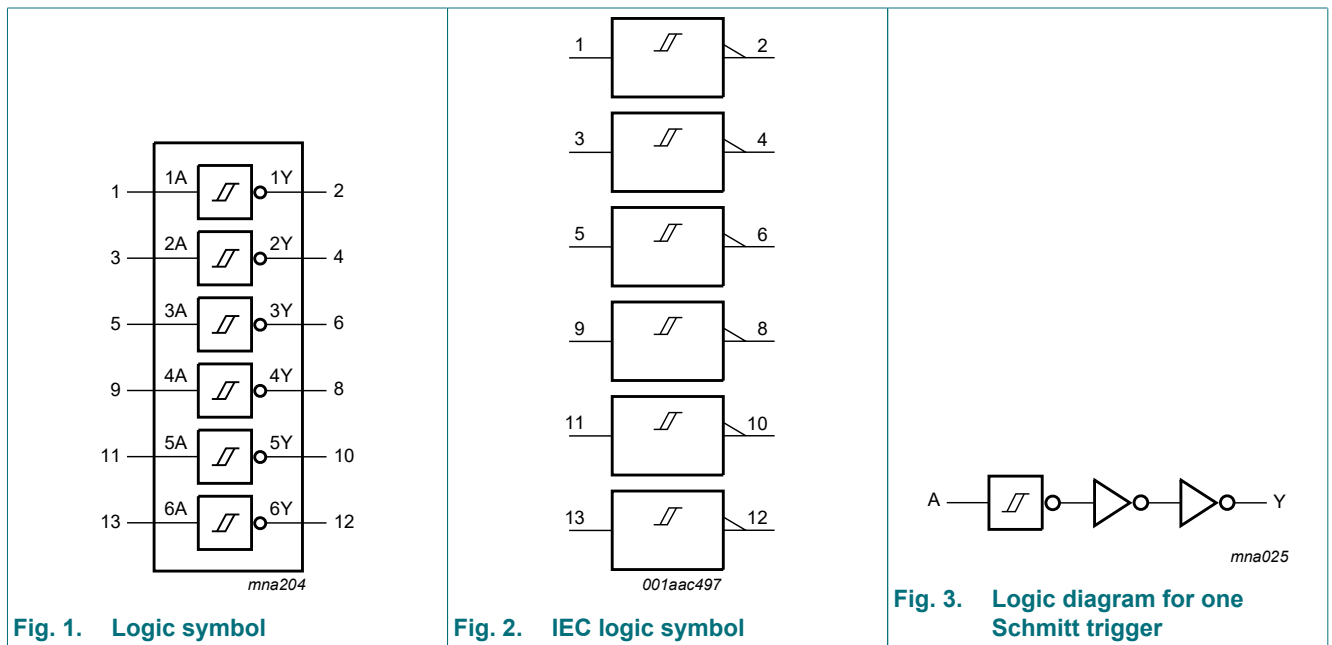
- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

## 4. Ordering information

Table 1. Ordering information

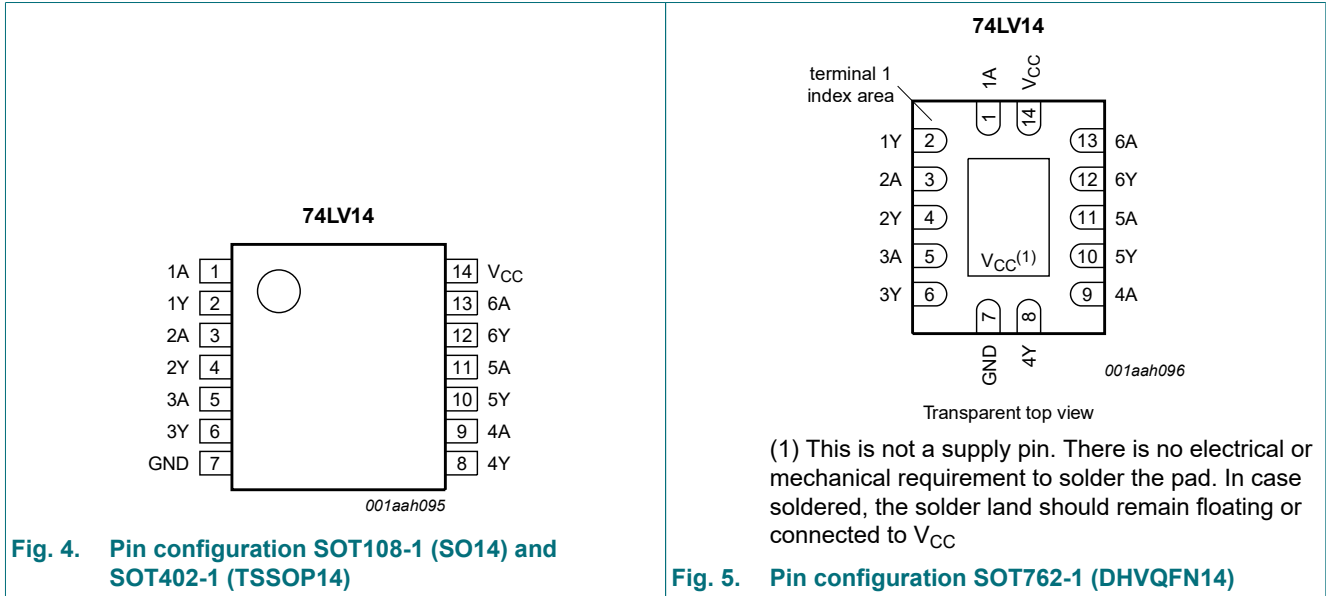
Type number	Package			Version
	Temperature range	Name	Description	
74LV14D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV14PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV14BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nA	Output nY
L	H
H	L

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 50$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
 For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.  
 For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	[1]	1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 10. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; For test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Fig. 6</a> [2]						
		$V_{CC} = 1.2\text{ V}$	-	80	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	27	37	-	48	ns
		$V_{CC} = 2.7\text{ V}$	-	20	28	-	35	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; $C_L = 15\text{ pF}$ [3]	-	13	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	15	22	-	28	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	18	-	23	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f_i = 1\text{ MHz}$ ; $V_I = GND\text{ to }V_{CC}$ [4]	-	15	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$ ).

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

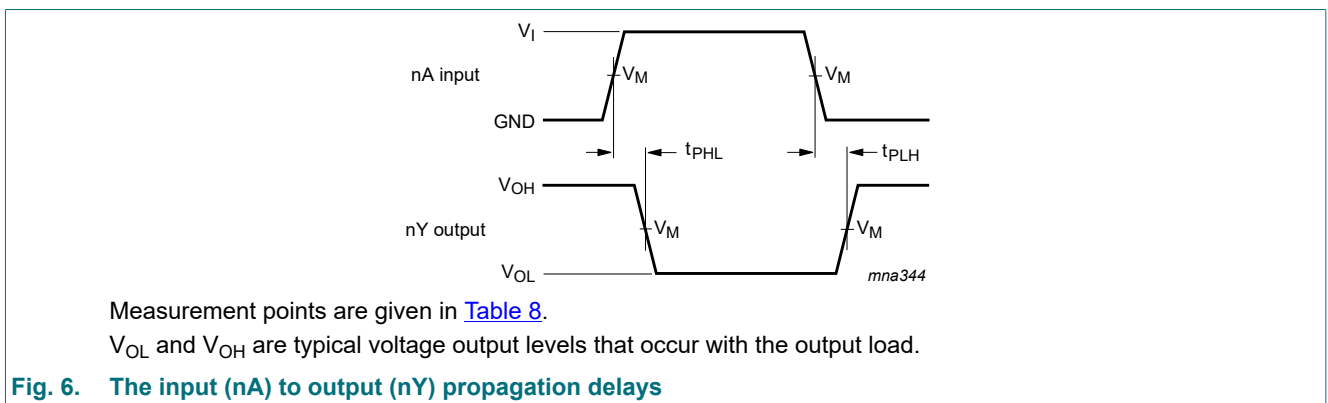
$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$N$  = number of inputs switching

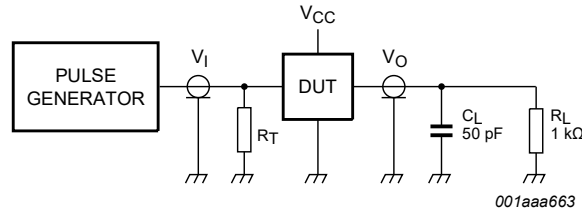
$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

### 11.1. Waveforms and test circuit



**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
$< 2.7\text{ V}$	$0.5V_{CC}$	$0.5V_{CC}$
$2.7\text{ V to }3.6\text{ V}$	$1.5\text{ V}$	$1.5\text{ V}$
$\geq 4.5\text{ V}$	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input	
$V_{CC}$	$V_I$	$t_r, t_f$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns

## 12. Transfer characteristics

**Table 10. Transfer characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see [Fig. 8](#) and [Fig. 9](#).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
$V_{T+}$	positive-going threshold voltage	$V_{CC} = 1.2$ V	-	0.70	-	-	-	V
		$V_{CC} = 2.0$ V	0.8	1.10	1.4	0.8	1.4	V
		$V_{CC} = 2.7$ V	1.0	1.45	2.0	1.0	2.0	V
		$V_{CC} = 3.0$ V	1.2	1.60	2.2	1.2	2.2	V
		$V_{CC} = 3.6$ V	1.5	1.95	2.4	1.5	2.4	V
		$V_{CC} = 4.5$ V	1.7	2.50	3.15	1.7	3.15	V
		$V_{CC} = 5.5$ V	2.1	3.00	3.85	2.1	3.85	V
$V_{T-}$	negative-going threshold voltage	$V_{CC} = 1.2$ V	-	0.34	-	-	-	V
		$V_{CC} = 2.0$ V	0.3	0.65	0.9	0.3	0.9	V
		$V_{CC} = 2.7$ V	0.4	0.90	1.4	0.4	1.4	V
		$V_{CC} = 3.0$ V	0.6	1.05	1.5	0.6	1.5	V
		$V_{CC} = 3.6$ V	0.8	1.30	1.8	0.8	1.8	V
		$V_{CC} = 4.5$ V	0.9	1.60	2.0	0.9	2.0	V
		$V_{CC} = 5.5$ V	1.1	2.00	2.6	1.1	2.6	V

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>H</sub>	hysteresis voltage	V <sub>CC</sub> = 1.2 V	-	0.3	-	-	-	V
		V <sub>CC</sub> = 2.0 V	0.2	0.55	0.8	0.2	0.8	V
		V <sub>CC</sub> = 2.7 V	0.3	0.60	1.1	0.3	1.1	V
		V <sub>CC</sub> = 3.0 V	0.4	0.65	1.2	0.4	1.2	V
		V <sub>CC</sub> = 3.6 V	0.4	0.70	1.2	0.4	1.2	V
		V <sub>CC</sub> = 4.5 V	0.4	0.80	1.4	0.4	1.4	V
		V <sub>CC</sub> = 5.5 V	0.6	1.00	1.5	0.6	1.5	V

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

### 12.1. Waveforms transfer characteristics

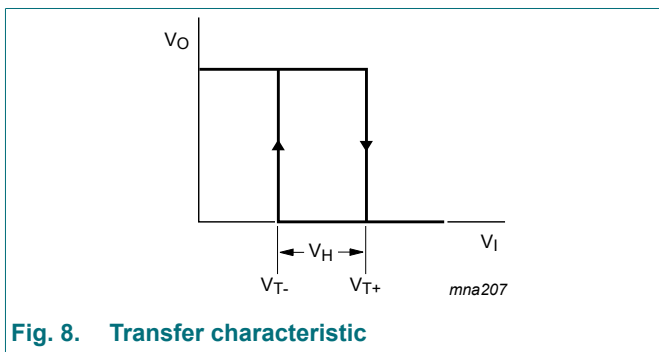


Fig. 8. Transfer characteristic

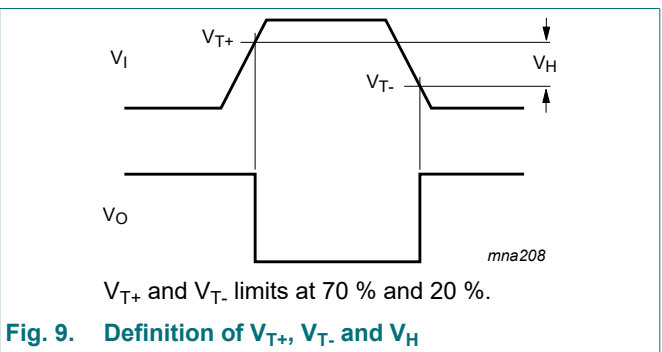


Fig. 9. Definition of V<sub>T+</sub>, V<sub>T-</sub> and V<sub>H</sub>

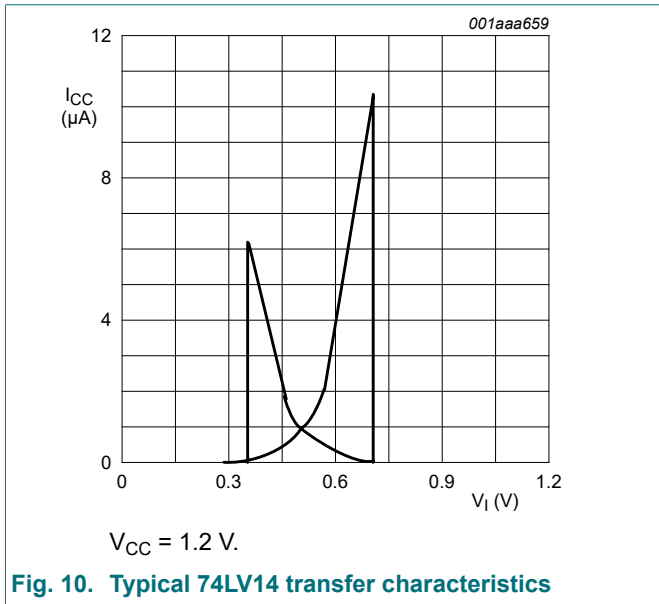


Fig. 10. Typical 74LV14 transfer characteristics

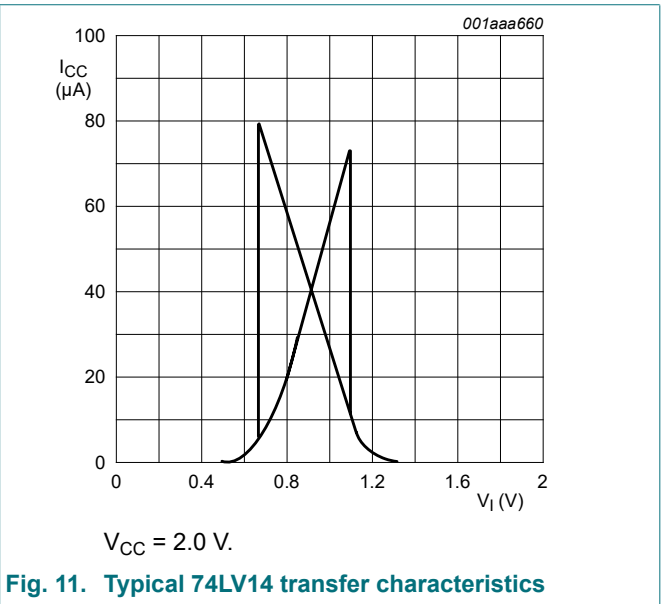
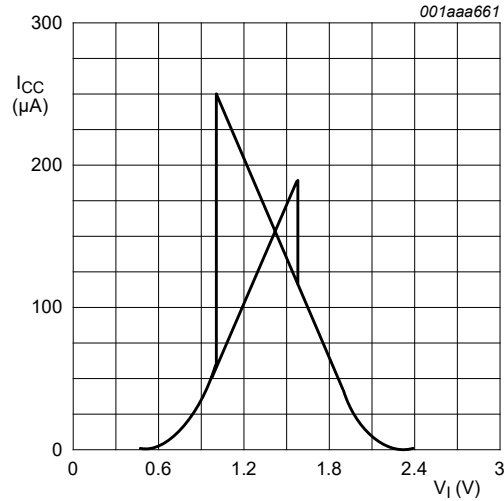


Fig. 11. Typical 74LV14 transfer characteristics





V<sub>CC</sub> = 3.0 V.

Fig. 12. Typical 74LV14 transfer characteristics

### 13. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC} \text{ where:}$$

P<sub>add</sub> = additional power dissipation (µW);

f<sub>i</sub> = input frequency (MHz);

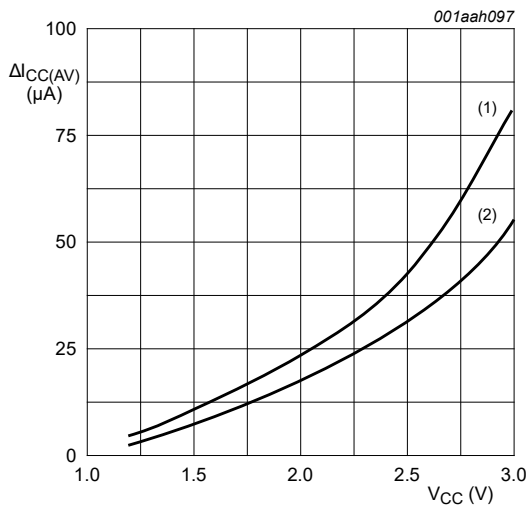
t<sub>r</sub> = rise time (ns); 10 % to 90 %;

t<sub>f</sub> = fall time (ns); 90 % to 10 %;

ΔI<sub>CC(AV)</sub> = average additional supply current (µA).

Average ΔI<sub>CC(AV)</sub> differs with positive or negative input transitions, as shown in Fig. 13.

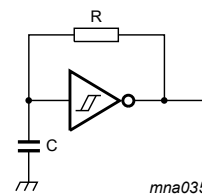
An example of a relaxation circuit using the 74LV14 is shown in Fig. 14.



(1) Positive-going edge.

(2) Negative-going edge.

Fig. 13. Average additional supply current as a function of V<sub>CC</sub>



$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Fig. 14. Relaxation oscillator

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

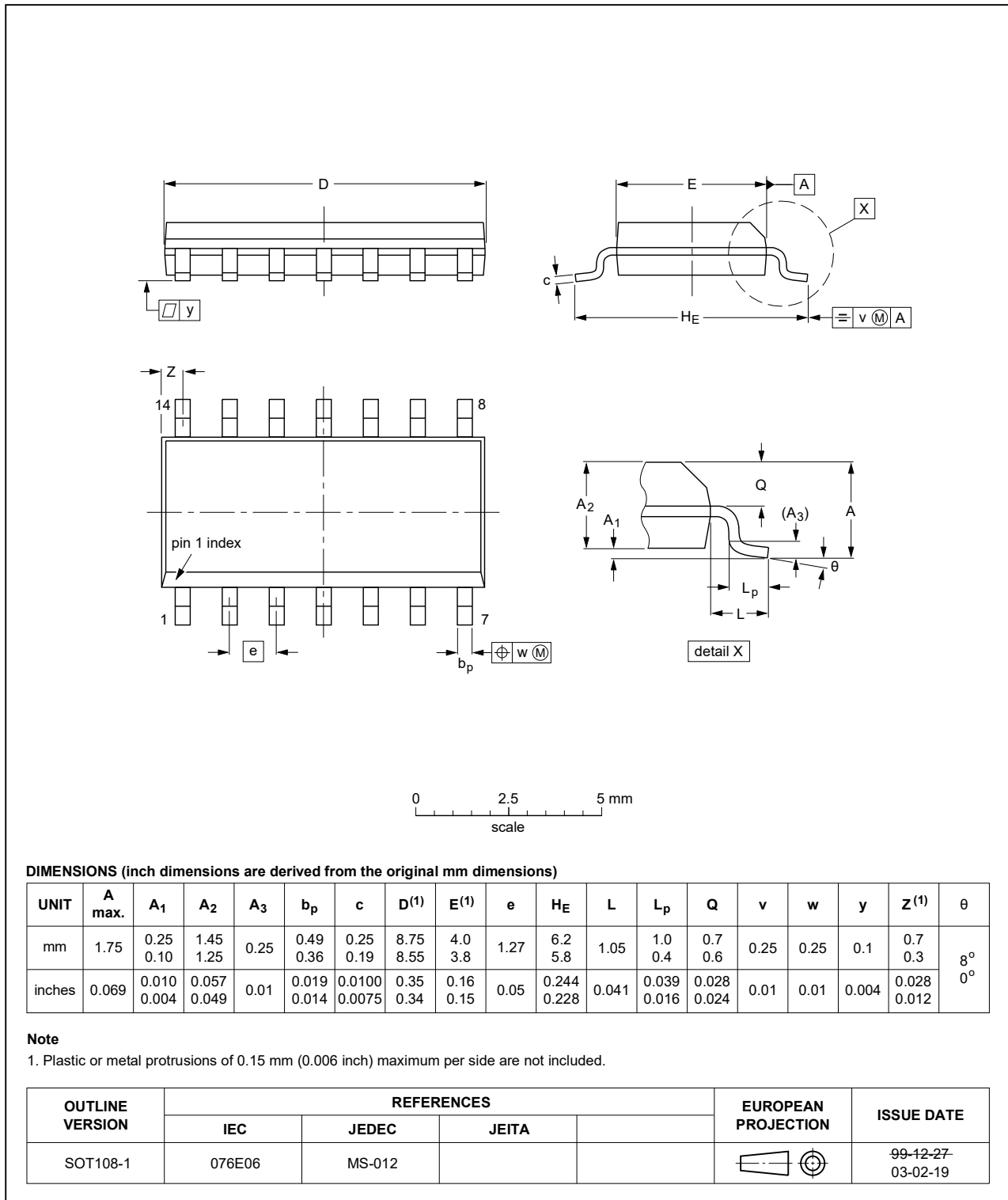


Fig. 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

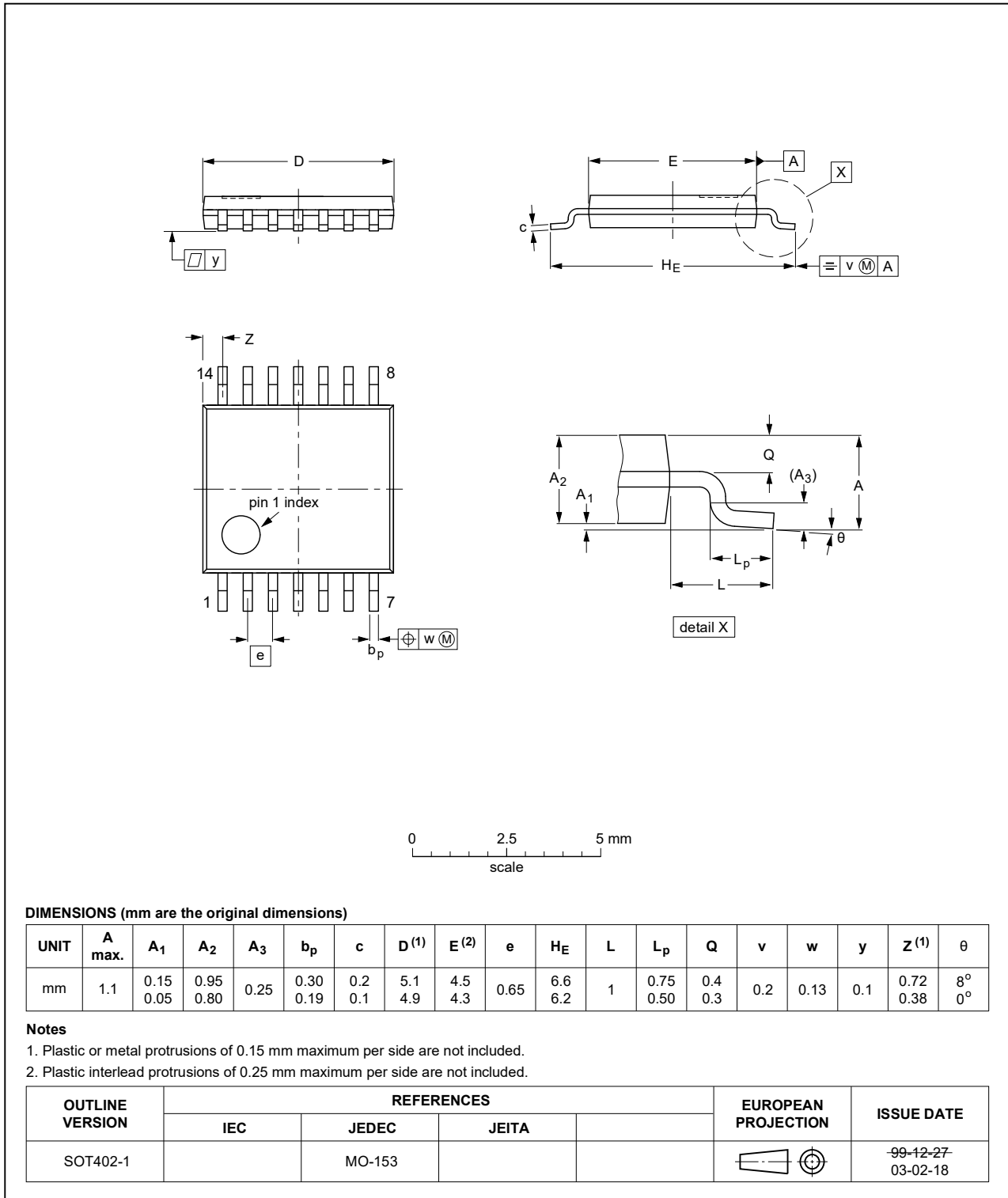


Fig. 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

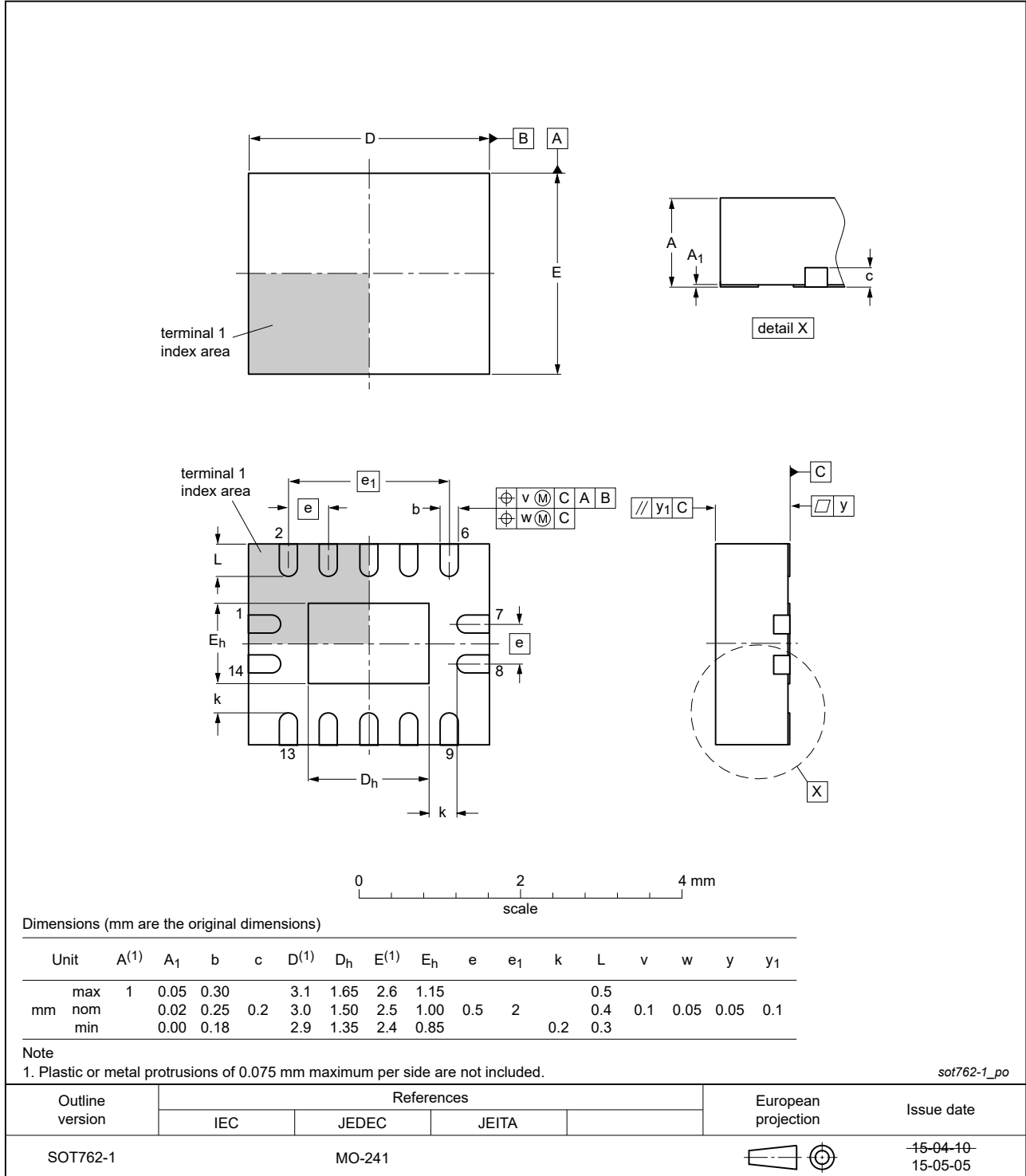


Fig. 17. Package outline SOT762-1 (DHVQFN14)

## 15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV14 v.9	20210914	Product data sheet	-	74LV14 v.8
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV14DB (SOT337-1/SSOP14) removed.</li> <li><a href="#">Section 2</a> updated.</li> </ul>			
74LV14 v.8	20210304	Product data sheet	-	74LV14 v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LV14 v.7	20151209	Product data sheet	-	74LV14 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV14N (SOT27-1) removed.</li> </ul>			
74LV14 v.6	20111212	Product data sheet	-	74LV14 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74LV14 v.5	20110105	Product data sheet	-	74LV14 v.4
74LV14 v.4	20090702	Product data sheet	-	74LV14 v.3
74LV14 v.3	20071220	Product data sheet	-	74LV14 v.2
74LV14 v.2	19980420	Product specification	-	74LV14 v.1
74LV14 v.1	19970203	Product specification	-	-

## 17. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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