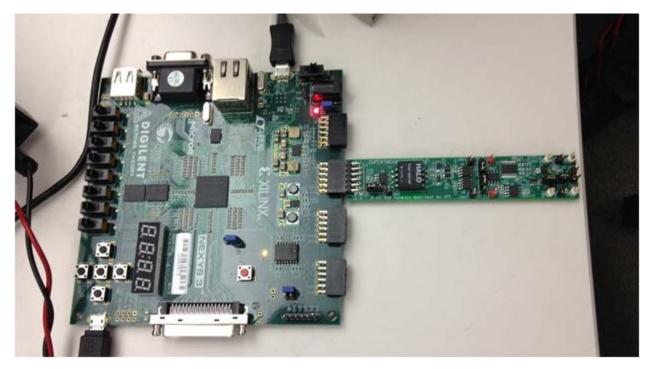


# Santa Fe (MAXREFDES5#) Nexys 3 Quick Start Guide

Rev 1; 2/14



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## **1. Required Equipment**

- PC with Windows® OS with Xilinx® ISE®/SDK version 13.4 or later and two USB ports
- License for Xilinx EDK/SDK version 13.4 or later
- Santa Fe (MAXREFDES5#) board
- Nexys<sup>™</sup>3 development kit
- Industrial sensor or signal source

## 2. Overview

Below is a high-level overview of the steps required to quickly get the Santa Fe design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. The Santa Fe (MAXREFDES5#) subsystem reference design will be referred to as Santa Fe throughout this document.

- 1) Connect the Santa Fe board to the JB1 port of a Nexys 3 development kit as shown in <u>Figure 1</u>. Ensure the connector is aligned as shown in <u>Figure 2</u>.
- 2) Download the latest RD5V01\_00.ZIP file located at the Santa Fe page.
- 3) Extract the **RD5V01\_00.ZIP** file to a directory on your PC.
- 4) Open the Xilinx SDK.
- 5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
- 6) Open a terminal program to communicate with FPGA board.
- Use Xilinx SDK to download and run the executable file (.ELF) on the MicroBlaze<sup>™</sup>.

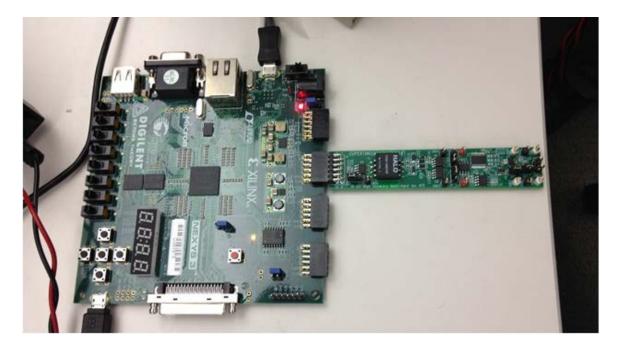


Figure 1. Santa Fe Board Connected to Nexys 3 Development Kit

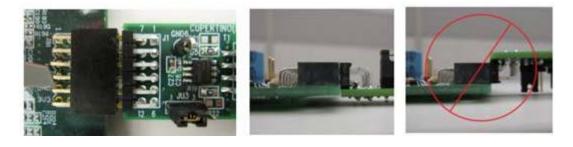
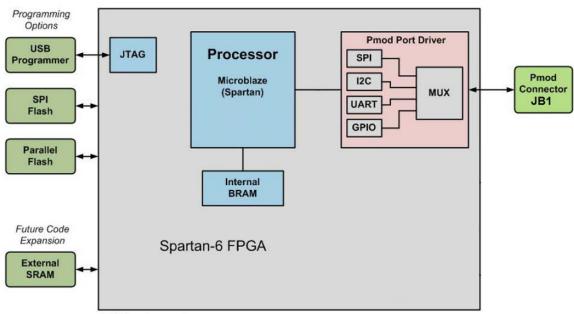


Figure 2. Pmod<sup>™</sup> Connector Alignment

## 3. Included Files

The top level of the hardware design is a Xilinx ISE Project Navigator Project (.XISE) for Xilinx ISE version 13.4. The Verilog-based HDL design instantiates the MicroBlaze core, the support hardware required to run the MicroBlaze, and the peripherals that interface to the Pmod ports. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Santa Fe subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.



\* SPI only used.

#### Figure 3. Block Diagram of FPGA Hardware Design

#### 4. Procedure

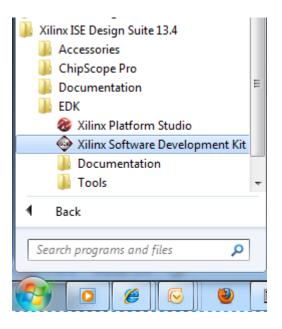
- 1. Connect the Santa Fe board to the JB1 port of a Nexys 3 development kit as shown in <u>Figure 1</u>. Power up the Nexys 3 development kit. The Santa Fe board is completely powered from the Nexys 3 development kit and no external power is required.
- Download the latest RD5V01\_00.ZIP file at <u>www.maximintegrated.com/AN5561</u>. All files available for download are available at the bottom of the page.
- Extract the RD5V01\_00.ZIP file to a directory on your PC. The location is arbitrary but the path prior to where you extract the .ZIP file must not exceed 82 characters due to the Windows 250-character total path limitation. For example, this 90-character preceding path would be an example of a path that would be too long:

# C:\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\RD5V01\_00.ZIP (This path is too long.)

In addition, the Xilinx tools require the path to not contain any spaces.

# C:\Do Not Use Spaces In The Path\RD5V01\_00.ZIP (This path has spaces.)

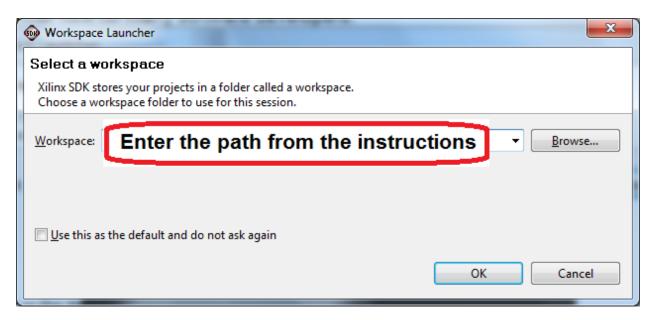
For the purposes of this document, it will be **C:\designs\maxim\RD5V01\_00\**. See <u>Appendix A: Project Structure and Key Filenames</u> in this document for the project structure and key filenames. 4. Open the Xilinx Software Development Kit (SDK) from the Windows Start menu.



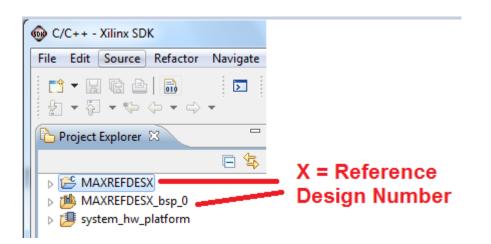
5. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

C:\designs\maxim\RD5V01\_00\RD5\_NEXYS3\_V01\_00\Design\_Files\sdkWorkspace

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse<sup>™</sup>-based IDE, so it will be a familiar flow for many software developers.



6. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.



7. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

C:\designs\maxim\RD5V01\_00\RD5\_NEXYS3\_V01\_00\Design\_Files\sdkWorkspace

and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

Click **Finish** to import the projects.

Import
Select Create new projects from an archive file or directory.
Select an import source:
type filter text
<ul> <li>General</li> <li>Archive File</li> <li>Existing Projects into Workspace</li> <li>File System</li> <li>Preferences</li> <li>C/C++</li> <li>Remote Systems</li> <li>Run/Debug</li> <li>Team</li> </ul>
A Section Cancel     A

8. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).



The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected as well as an FPGA BMM (.BMM) file. Be sure to select the .BIT file and the .BMM by using the paths below.

#### Bitstream:

C:\designs\maxim\RD5V01\_00\RD5\_NEXYS3\_V01\_00\Design\_Files\ sdkWorkspace\system\_hw\_platform\system.bit

BMM File:

C:\designs\maxim\RD5V01\_00\RD5\_NEXYS3\_V01\_00\Design\_Files\ sdkWorkspace\system\_hw\_platform\system\_bd.bmm Additionally, make sure **bootloop** is selected as shown, then press **Program**.

Program FPGA				×					
Program FPGA Specify the bitstre	am and the ELF files that reside in BRAM m	nemory							
Hardware Specification: path filled in automatically									
Bitstream: BMM File:	nter the path from the	instructions		Browse Browse					
Processor	ELF File to Initialize in Block RAM								
microblaze_0	bootloop	-							
?			Program	Cancel					

It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

9. Set up the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

The Nexys 3 utilizes the FTDI FT232 USB-UART bridge IC, so you need to install FTDI's virtual COM port (VCP) driver for the FT232 device family. Make sure to choose the driver that supports a **Virtual Com Port**, also known as VCP. These can be obtained from the FTDI website (www.ftdichip.com).

Once installed, Windows assigns a previously unused COM port. Use the Windows **Control Panel** | **System** | **Device Manager** to determine the COM port number. (It will be named **USB Serial Port**). Make a note of which COM port this is. That information is needed in the next step.

Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (<u>http://ttssh2.sourceforge.jp/</u>). Whatever terminal program you

choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

bits per second: 460,800;

data bits: 8;

parity: **none**;

stop bits: 1;

flow control: **none**.

10. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the MicroBlaze using the following steps.

Right-click the mouse while the **MAXREFDES5 C** project is selected, choose the **Run As** menu, and then **Run Configurations...** menu as shown below.

Project Explo		New Go Into	+		Mał	
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	×	Delete	Delete			REFDESX C project
		Move				
		Rename	F2		Selec	t Run As
	2	Import				
	4	Export			Run C	Configurations
		Build Project				
		Clean Project				
	8	Refresh	F5			
		Close Project				
		Close Unrelated Projects				
		Build Configurations	×			
		Make Targets	+			
		Index	+			
		Show in Remote Systems view				
		Convert To		📮 Console 🛛 🔲 Properti	ior 🗐 1	
	0	Format Project With Jindent				
	С	Run As	×	1 Launch on Hardware		
		Debug As	۱.	2 Local C/C++ Application		
		Profile As	•	3 Remote ARM Linux Appli	cation	•
		Team	×	Run Configurations		

Next, double-click the mouse on the Xilinx C/C++ ELF menu.

🐵 Run Configurations	CARLES DO	a second	×
Create, manage, and run confi	gurations		
Image: Second system       Image: Second system	Configure launch settings from this dialog: Press the 'New' button to create a configuration of the selected type. Press the 'Duplicate' button to copy the selected configuration. Press the 'Delete' button to remove the selected configuration. Press the 'Filter' button to configure filtering options. Edit or view an existing configuration by selecting it. Configure launch perspective settings from the <u>Perspectives</u> preference page.		
?	[	Run	Close

Next, press the **Search Project** button.

💀 Run Configurations		🗙 📼 👘 Sanat (Sanat (Sanat (Sanat )
Create, manage, and run confi Ø Program not specified	gurations	
Yee filter text         C C/C++ Application         C C/C++ Remote Application         Launch Group         Remote ARM Linux Applicati         Xilinx C/C++ ELF         Xilinx C/C++ ELF         XXREFDESX Debug	C/C++ Application: Project: MAXREFDESX Build (if required) before launching Build configuration: Debug © Enable auto build © Use workspace settings	y STDIO Connection y STDIO Connection y Profile Options Search Project Browse Browse © Disable auto build Configure Workspace Settings turning
Filter matched 6 of 6 items	Connect process input & output to a	Apply Reyert

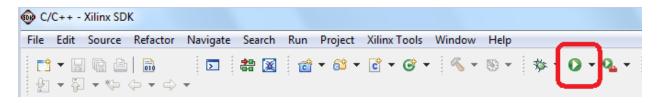
Double-click on the **MAXREFDES5.elf** binary.

Program Selection
Choose a <u>p</u> rogram to run:
Binaries:
MAXREFDESX.elf
Qualifier:
microblazele - /MAXREFDESX/Debug/MAXREFDESX.elf microblazele - /MAXREFDESX/Release/MAXREFDESX.el
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OK Cancel

💀 Run Configurations		"forest " to gate, multipl" mult	<b>—</b> X—
Create, manage, and run confi	gurations		
Yee       Yee         type filter text         C       C/C++ Application         C       C/C++ Remote Application         Launch Group       Remote ARM Linux Applicati         Xilinx C/C++ ELF       Xilinx C/C++ ELF         XXXREFDESX Debug       XXXREFDESX Debug	Name: MAXREFDESX Debug Main & Device Initialization & C/C++ Application: Debug/MAXREFDESX.elf Project: MAXREFDESX Build (if required) before launching Build configuration: Debug © Enable auto build © Use workspace settings Connect process input & output to a	Oisable auto build Configure Workspace Se	Search Project Browse Browse
<ul> <li>✓ Ⅲ →</li> <li>Filter matched 6 of 6 items</li> </ul>			Apply Reyert
?			Run Close

Verify the application is selected and press the **Run** button.

Once the Debug/MAXREFDES5 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.



At this point, the application is running on the MicroBlaze and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select channel AINO, press 0.

ile	OM8:460800b <u>E</u> dit <u>S</u> etup			anjiCode	Resi <u>z</u> e	<u>H</u> elp				
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# 5. Code Documentation

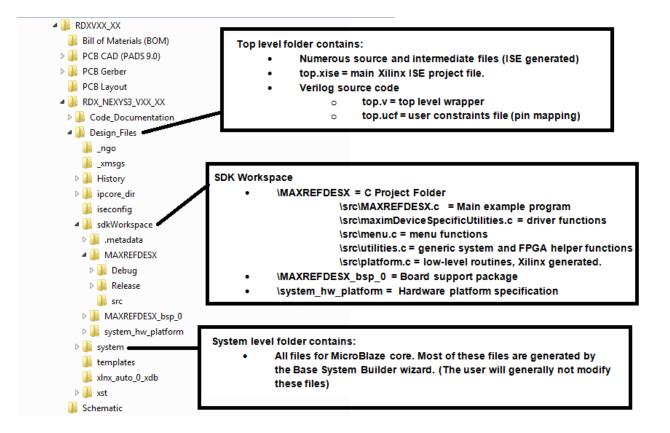
Code documentation can be found at: C:\...\RD5V01\_00\RD5\_NEXYS3\_V01\_00\Code\_Documentation\

RDXVXX_XX   RDX_NEXYS3_VXX_XX   Code_Documentation								
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1	🕖 MainPage.html	12/6/2012 3:42 PM	HTML Document	1 KB				
	AAXREFDESX_Code_Documentation.pdf	12/13/2012 2:56 PM	Adobe Acrobat D	157 KB				

To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES5\_Code\_Documentation.pdf** file.





## 7. Trademarks

Eclipse is a trademark of Eclipse Foundation, Inc.

MicroBlaze is a trademark of Xilinx, Inc.

Nexys is a trademark of Digilent, Inc.

Pmod is a trademark of Digilent, Inc.

Spartan is a registered trademark of Xilinx, Inc.

Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.

Xilinx is a registered trademark and registered service mark of Xilinx, Inc.

8.	Revision	History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	
1	2/14	Replaced the board name "Cupertino" with "Santa Fe"	All