PUSB3FA2

ESD protection for ultra high-speed interfaces

5 April 2018 **Product data sheet**

1. General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB 3.1 at 10 Gbps, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes a high-level ESD protection diode structure protecting sensitive transmitters and receivers for ultra high-speed signal lines. The device is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.2 pF maximum. These diodes utilize a snapback structure in order to provide protection to downstream components from ESD voltages up to ±15 kV contact exceeding IEC 61000-4-2, level 4.

2. Features and benefits

- System-level ESD protection for USB 2.0 and SuperSpeed USB 3.1 at 10 Gbps, HDMI, DisplayPort, eSATA and LVDS
- Line capacitance of only 0.2 pF maximum for each channel
- Outstanding system protection: extremely deep snapback combined with dynamic resistance of only 0.4 Ω
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±15 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Design-friendly ‘pass-through’ signal routing

3. Applications

The device is designed for high-speed receiver and transmitter port protection:

- Smartphones, tablet computers, Mobile Internet Devices (MID) and portable devices
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

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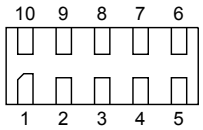
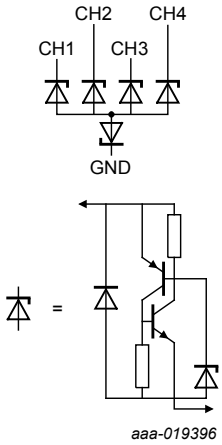
4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 Transparent top view **DFN2510A-10 (SOT1176-1)**	
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	no connection		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3FA2	DFN2510A-10	plastic, extremely thin small outline package; 10 terminals; 0.5 mm pitch; 2.5 mm x 1 mm x 0.5 mm body	SOT1176-1

6. Marking

Table 3. Marking codes

Type number	Marking code
PUSB3FA2	AB

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			-1.5	1.5	V
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	7	A
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; contact discharge	[2]	-15	15	kV
		IEC 61000-4-2, level 4; air discharge	[2]	-15	15	kV
T_{stg}	storage temperature			-55	125	°C
T_{amb}	ambient temperature			-40	85	°C

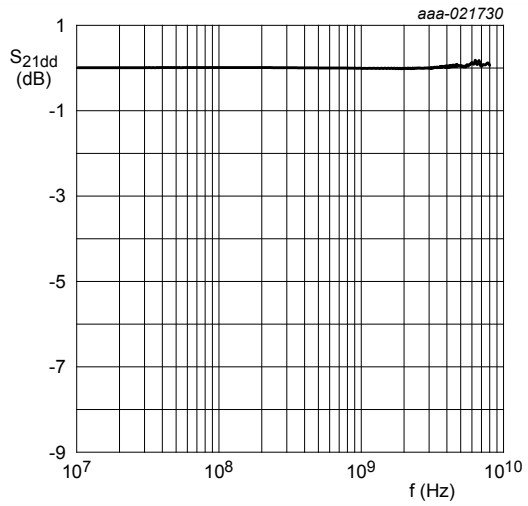
[1] In positive and negative direction.
[2] All pins to ground.

8. Characteristics

Table 5. Characteristics

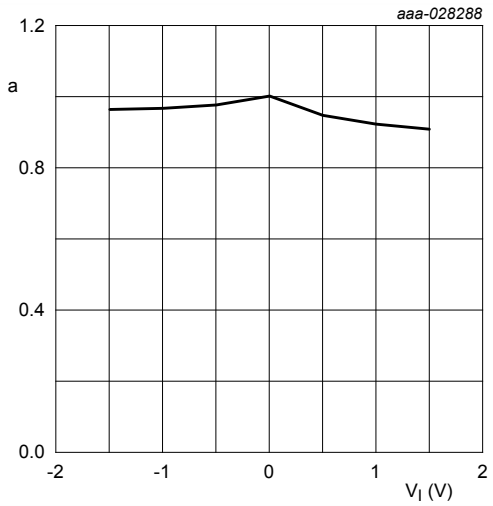
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA; T_{amb} = 25 °C		5.5	9	-	V
I_{LR}	reverse leakage current	per channel; V_I = 1.5 V; T_{amb} = 25 °C		-	1	100	nA
C_{line}	line capacitance	f = 1 MHz; V_I = 1.5 V; T_{amb} = 25 °C	[1]	-	0.17	0.2	pF
r_{dyn}	dynamic resistance	TLP; positive transient; T_{amb} = 25 °C	[2]	-	0.4	-	Ω
		TLP; negative transient; ; T_{amb} = 25 °C	[2]	-	0.4	-	Ω
V_{sbck}	snapback voltage	I_I = 1 A; TLP 100/10 ns; T_{amb} = 25 °C		-	3.3	-	V
V_{CL}	clamping voltage	I_{PP} = 5 A; positive transient; T_{amb} = 25 °C	[3]	-	5	-	V
		I_{PP} = -5 A; negative transient; T_{amb} = 25 °C	[3]	-	-5	-	V

[1] The parameter is guaranteed by design.
[2] 100 ns Transmission Line Pulse (TLP), 50 Ω, pulser at 80 ns.
[3] According to IEC 61000-4-5 (8/20 µs current waveform).



differential mode

Fig. 1. Insertion loss; typical values



$$a = \frac{C_{line}}{C_{line}(V_I = 0\ V)}$$

Fig. 2. Relative capacitance as a function of input voltage; typical values

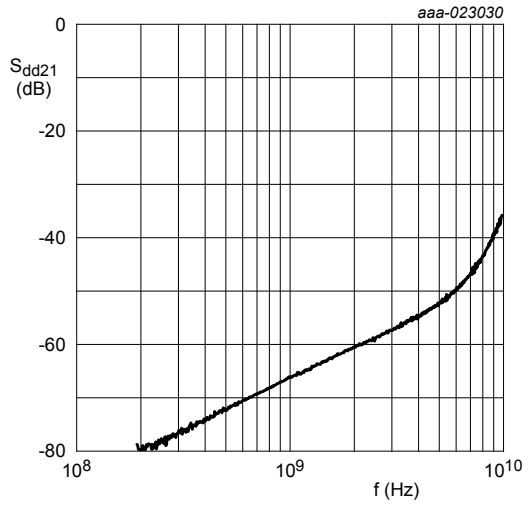
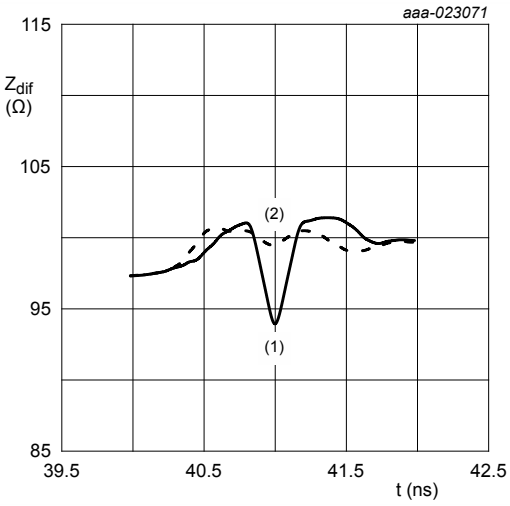
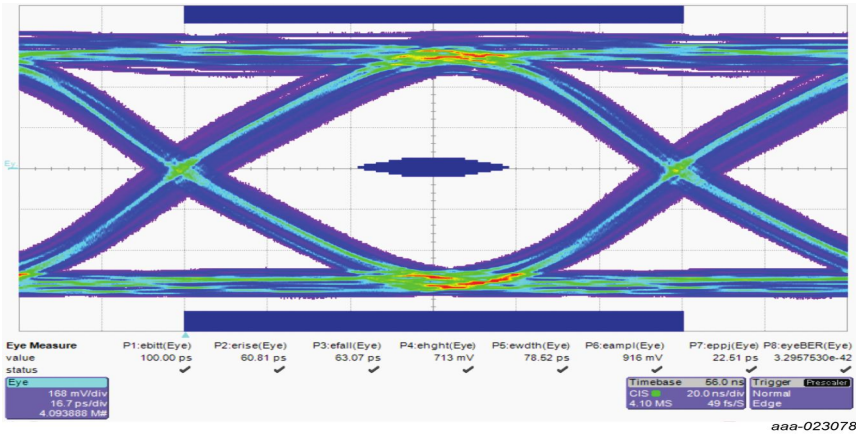


Fig. 3. Differential crosstalk; typical values



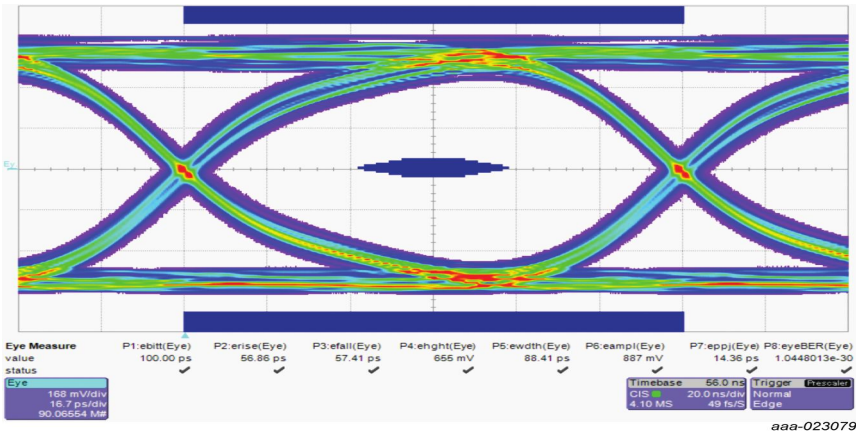
t_r = 200 ps
(1) Device on reference board
(2) Reference board without Device Under Test (DUT)

Fig. 4. Differential Time Domain Reflectometer (TDR) plot; typical values



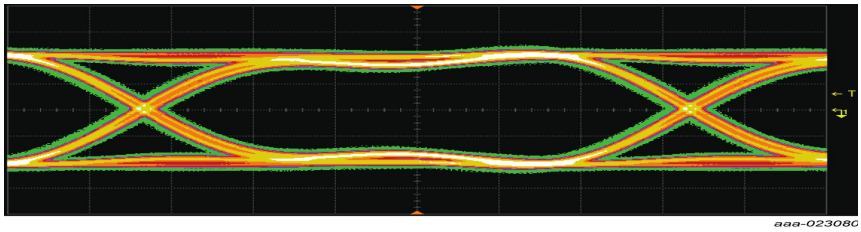
Data rate: 10 Gbit/s

Fig. 5. USB 3.1 eye diagram, PCB with device



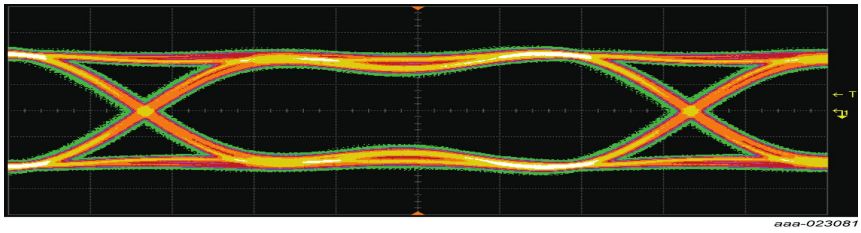
Data rate: 10 Gbit/s

Fig. 6. USB 3.1 eye diagram, PCB without device



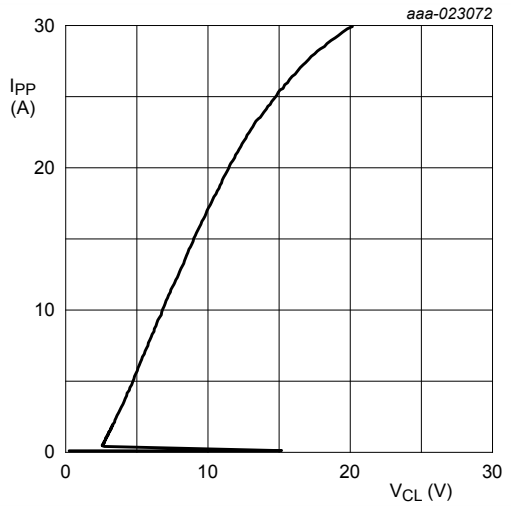
Test frequency: 148.5 MHz
Differential swing voltage: 840 mV
Horizontal scale: 25 ps/div

Fig. 7. HDMI 2.0 TP1 eye diagram, PCB with device



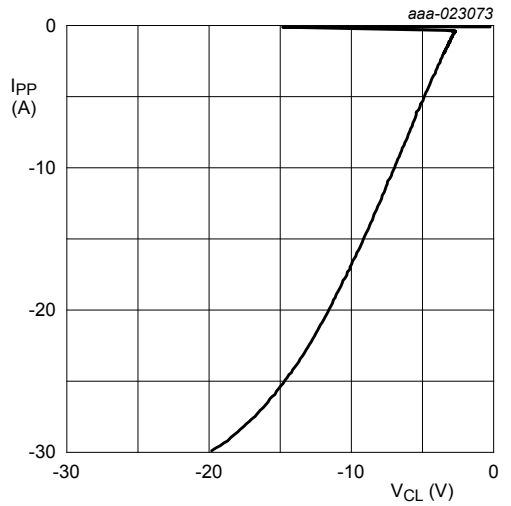
Test frequency: 148.5 MHz
Differential swing voltage: 906 mV
Horizontal scale: 25 ps/div

Fig. 8. HDMI 2.0 TP1 eye diagram, PCB without device



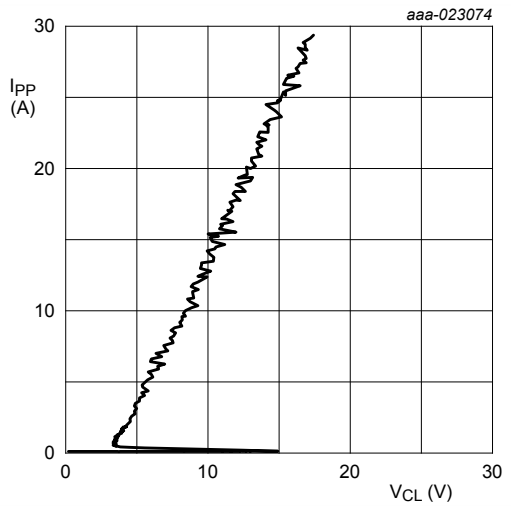
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 9. Dynamic resistance with positive clamping; typical values



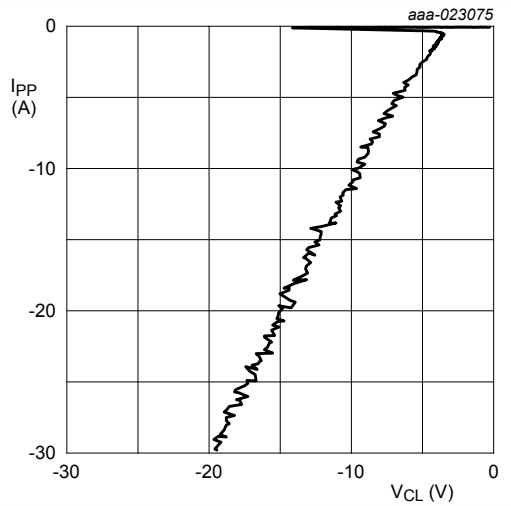
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 10. Dynamic resistance with negative clamping; typical values



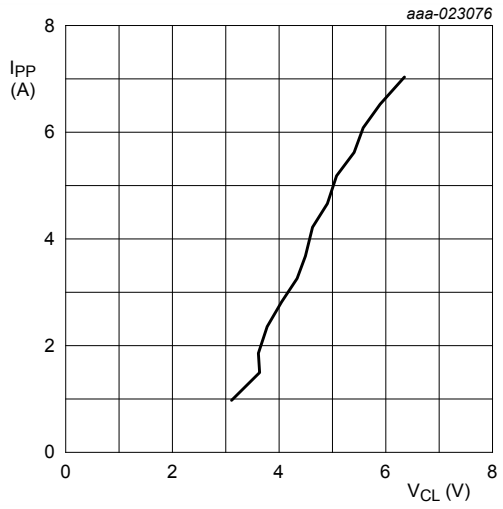
Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns

Fig. 11. Dynamic resistance with positive clamping; typical values



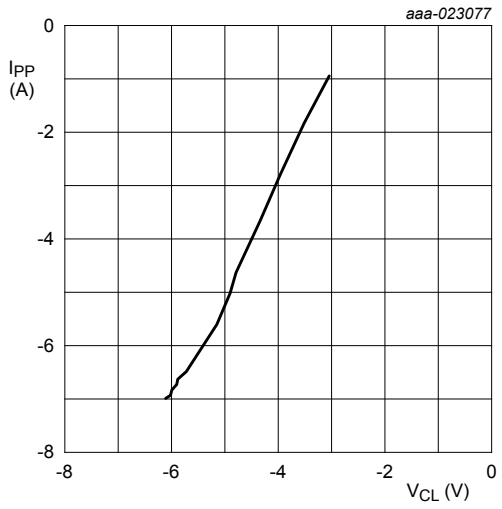
Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns

Fig. 12. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5; t_p = 8/20 µs; positive pulse

Fig. 13. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; t_p = 8/20 µs; negative pulse

Fig. 14. Dynamic resistance with negative clamping; typical values

9. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

Note: When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

Dynamic resistance

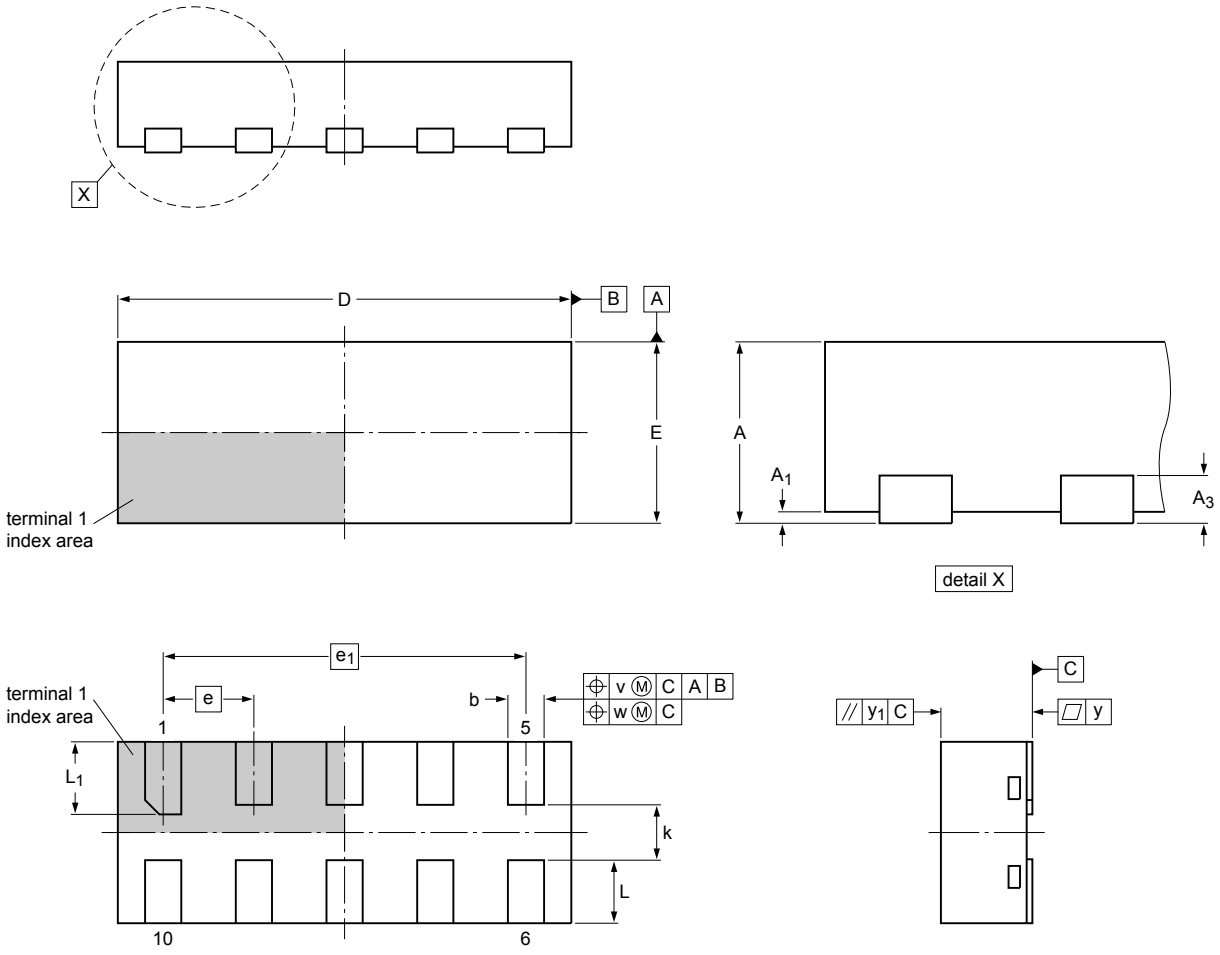
The device uses an advanced clamping structure showing a negative dynamic resistance.

This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

10. Package outline

DFN2510A-10: plastic extremely thin small outline package; no leads; 10 terminals; body 1 x 2.5 x 0.5 mm

SOT1176-1



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	k	L	L_1	v	w	y	y_1
mm	max	0.5	0.05		0.25	2.6	1.1				0.40	0.45				
	nom			0.127	0.20	2.5	1.0	0.5	2		0.35	0.40	0.1	0.05	0.05	0.05
	min		0.00		0.15	2.4	0.9			0.2	0.30	0.35				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

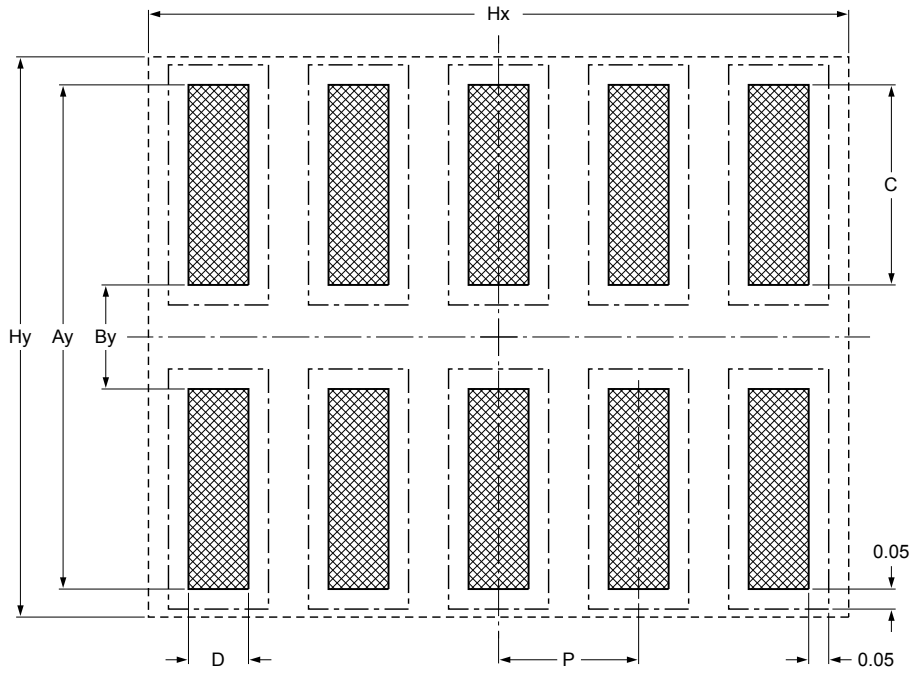
sot1176-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1176-1	- - -	- - -	- - -			~~10-06-22~~ 12-05-22

Fig. 15. Package outline DFN2510A-10 (SOT1176-1)

11. Soldering

Footprint information for reflow soldering of DFN2510A-10 package **SOT1176-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

Dimensions in mm

P	Ay	By	C	D	Hx	Hy
0.5	1.25	0.3	0.475	0.2	2.45	1.5

Remark:
Stencil of 75 μm is recommended.
A stencil of 75 μm gives an aspect ratio of 0.77
With a stencil of 100 μm one will obtain an aspect ratio of 0.58

sot1176-1_fr

Fig. 16. Reflow soldering footprint for DFN2510A-10 (SOT1176-1)

12. Revision history

Table 6. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3FA2 v.1	20180405	Product data sheet	-	-

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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14. Contents

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Date of release: 5 April 2018