NCP2809 Series

Audio Power Amplifier, Stereo Headphone 135 mW

The NCP2809 is a cost−effective stereo audio power amplifier capable of delivering 135 mW of continuous average power per channel into 16 Ω loads.

The NCP2809 audio power amplifier is specifically designed to provide high quality output power from low supply voltage, requiring very few external components. Since NCP2809 does not require bootstrap capacitors or snubber networks, it is optimally suited for low−power portable systems. NCP2809A has an internal gain of 0 dB while specific external gain can externally be set with NCP2809B.

If the application allows it, the virtual ground provided by the device can be connected to the middle point of the headset (Figure 1). In such case, the two external heavy coupling capacitors typically used can be removed. Otherwise, you can also use both outputs in single ended mode with external coupling capacitors (Figure 43).

Due to its excellent Power Supply Rejection Ratio (PSRR), it can be directly connected to the battery, saving the use of an LDO.

Features

- 135 mW to a 16 Ω Load from a 5.0 V Power Supply
- Excellent PSRR (85 dB Typical): Direct Connection to the Battery
- “Pop and Click” Noise Protection Circuit
- Ultra Low Current Shutdown Mode
- 2.2 V–5.5 V Operation
- Outstanding Total Harmonics Distortion + Noise (THD+N): Less than 0.01%
- External Turn−on and Turn−off Configuration Capability
- Thermal Overload Protection Circuitry
- NCP2809B available in Ultra Thin UDFN Package (3x3)
- Pb−Free Packages are Available

Typical Applications

- Cellular Phone
- Portable Stereo
- MP3 Player
- Personal and Notebook Computers

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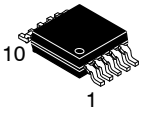
MARKING DIAGRAM



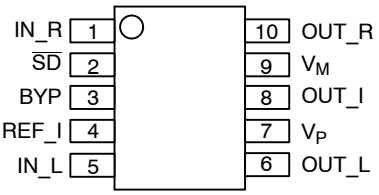
Micro10
DM SUFFIX
CASE 846B

10 PIN DFN
MU SUFFIX
CASE 506AT

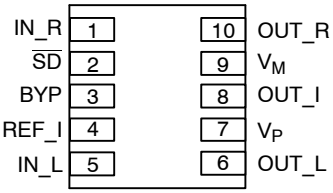
x = E for NCP2809A
C for NCP2809B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)
Micro10



(Top View)
UDFN10

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 22 of this data sheet.

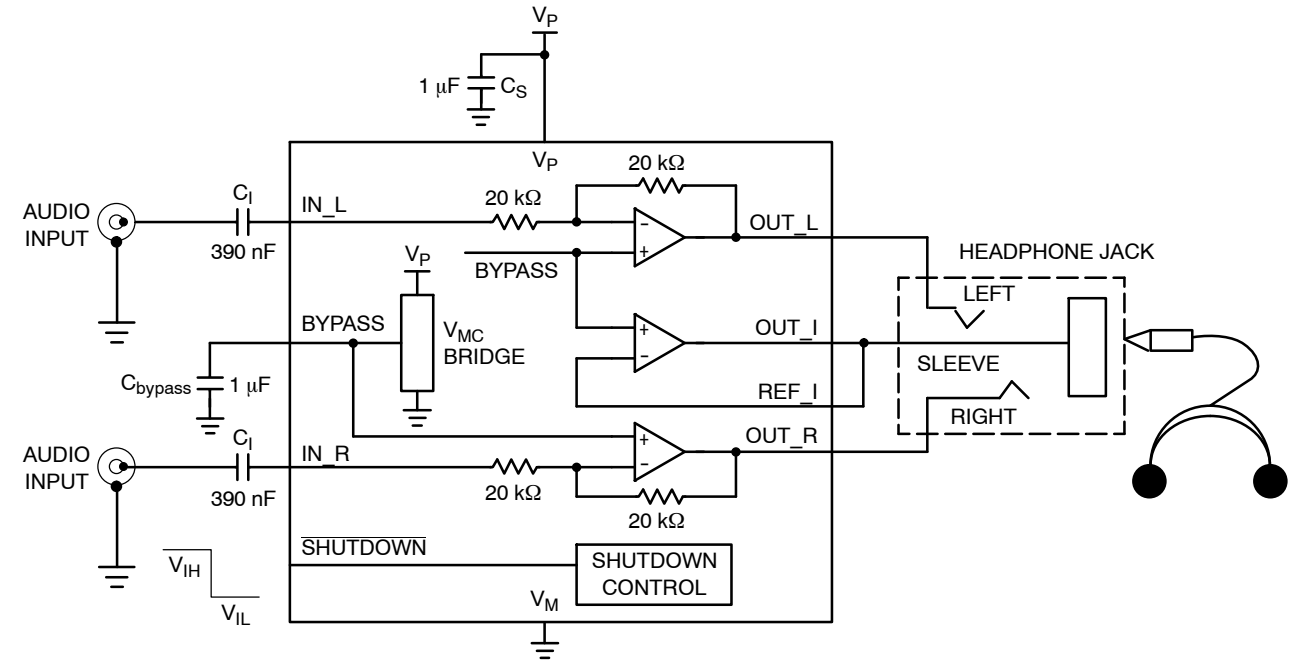


Figure 1. NCP2809A Typical Application Schematic without Output Coupling Capacitor (NOCAP Configuration)

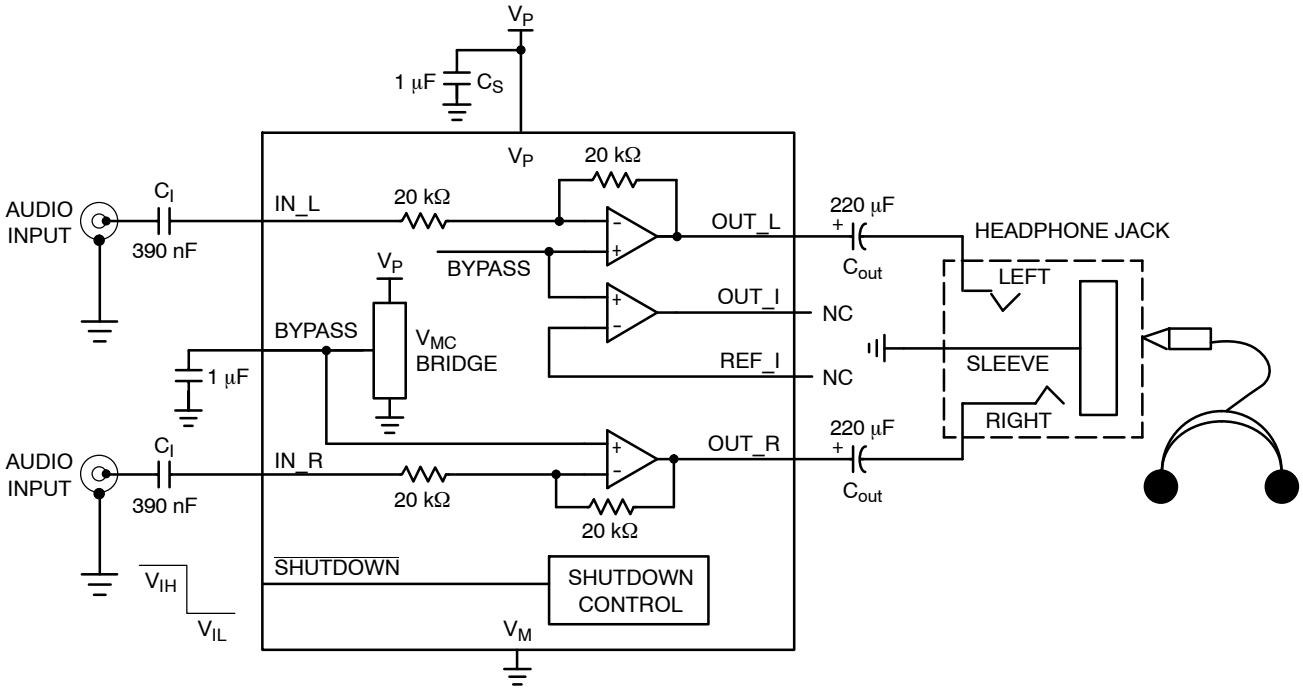


Figure 2. NCP2809A Typical Application Schematic with Output Coupling Capacitor

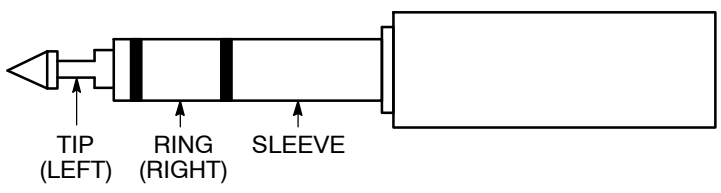


Figure 3. Typical 3−Wire Headphone Plug

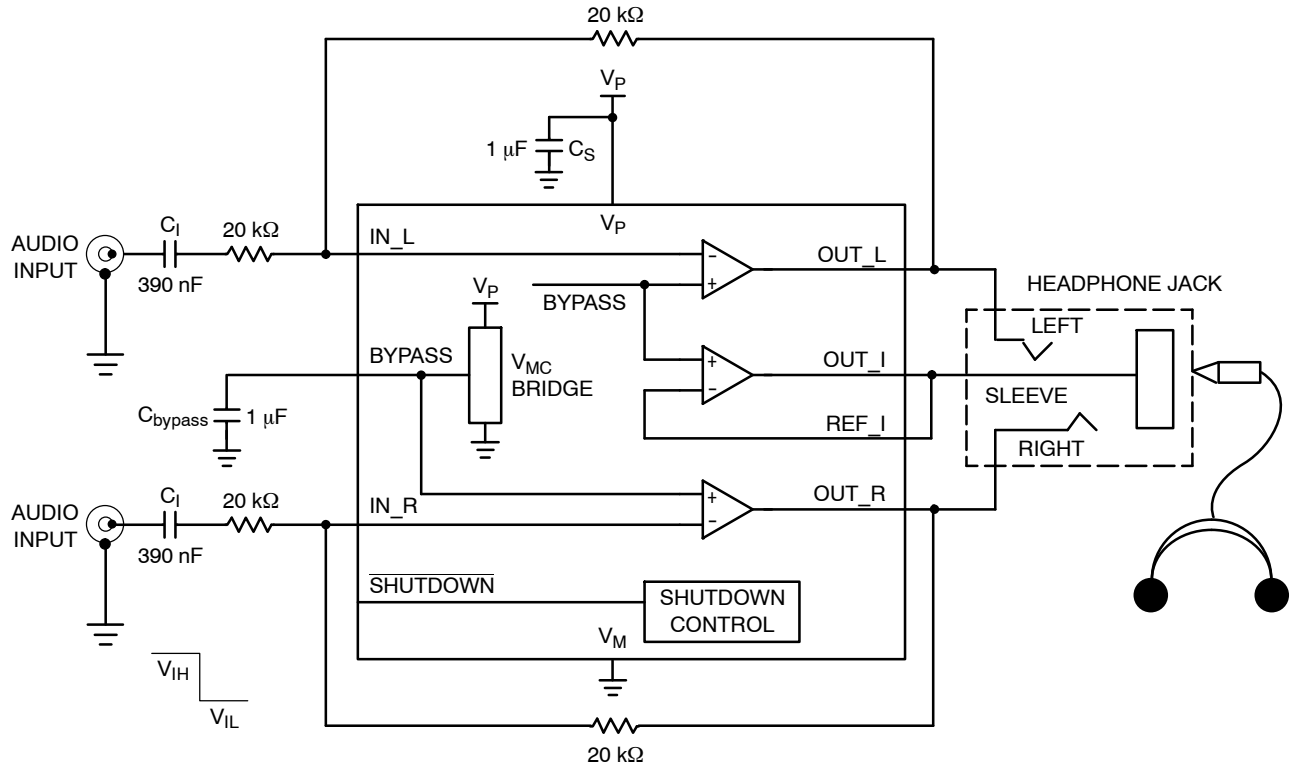


Figure 4. NCP2809B Typical Application Schematic without Output Coupling Capacitor (NOCAP Configuration)

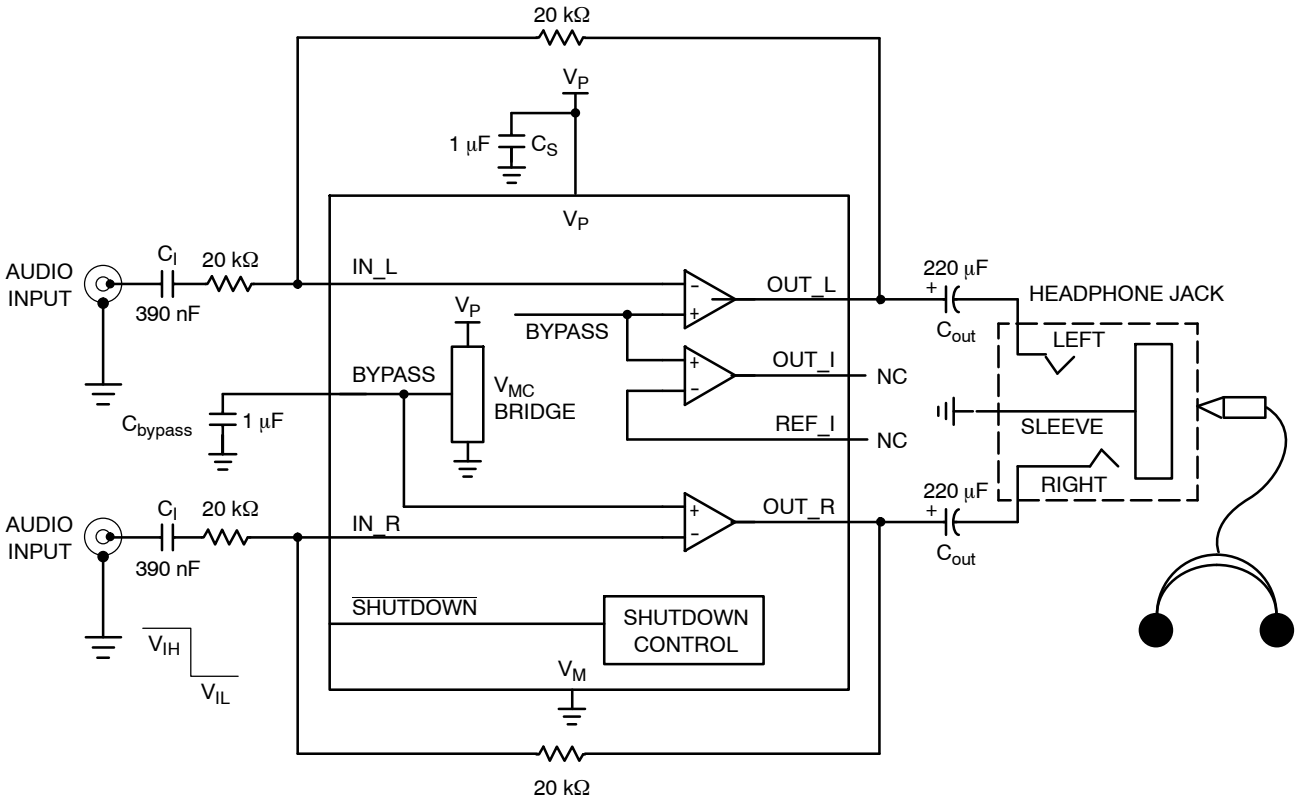


Figure 5. NCP2809B Typical Application Schematic with Output Coupling Capacitor

PIN FUNCTION DESCRIPTION

Pin	Type	Symbol	Description
1	I	IN_R	Negative input of the second amplifier. It receives the audio input signal. Connected to the input capicator C_{in} (NCP2809A) or the external R_{in} (NCP2809B).
2	I	$\overline{\text{SHUTDOWN}}$	The device enters in shutdown mode when a a low level is applied on this pin.
3	I	BYPASS	Bypass capacitor pin which provides the common mode voltage (V_P/2).
4	O	REF_I	Virtual ground amplifier feed back. This pin sets the stereo headset ground. In order to improve crosstalk, this pin must be connected as close as possible to the ground connection of the headset (ideally at the ground pin of the headset connector). When one uses bypassing capacitors, this pin must be left unconnected.
5	I	IN_L	Negative input of the first amplifier. It receives the audio input signal. Connected to the input capacitor C_{in} (NCP2809A) or the external R_{in} (NCP2809B).
6	O	OUT_L	Stereo headset amplifier analog output left. This pin will output the amplified analog signal and, depending on the application, must be coupled with a capacitor or directly connected to the left loudspeaker of the headset. This output is able to drive a 16 Ω load in a single−ended configuration.
7	I	V_P	Positive analog supply of the cell. Range: 2.2 V − 5.5 V
8	O	OUT_I	Virtual ground for stereo Headset common connection. This pin is directly connected to the common connection of the headset when use of bypassing capacitor is not required. When one uses bypassing capacitors, this pin must be left unconnected.
9	I	V_M	Analog Ground
10	O	OUT_R	Stereo headset amplifier analog output right. This pin will output the amplified analog signal and, depending on the application, must be coupled with a capacitor or directly connected to the right loudspeaker of the headset. This output is able to drive a 16 Ω load in a single−ended configuration.

MAXIMUM RATINGS (T_A = +25°C)

Rating		Symbol	Value	Unit
Supply Voltage		V_p	6.0	V
Operating Supply Voltage		O_p V_p	2.2 to 5.5	V
Input Voltage		V_{in}	−0.3 to V_{CC} + 0.3	V
Max Output Current		I_{out}	250	mA
Power Dissipation		P_d	Internally Limited	−
Operating Ambient Temperature		T_A	−40 to +85	°C
Max Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Thermal Resistance, Junction−to−Air	Micro10 UDFN	$R_{\theta JA}$	200 240	°C/W
ESD Protection	Human Body Model (HBM) (Note 1) Machine Model (MM) (Note 2)	−	8000 200	V
Latch up current at Ta = 85°C (Note 3)			±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114 8.0 kV can be applied on OUT_L, OUT_R, REF_I and OUT_I outputs. For other pins, 2.0 kV is the specified voltage.
2. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
3. Maximum ratings per JEDEC standard JESD78.

*This device contains 752 active transistors and 1740 MOS gates.

ELECTRICAL CHARACTERISTICS All the parameters are given in the capless configuration (typical application).
The following parameters are given for the NCP2809A and NCP2809B mounted externally with 0 dB gain, unless otherwise noted.
(For typical values T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{Jmax} = 125°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Supply Quiescent Current	I_{DD}	V_{in} = 0 V, R_L = 16 Ω V_p = 2.4 V V_p = 5.0 V		 1.54 1.84	 2.8 3.6	mA
Output Offset Voltage	V_{off}	V_p = 2.4 V V_p = 5.0 V	−25	1.0	+25	mV
Shutdown Current	I_{SD}	V_p = 5.0 V		10	600	nA
Shutdown Voltage High (Note 5)	V_{SDIH}	−	1.2			V
Shutdown Voltage Low	V_{SDIL}	−			0.4	V
Turning On Time (Note 6)	T_{WU}	C_{by} = 1.0 μF		285		ms
Turning Off Time (Note 6)	T_{SD}	C_{by} = 1.0 μF		50		ms
Max Output Swing	$V_{loadpeak}$	V_p = 2.4 V, R_L = 16 Ω V_p = 5.0 V, R_L = 16 Ω V_p = 2.4 V, R_L = 32 Ω V_p = 5.0 V, R_L = 32 Ω	0.82 1.94	0.9 2.05 1.04 2.26		V
Max Rms Output Power	P_{Orms}	V_p = 2.4 V, R_L = 16 Ω, THD+N<0.1% V_p = 5.0 V, R_L = 16 Ω, THD+N<0.1% V_p = 2.4 V, R_L = 32 Ω, THD+N<0.1% V_p = 5.0 V, R_L = 32 Ω, THD+N<0.1%		24 131 17 80		mW
Voltage Gain	G	NCP2809A only	−0.5	0	+0.5	dB
Input Impedance	Z_{in}	NCP2809A only		20		kΩ
Crosstalk	CS	f = 1.0 kHz V_p = 2.4 V, R_L = 16 Ω, P_{out} = 20 mW V_p = 2.4 V, R_L = 32 Ω, P_{out} = 10 mW V_p = 3.0 V, R_L = 16 Ω, P_{out} = 30 mW V_p = 3.0 V, R_L = 32 Ω, P_{out} = 20 mW V_p = 5.0 V, R_L = 16 Ω, P_{out} = 75 mW V_p = 5.0 V, R_L = 32 Ω, P_{out} = 50 mW		 −63.5 −72.5 −64 −73 −64 −73		dB
Signal to Noise Ratio	SNR	f = 1.0 kHz V_p = 2.4 V, R_L = 16 Ω, P_{out} = 20 mW V_p = 2.4 V, R_L = 32 Ω, P_{out} = 10 mW V_p = 3.0 V, R_L = 16 Ω, P_{out} = 30 mW V_p = 3.0 V, R_L = 32 Ω, P_{out} = 20 mW V_p = 5.0 V, R_L = 16 Ω, P_{out} = 75 mW V_p = 5.0 V, R_L = 32 Ω, P_{out} = 50 mW		 88.3 89 90.5 92 95.1 96.1		dB

4. Min/Max limits are guaranteed by production test.
5. At T_A = −40°C, the minimum value is set to 1.5 V.
6. See page 10 for a theoretical approach to these parameters.

ELECTRICAL CHARACTERISTICS All the parameters are given in the capless configuration (typical application).
The following parameters are given for the NCP2809A and NCP2809B mounted externally with 0 dB gain, unless otherwise noted.
(For typical values T_A = 25°C, for min and max values T_A = −40°C to 85°C, T_{Jmax} = 125°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Positive Supply Rejection Ratio	PSRR V+	R_L = 16 Ω $V_{pripple\_pp}$ = 200 mV C_{by} = 1.0 μF Input Terminated with 10 Ω **NCP2809A** F = 217 Hz V_p = 5.0 V V_p = 2.4 V F = 1.0 kHz V_p = 5.0 V V_p = 2.4 V		 −73 −82 −73 −85		dB
Positive Supply Rejection Ratio	PSRR V+	R_L = 16 Ω $V_{pripple\_pp}$ = 200 mV C_{by} = 1.0 μF Input Terminated with 10 Ω **NCP2809B** with 0 dB External Gain F = 217 Hz V_p = 5.0 V V_p = 2.4 V F = 1.0 kHz V_p = 5.0 V V_p = 2.4 V		 −80 −82 −81 −81		dB
Efficiency	η	V_P = 5.0 V, R_L = 16 Ω = 135 mW		63		%
Thermal Shutdown Temperature (Note 8)	T_{sd}	–		160		°C
Total Harmonic Distortion + Noise (Note 9)	THD+N	V_P = 2.4 V, f = 1.0 kHz R_L = 16 Ω, P_{out} = 20 mW R_L = 32 Ω, P_{out} = 15 mW V_P = 5.0 V, f = 1.0 kHz R_L = 16 Ω, P_{out} = 120 mW R_L = 32 Ω, P_{out} = 70 mW		 0.006 0.004 0.005 0.003		%

7. Min/Max limits are guaranteed by production test.
8. This thermal shutdown is made with an hysteresis function. Typically, the device turns off at 160°C and turns on again when the junction temperature is less than 140°C.
9. The outputs of the device are sensitive to a coupling capacitor to Ground. To ensure THD+N at very low level for any sort of headset (16 Ω or 32 Ω), outputs (OUT_R, OUT_L, OUT_I and REF_I) must not be grounded with more than 500 pF.

TYPICAL CHARACTERISTICS

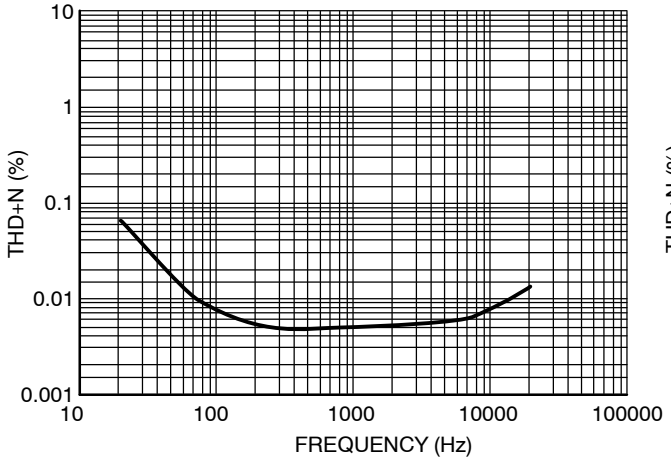


Figure 6. THD+N vs. Frequency
V_p = 5.0 V, R_L = 16 Ω, P_{out} = 75 mW

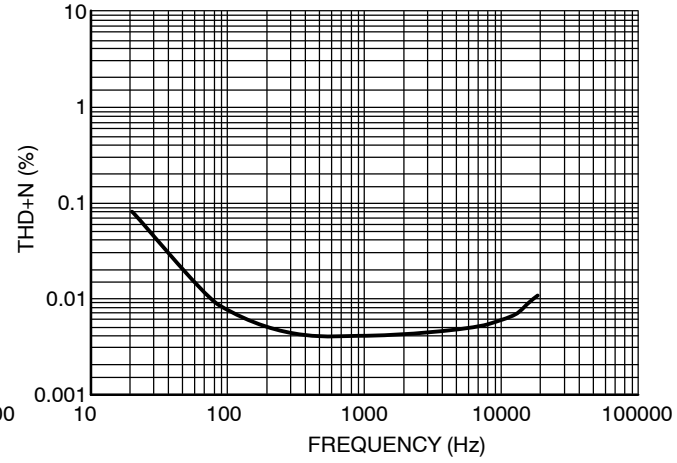


Figure 7. THD+N vs. Frequency
V_p = 5.0 V, R_L = 32 Ω, P_{out} = 50 mW

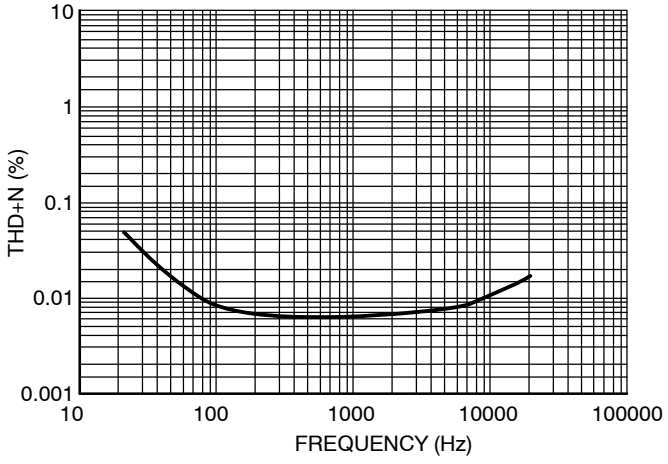


Figure 8. THD+N vs. Frequency
V_p = 3.0 V, R_L = 16 Ω, P_{out} = 30 mW

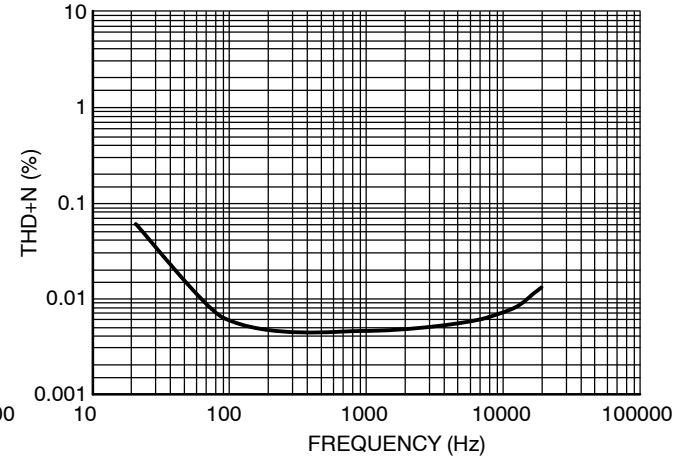


Figure 9. THD+N vs. Frequency
V_p = 3.0 V, R_L = 32 Ω, P_{out} = 20 mW

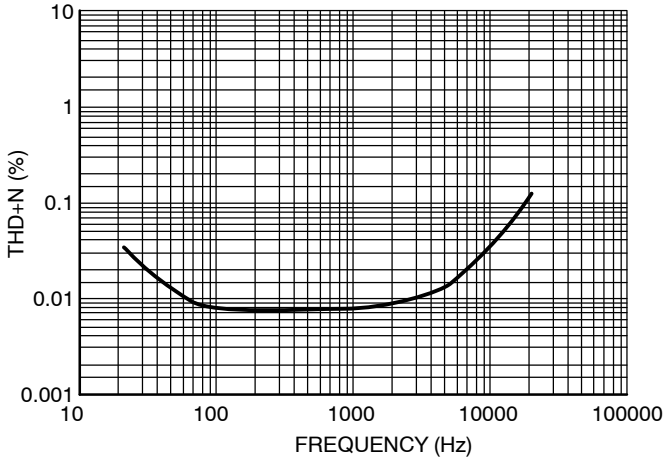


Figure 10. THD+N vs. Frequency
V_p = 2.4 V, R_L = 16 Ω, P_{out} = 20 mW

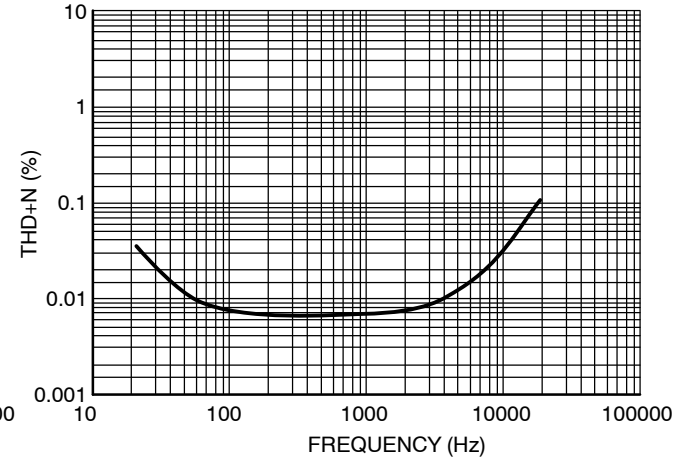


Figure 11. THD+N vs. Frequency
V_p = 2.4 V, R_L = 32 Ω, P_{out} = 10 mW

TYPICAL CHARACTERISTICS

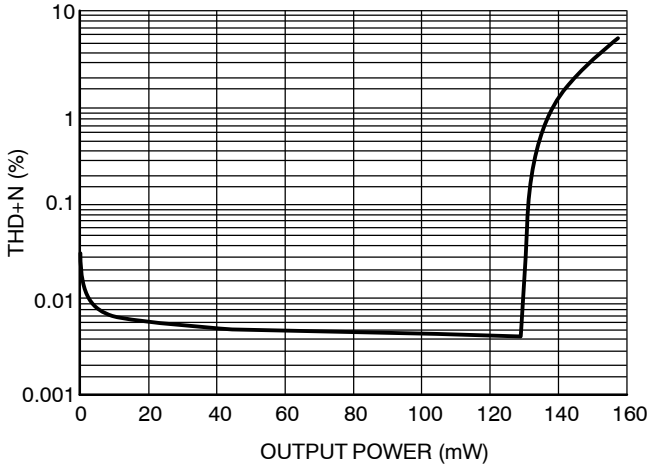


Figure 12. THD+N vs. Power Out
V_p = 5.0 V, R_L = 16 Ω, 1.0 kHz

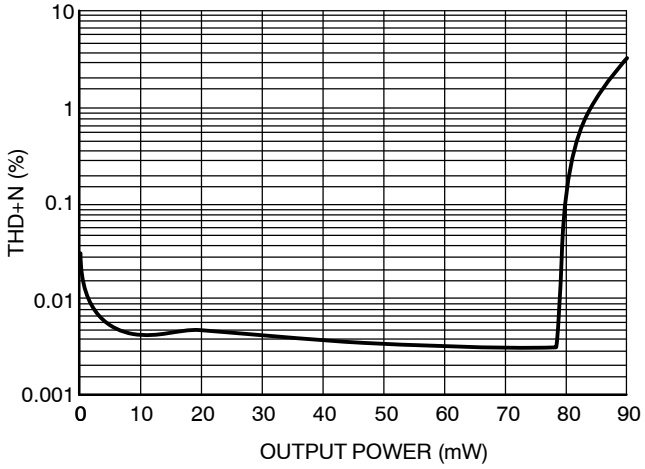


Figure 13. THD+N vs. Power Out
V_p = 5.0 V, R_L = 32 Ω, 1.0 kHz

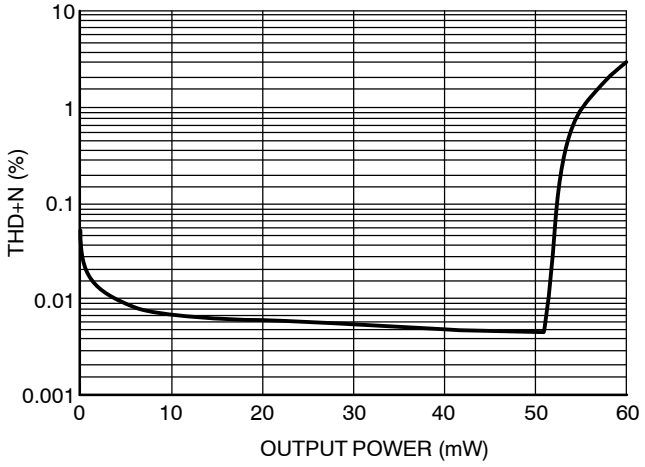


Figure 14. THD+N vs. Power Out
V_p = 3.3 V, R_L = 16 Ω, 1.0 kHz

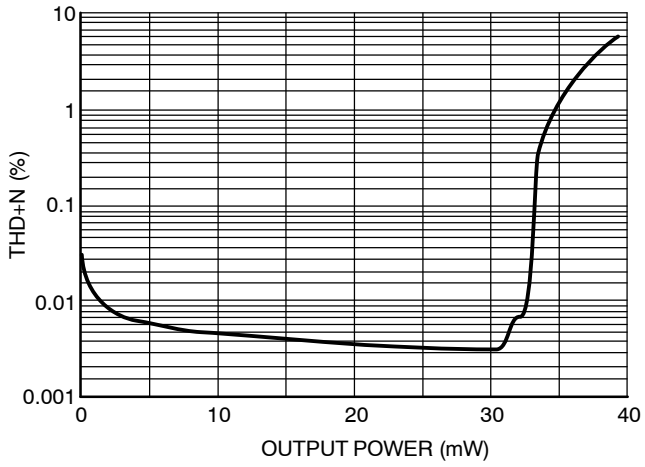


Figure 15. THD+N vs. Power Out
V_p = 3.3 V, R_L = 32 Ω, 1.0 kHz

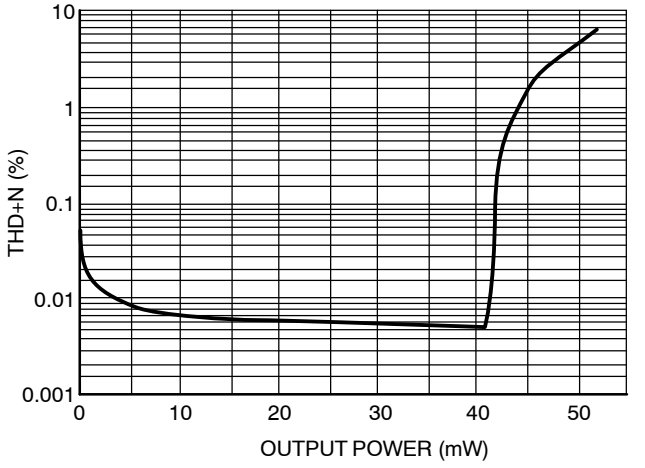


Figure 16. THD+N vs. Power Out
V_p = 3.0 V, R_L = 16 Ω, 1.0 kHz

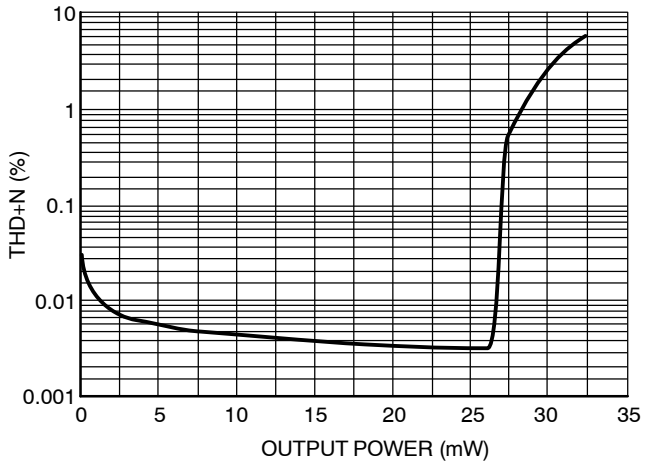


Figure 17. THD+N vs. Power Out
V_p = 3.0 V, R_L = 32 Ω, 1.0 kHz

TYPICAL CHARACTERISTICS

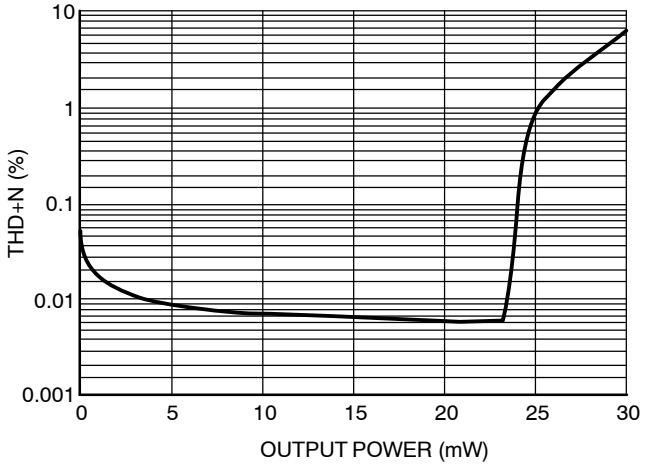


Figure 18. THD+N vs. Power Out
V_p = 2.4 V, R_L = 16 Ω, 1.0 kHz

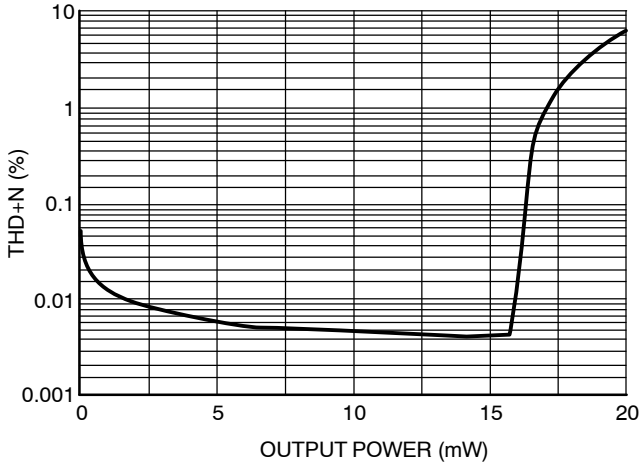


Figure 19. THD+N vs. Power Out
V_p = 2.4 V, R_L = 3.2 Ω, 1.0 kHz

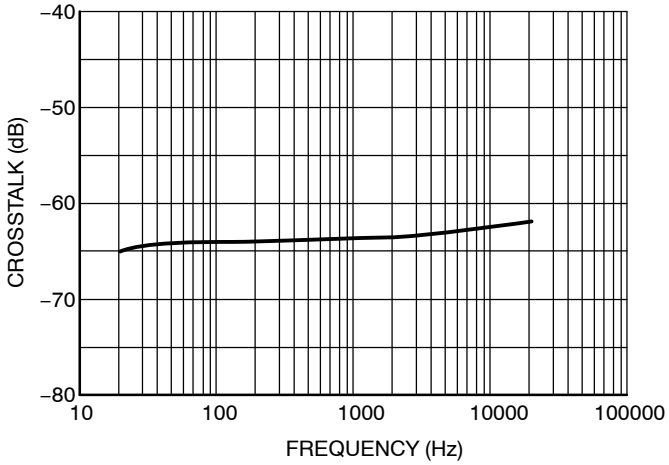


Figure 20. Crosstalk
V_p = 5.0 V, R_L = 16 Ω, P_{out} = 75 mW

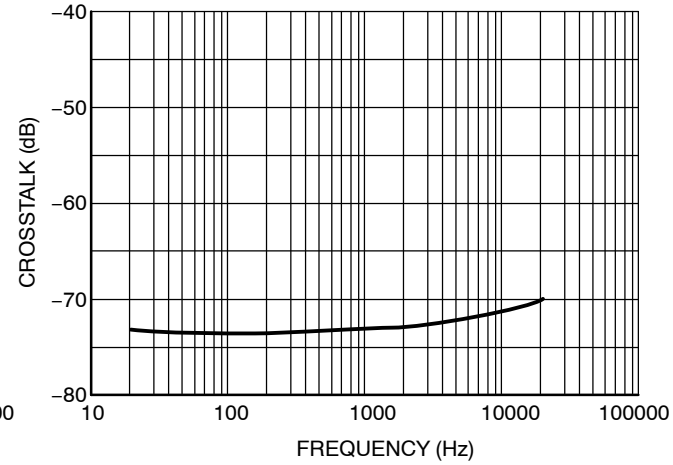


Figure 21. Crosstalk
V_p = 5.0 V, R_L = 32 Ω, P_{out} = 50 mW

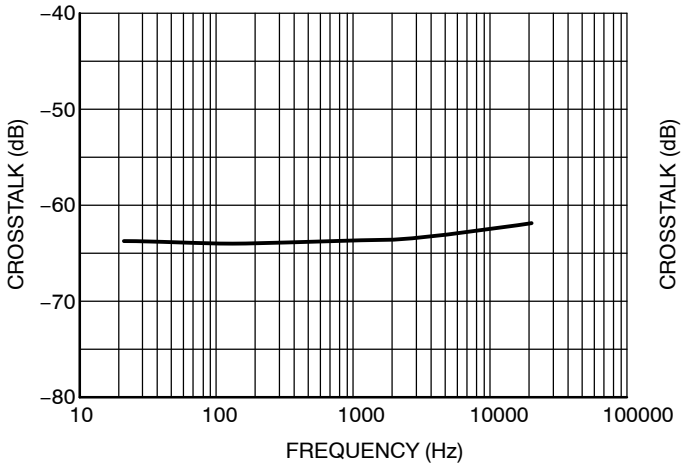


Figure 22. Crosstalk
V_p = 3.0 V, R_L = 16 Ω, P_{out} = 30 mW

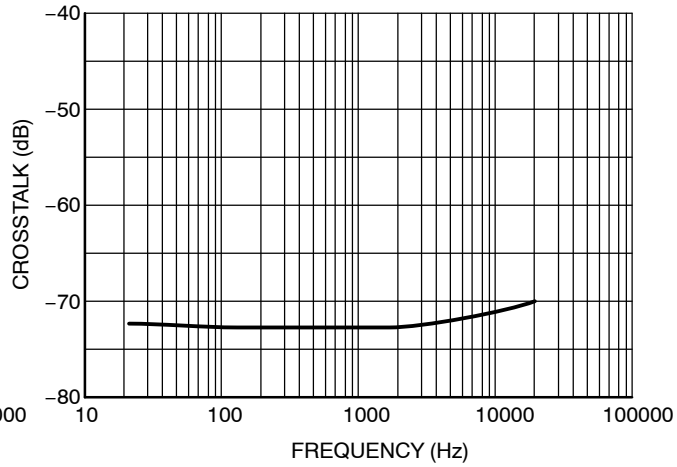


Figure 23. Crosstalk
V_p = 3.0 V, R_L = 32 Ω, P_{out} = 20 mW

TYPICAL CHARACTERISTICS

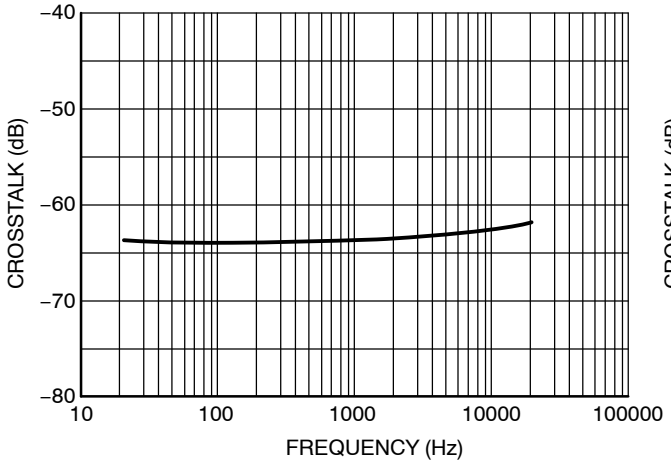


Figure 24. Crosstalk
V_p = 2.4 V, R_L = 16 Ω, P_{out} = 20 mW

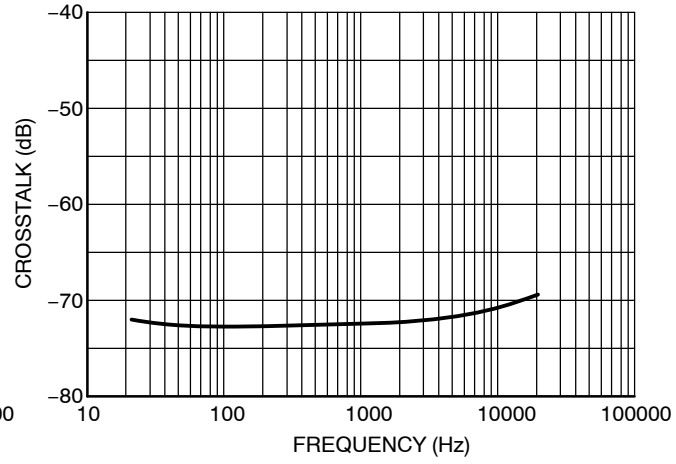


Figure 25. Crosstalk
V_p = 2.4 V, R_L = 32 Ω, P_{out} = 10 mW

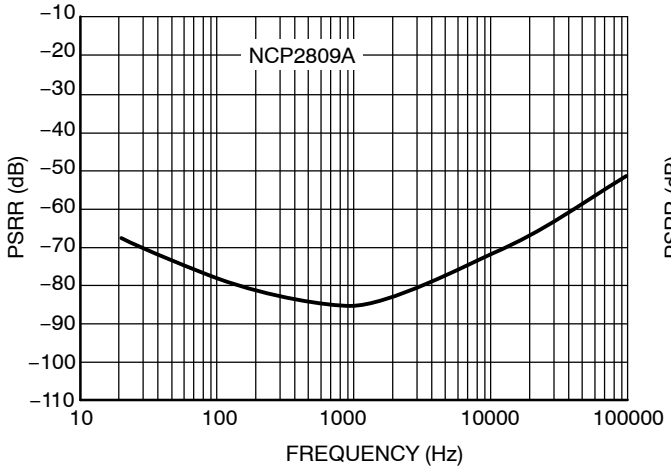


Figure 26. PSRR − Input Grounded with 10 Ω
V_p = 2.4 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω

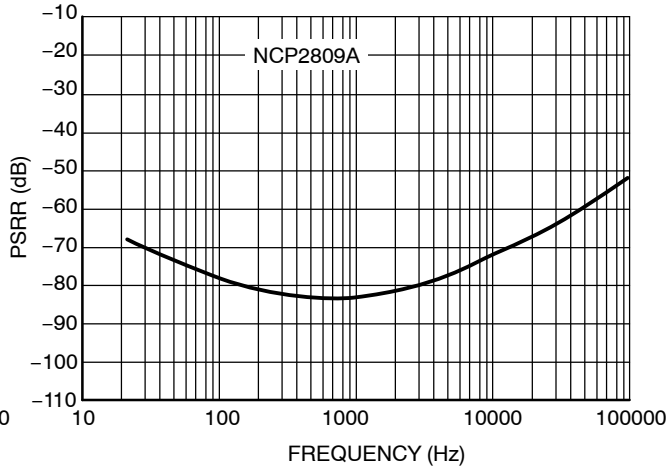


Figure 27. PSRR − Input Grounded with 10 Ω
V_p = 2.4 V, V_{ripple} = 200 mV pk−pk, R_L = 32 Ω

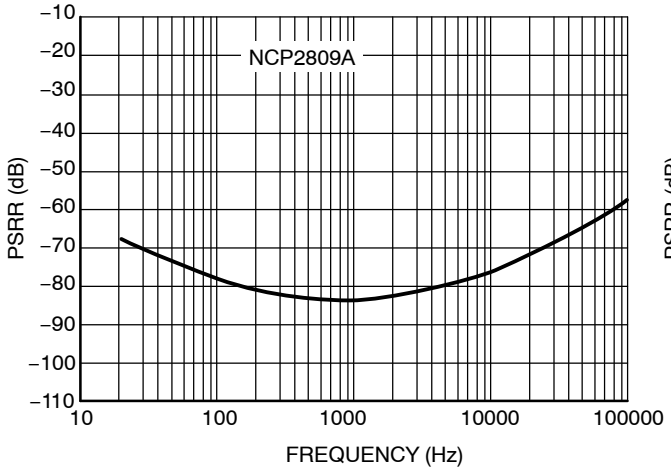


Figure 28. PSRR − Input Grounded with 10 Ω
V_p = 3.0 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω

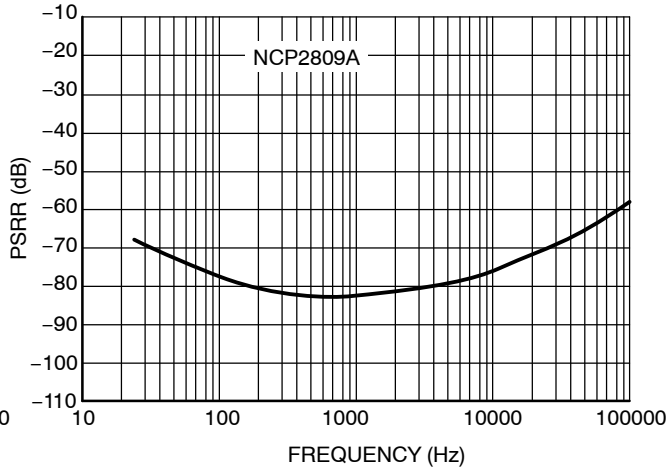


Figure 29. PSRR − Input Grounded with 10 Ω
V_p =3.0 V, V_{ripple} = 200 mV pk−pk, R_L = 32 Ω

TYPICAL CHARACTERISTICS

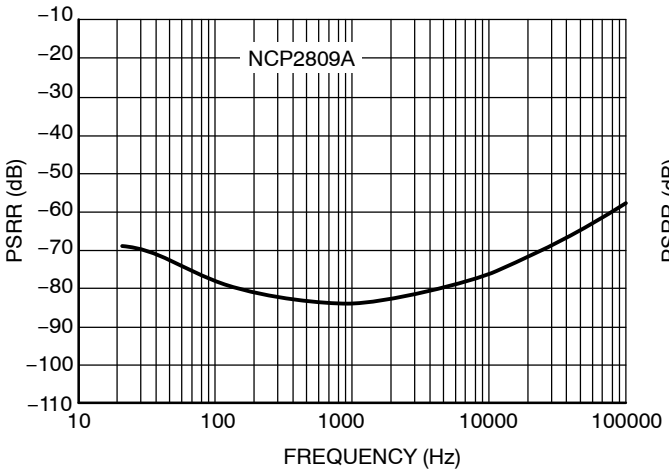


Figure 30. PSRR − Input Grounded with 10 Ω
V_p = 3.3 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω

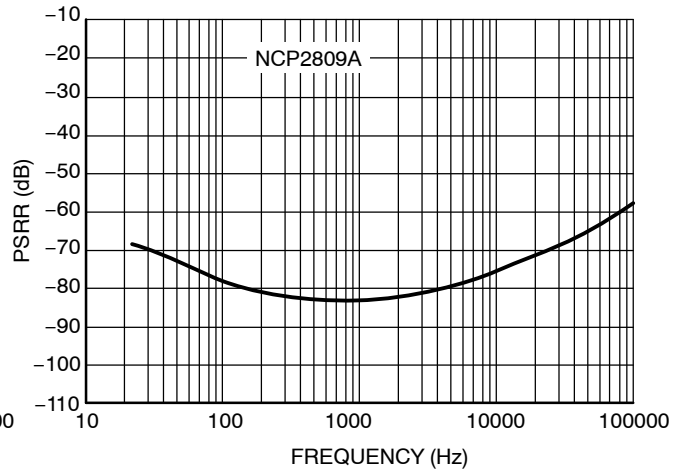


Figure 31. PSRR − Input Grounded with 10 Ω
V_p = 3.3 V, V_{ripple} = 200 mV pk−pk, R_L = 32 Ω

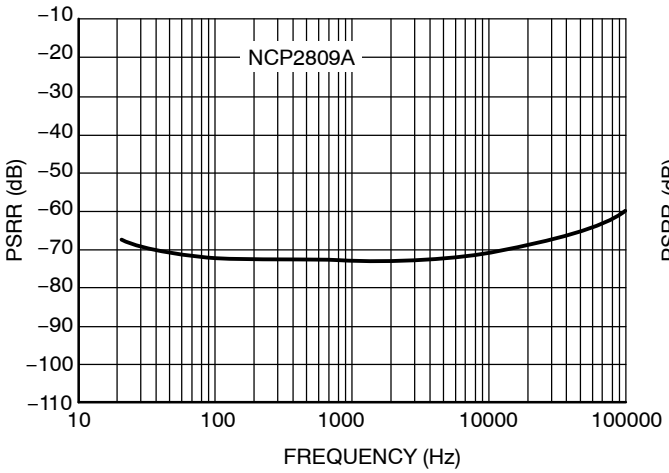


Figure 32. PSRR − Input Grounded with 10 Ω
V_p = 5.0 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω

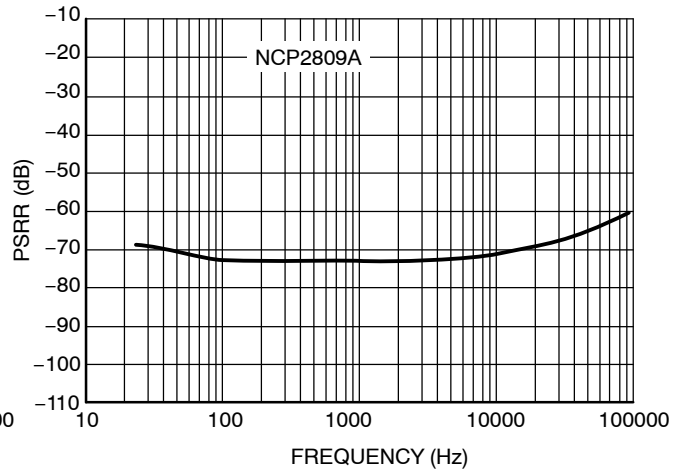


Figure 33. PSRR − Input Grounded with 10 Ω
V_p = 5.0 V, V_{ripple} = 200 mV pk−pk, R_L = 32 Ω

TYPICAL CHARACTERISTICS

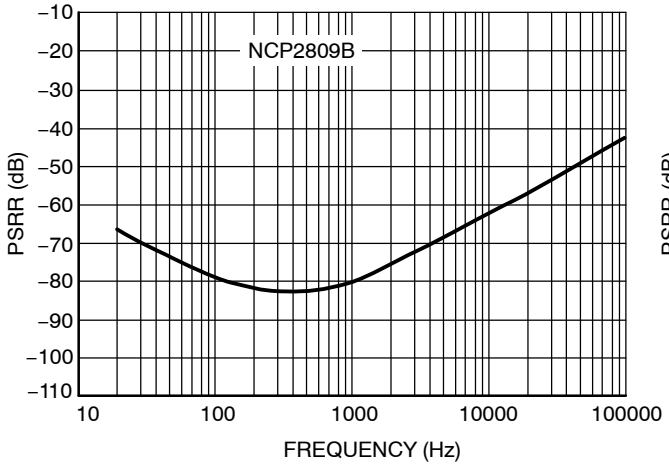


Figure 34. PSRR − Input Grounded with 10 Ω V_p = 2.4 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω, G = 1 (0 dB)

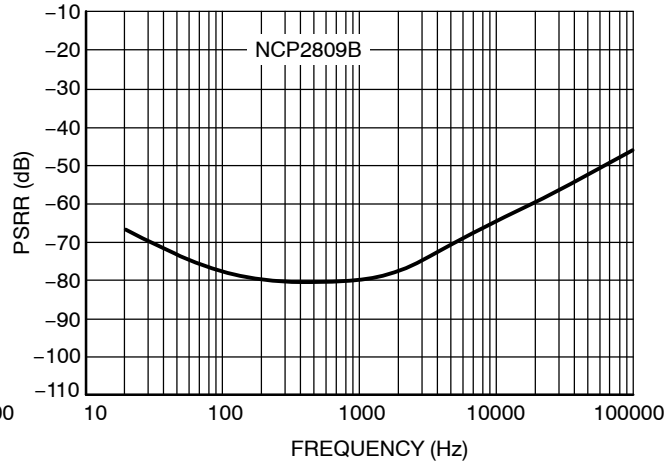


Figure 35. PSRR − Input Grounded with 10 Ω V_p = 5.0 V, V_{ripple} = 200 mV pk−pk, R_L = 16 Ω, G = 1 (0 dB)

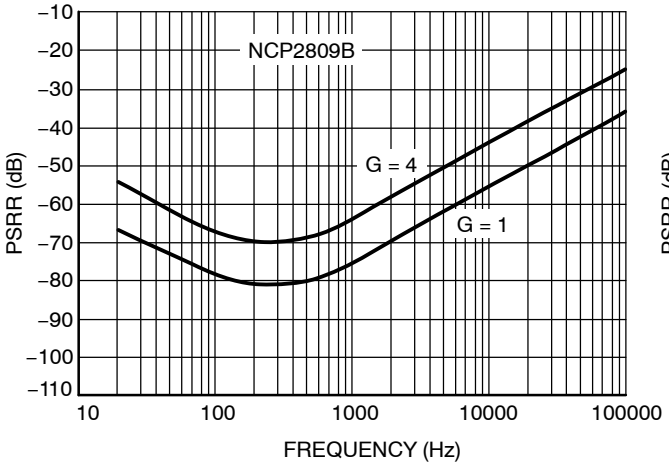


Figure 36. PSRR − Input Grounded with 10 Ω V_p = 2.4 V, V_{ripple} = 200 mV pk−pk, R_L =16 Ω, G = 1 (0 dB) and G = 4 (12 dB)

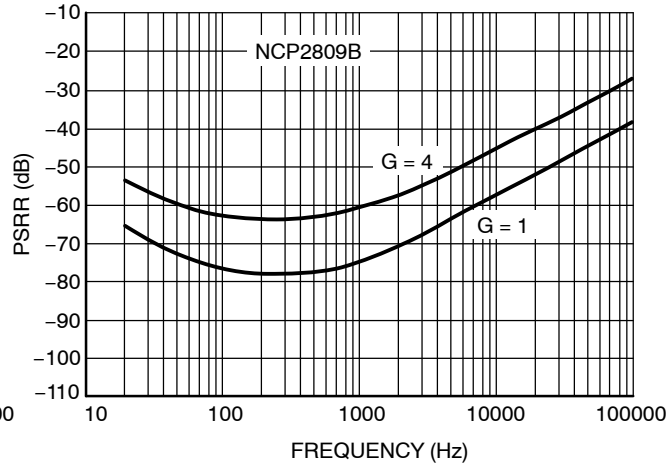


Figure 37. PSRR − Input Grounded with 10 Ω V_p = 5.0 V, V_{ripple} = 200 mV pk−pk, R_L = 16 Ω, G = 1 (0 dB) and G = 4 (12 dB)

TYPICAL CHARACTERISTICS

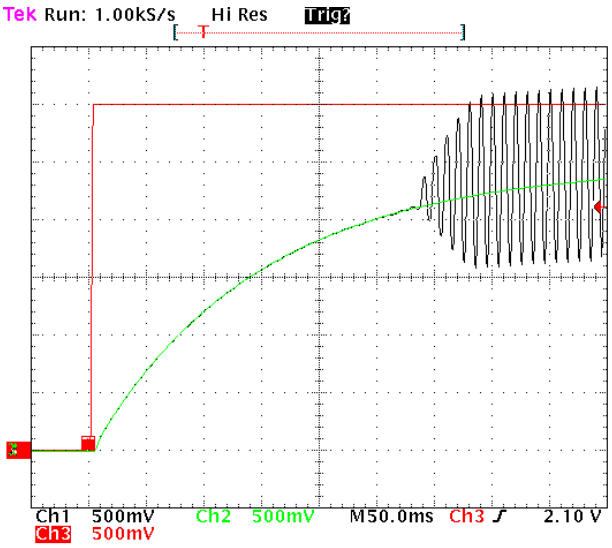


Figure 38. Turning–On Time/V_p = 5.0 V and F = 100 Hz Ch1 = OUT_R, Ch2 = VMC and Ch3 = Shutdown

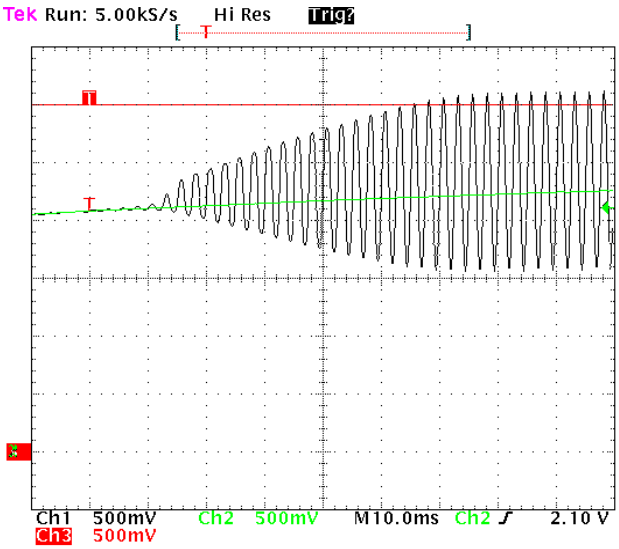


Figure 39. Turning–On Time Zoom/V_p = 5.0 V and F = 400 Hz Ch1 = OUT_R, Ch2 = VMC and Ch3 = Shutdown

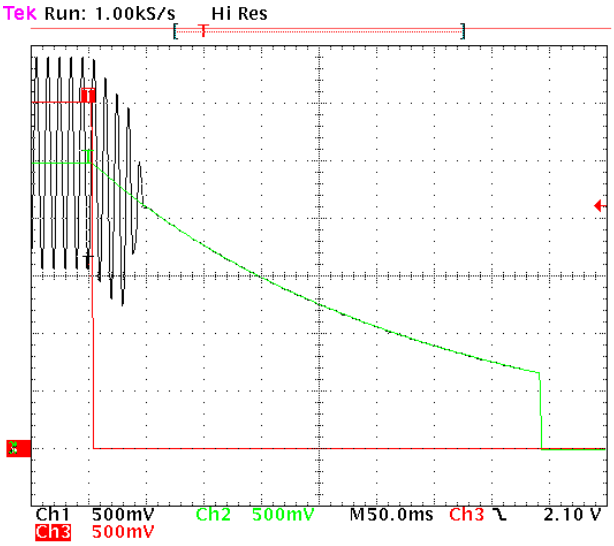


Figure 40. Turning–Off Time/V_p = 5.0 V and F = 100 Hz Ch1 = OUT_R, Ch2 = VMC and Ch3 = Shutdown

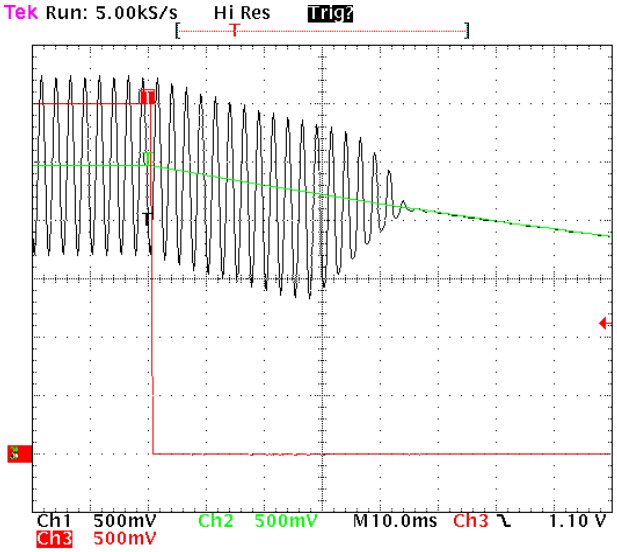


Figure 41. TurningOff Time Zoom/Vp = 5.0 V and F = 400 Hz Ch1 = OUT_R, Ch2 = VMC and Ch3 = Shutdown

APPLICATION INFORMATION

Detailed Description

The NCP2809 power audio amplifier can operate from 2.6 V to 5.0 V power supply. It delivers 24 mW_{rms} output power to a 16 Ω load (V_P = 2.4 V) and 131 mW_{rms} output power to a 16 Ω load (V_P = 5.0 V).

The structure of NCP2809 is basically composed of two identical internal power amplifiers; NCP2809A has a fixed internal gain of 0 dB and the gain can be set externally with the NCP2809B.

Internal Power Amplifier

The output P_{mos} and N_{mos} transistors of the amplifier are designed to deliver the specified output power without clipping. The channel resistance (R_{on}) of the N_{mos} and P_{mos} transistors does not exceed 3.0 Ω when driving current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages in order to maximize bandwidth and DC gain.

Turn−On and Turn−Off Transitions

A Turn−on/off transition is shown in the following plot corresponding to curves in Figures 38 to 41.

In order to eliminate “pop and click” noises during transitions, output power in the load must be slowly established or cut. When logic high is applied to the shutdown pin, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the gain is established slowly (50 ms). This way to turn−on the device is optimized in terms of rejection of “pop and click” noises.

A theoretical value of turn−on time at 25°C is given by the following formula.

C_{by}: Bypass Capacitor

R: Internal 300 k resistor with a 25% accuracy

$T_{on} = 0.95 * R * C_{by}$

When logic is turned low on shutdown pin, the device enters in shutdown mode:

− 50 ms later the audio signal is cut off as the gain is turned to zero internally as shown in Figure 41.

− 385 ms later, the DC signal will reach 0.7 V due to exponential discharge of the bypass voltage. It is then tied to Ground as shown in Figure 40.

A theoretical approach of this time is:

$T_{off} = R * C_{by} * Ln(V_p/1.4)$

Shutdown Function

The device enters shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 600 nA.

Current Limit Protection Circuitry

The maximum output power of the circuit (P_{Orms} = 135 mW, V_P = 5.0 V, R_L = 16 Ω) requires a peak current in the load of 130 mA.

In order to limit excessive power dissipation in the load when a short−circuit occurs, the current limit in the load is fixed to 250 mA. The current in the output MOS transistors is real−time monitored, and when exceeding 250 mA, the gate voltage of the corresponding MOS transistor is clipped and no more current can be delivered.

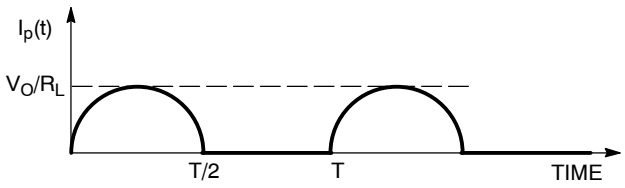
Thermal Overload Protection Circuitry

Internal amplifiers are switched off when temperature exceeds 160°C, and will be switched back on only when the temperature goes below 140°C.

NCP2809 is a stereo power audio amplifier.

If the application requires a Single Ended topology with output coupling capacitors, then the current provided by the battery for one output is as following:

- $V_O(t)$ is the AC voltage seen by the load. Here we consider a sine wave signal with a period T and a peak voltage V_O.
- R_L is the load.



So, the total power delivered by the battery to the device is:

$$P_{TOT} = V_p \times I_{pavg}$$

$$I_{pavg} = \frac{1}{2\pi} \times \int_0^{\pi} \frac{V_o}{R_L} \sin(t)dt = \frac{V_o}{\pi.R_L}$$

$$P_{TOT} = \frac{V_p.V_o}{\pi.R_L}$$

The power in the load is P_{OUT}.

$$P_{OUT} = \frac{V_O^2}{2R_L}$$

The dissipated power by the device is

$$P_D = P_{TOT} - P_{OUT}$$

$$P_D = \frac{V_o}{R_L} \times \left[\frac{V_P}{\pi} - \frac{V_O}{2}\right]$$

At a given power supply voltage, the maximum power dissipated is:

$$P_{Dmax} = \frac{V_P^2}{2\pi^2.R_L}$$

Of course, if the device is used in a typical stereo application, each load with the same output power will give the same dissipated power. Thus the total lost power for the device is:

$$P_D = \frac{V_o}{R_L} \times \left[\frac{2V_P}{\pi} - V_O\right]$$

And in this case, the maximum power dissipated will be:

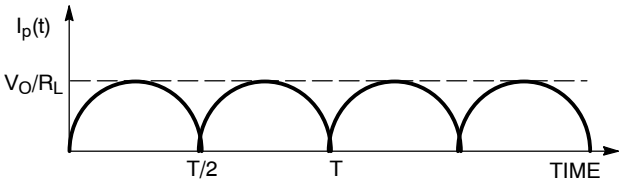
$$P_{Dmax} = \frac{V_P^2}{\pi^2.R_L}$$

In single ended operation, the efficiency is:

$$\eta = \frac{\pi.V_O}{2V_P}$$

If the application requires a NOCAP scheme without output coupling capacitors, then the current provided by the battery for one output is as following:

- $V_o(t)$ is the AC voltage seen by the load. Here we consider a sine wave signal with a period T and a peak voltage V_O.
- R_L is the load.



So, the total power delivered by the battery to the device is:

$$P_{TOT} = V_p \times I_pavg$$

$$I_pavg = \frac{1}{\pi} \times \int_0^{\pi} \frac{V_o}{R_L} \sin(t)dt = \frac{2V_o}{\pi.R_L}$$

$$P_{TOT} = \frac{2V_p.V_o}{\pi.R_L}$$

The power in the load is P_{OUT}

$$P_{OUT} = \frac{V_O^2}{2R_L}$$

The dissipated power by the device is

$$P_D = P_{TOT} - P_{OUT}$$

$$P_D = \frac{V_o}{R_L} \times \left[\frac{2V_P}{\pi} - \frac{V_O}{2}\right]$$

At a given power supply voltage, the maximum power dissipated happens when $V_O = Vp/2$.

$$P_{Dmax} = \frac{0.19V_P^2}{R_L}$$

Of course, if the device is used in a typical stereo application, each load with the same output power will give the same dissipated power. Thus the total lost power for the device is:

$$P_D = \frac{V_o}{R_L} \times \left[\frac{4V_P}{\pi} - V_O\right]$$

And in this case, the maximum power dissipated will be:

$$P_{Dmax} = \frac{0.38V_P^2}{R_L}$$

In NOCAP operation, the efficiency is:

$$\eta = \frac{\pi.V_O}{4V_P}$$

Gain−Setting Selection

With NCP2809 Audio Amplifier family, you can select a closed−loop gain of 0db for the NCP2809A and an external gain setting with the NCP2809B. In order to optimize device and system performance, NCP2809 needs to be used in low gain configurations. It minimizes THD+N values and maximizes the signal−to−noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

NCP2809A can be used when a 0 dB gain is required. Adjustable gain is available on NCP2809B.

NCP2809 Amplifier External Components

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with the internal (A version with 20 kΩ) or external (B version) resistor. Its cut−off frequency is given by:

$$f_c = \frac{1}{2 * \pi * R_{in} * C_{in}} \quad \text{(eq. 1)}$$

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage ($V_P/2$) and can increase the turn−on pops.

An input capacitor value of 100 nF performs well in many applications (in case of R_{in} = 20 kΩ).

Bypass Capacitor Selection (C_{bypass})

The bypass capacitor C_{by} provides half−supply filtering and determines how fast the NCP2809 turns on.

A proper supply bypassing is critical for low noise performance and high power supply rejection ratio.

Moreover, this capacitor is a critical component to minimize the turn−on pop noise. A 1.0 μF bypass capacitor value should produce clickless and popless shutdown transitions. The amplifier is still functional with a 0.1 μF capacitor value but is more sensitive to “pop and click” noises.

Thus, for optimized performances, a 1.0 μF ceramic bypassing capacitor is recommended.

Without Output Coupling Capacitor

As described in Figure 42, the internal circuitry of the NCP2809 device eliminates need of heavy bypassing capacitors when connecting a stereo headset with 3 connecting points. This circuitry produces a virtual ground and does not affect either output power or PSRR. Additionally, eliminating these capacitors reduces cost and PCB place.

However, user must take care to the connection between pin REF_I and ground of the headset: this pin is the ground reference for the headset. **So, in order to improve crosstalk performances, this pin must be plugged directly to the middle point of the headset connector.**

With Output Coupling Capacitor

However, when using a low cost jack connector (with third connection to ground), the headset amplifier requires very few external components as described in Figure 43. Only two external coupling capacitors are needed. The main concern is in output coupling capacitors, because of the value and consequently the size of the components required. Purpose of these capacitors is biasing DC voltage and very low frequency elimination. Both, coupling capacitor and output load form a high pass filter. Audible frequency ranges from 20 Hz to 20 kHz, but headset used in portable appliance has poor ability to reproduce signals below 75 or 100 Hz. Input coupling capacitor and input resistance also form a high pass filter. These two first order filters form a second order high pass filter with the same −3 dB cut off frequency. Consequently, the below formula must be followed:

$$\frac{1}{2 \times \pi \times R_{in} \times C_{in}} \approx \frac{1}{2 \times \pi \times R_L \times C_{out}} \qquad \text{(eq. 2)}$$

As for a loudspeaker amplifier, the input impedance value for calculating filters cut off frequency is the minimum input impedance value at maximum output volume.

To obtain a frequency equal to when frequency is 5 times the cut off frequency, attenuation is 0.5 dB. So if we want a ±0.5 dB at 150 Hz, we need to have a –3 dB cut off frequency of 30 Hz:

$$f_{-3dB} \geq \frac{1}{2 \times \pi \times R_L \times C_{out}} \qquad \text{(eq. 3)}$$

$$C_{out} \geq \frac{1}{2 \times \pi \times R_L \times f_{-3dB}} \qquad \text{(eq. 4)}$$

With R_L = 16 Ω, and f_{-3dB} = 30 Hz formula (4) shows that $C_{out} \geq 330$ μF.

With C_{out} = 220 μF, ±0.5 dB attenuation frequency will be 225 Hz with a –3.0 dB cut off frequency of 45 Hz. Following this, the input coupling capacitor choice is straightforward. Using formula (2) input coupling capacitor value would be 68 nF for a 220 μF output coupling capacitor and 100 nF for a 330 μF output coupling capacitor.

When using the NCP2809 with this configuration, pins REF_I and OUT_I must be left unconnected
(see Figure 43).

Optimum Equivalent Capacitance at Output Stage

Cellular phone and wireless portable device designers normally place several Radio Frequency filtering capacitors and ESD protection devices between the outputs and the headset connector. Those devices are usually connected between amplifier outputs and ground, or amplifier output and virtual ground. Different headsets with different impedance can be used with NCP2809. 16, 32 and 64Ohm are standard values. The extra impedance resulting of parasitic headset inductance and protections capacitance can affect sound quality.

In order to achieve the best sound quality, we suggest the optimum value of total equivalent capacitance:

- Between each output terminal to the virtual ground should be less than or equal to 100pF
- Between each output terminal to the ground should be less than or equal to 100pF.

This total equivalent capacitance consists of the radio frequency filtering capacitors and ESD protection device equivalent parasitic capacitance. Because of their very low parasitic capacitance value, diode based ESD protection are preferred.

If for some reason the above requirements cannot be met, a series resistor between each NCP2809 output and the protection device can improve amplifier operation. In order to keep dynamic output signal range, the resistor value should be very small compared to the loudspeaker impedance. For example, a 10Ohm resistor for a 64Ohm loudspeaker allows up to 400pF parasitic capacitance load.

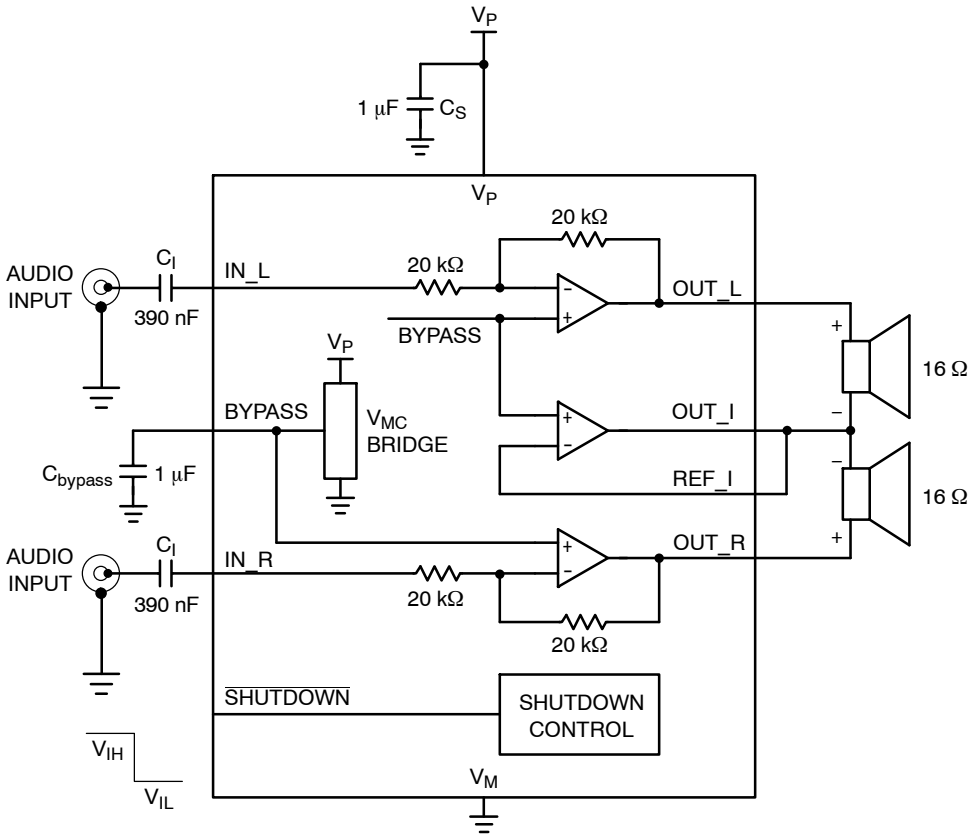


Figure 42. Typical Application Schematic Without Output Coupling Capacitor

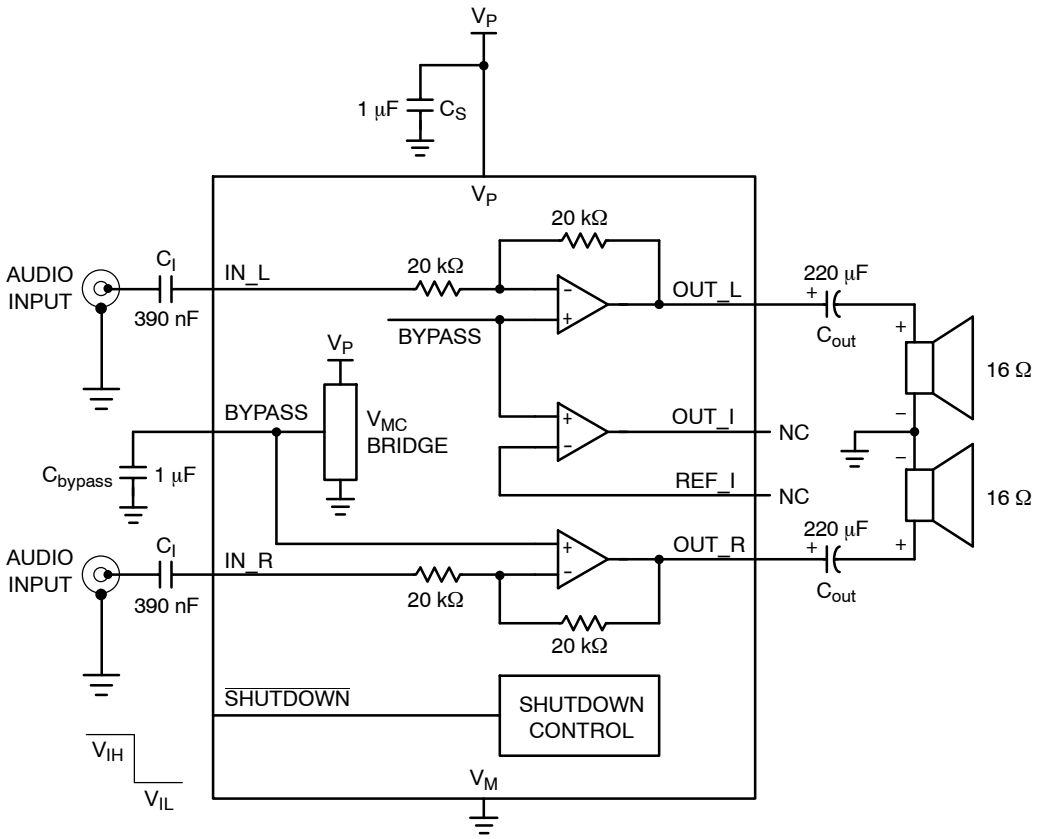


Figure 43. Typical Application Schematic With Output Coupling Capacitor

DEMONSTRATION BOARD AND LAYOUT GUIDELINES

Demonstration Board for Micro10 Devices

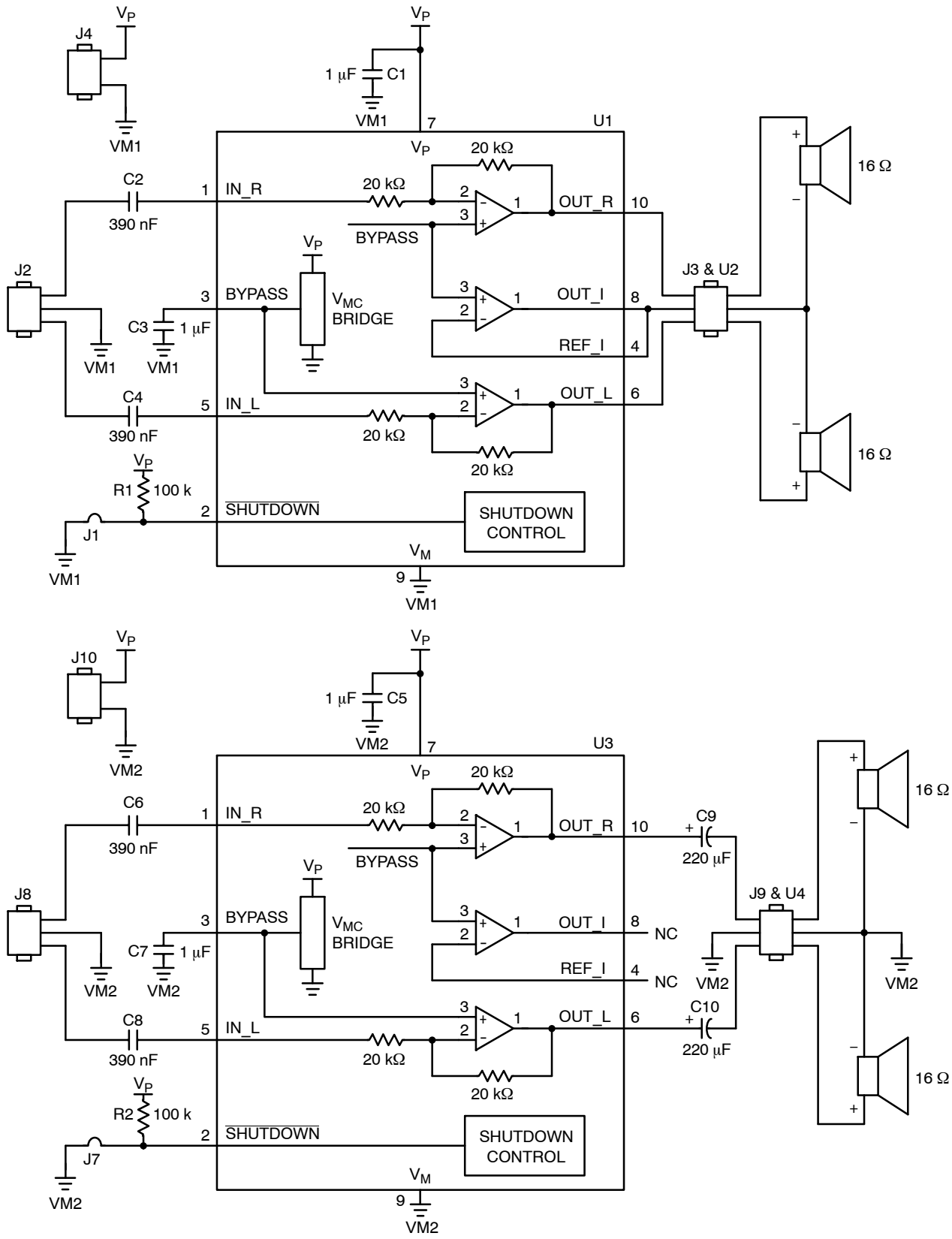
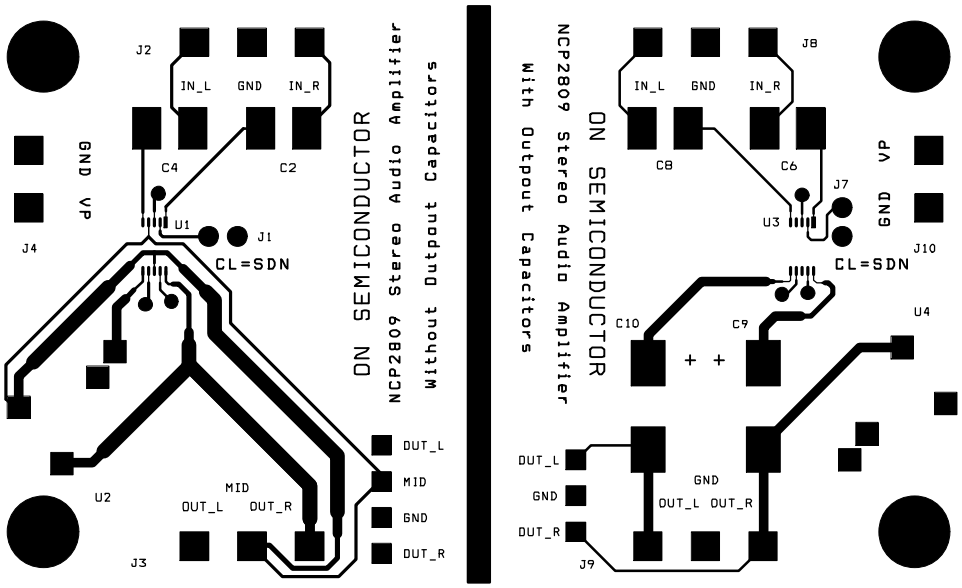
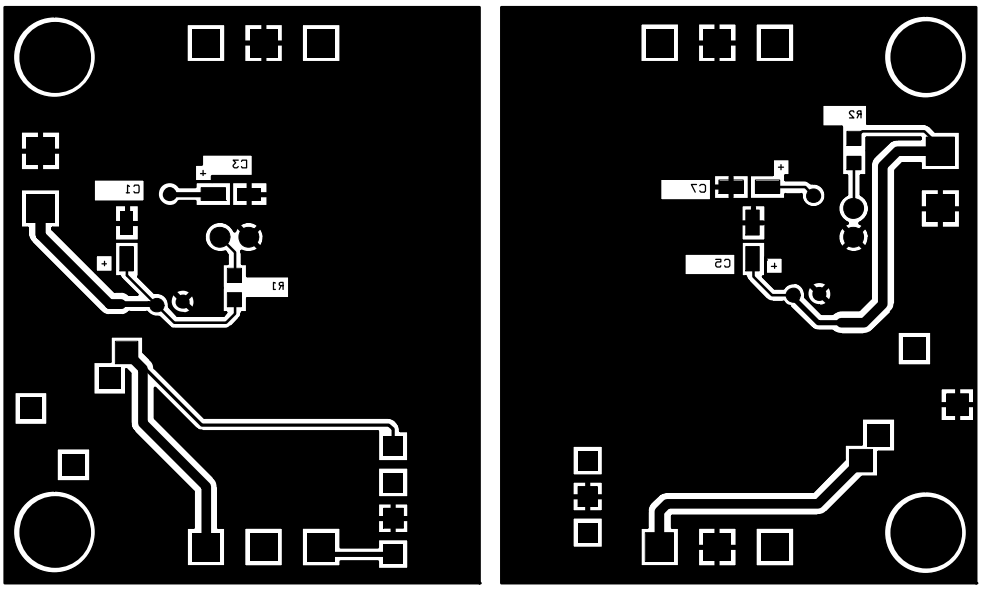


Figure 44. Schematic of the Demonstration Board for Micro10 Device



TOP LAYER



BOTTOM LAYER

Figure 45. Demonstration Board for Micro10 Device – PCB Layers

Demonstration Board for UDFN10 Device

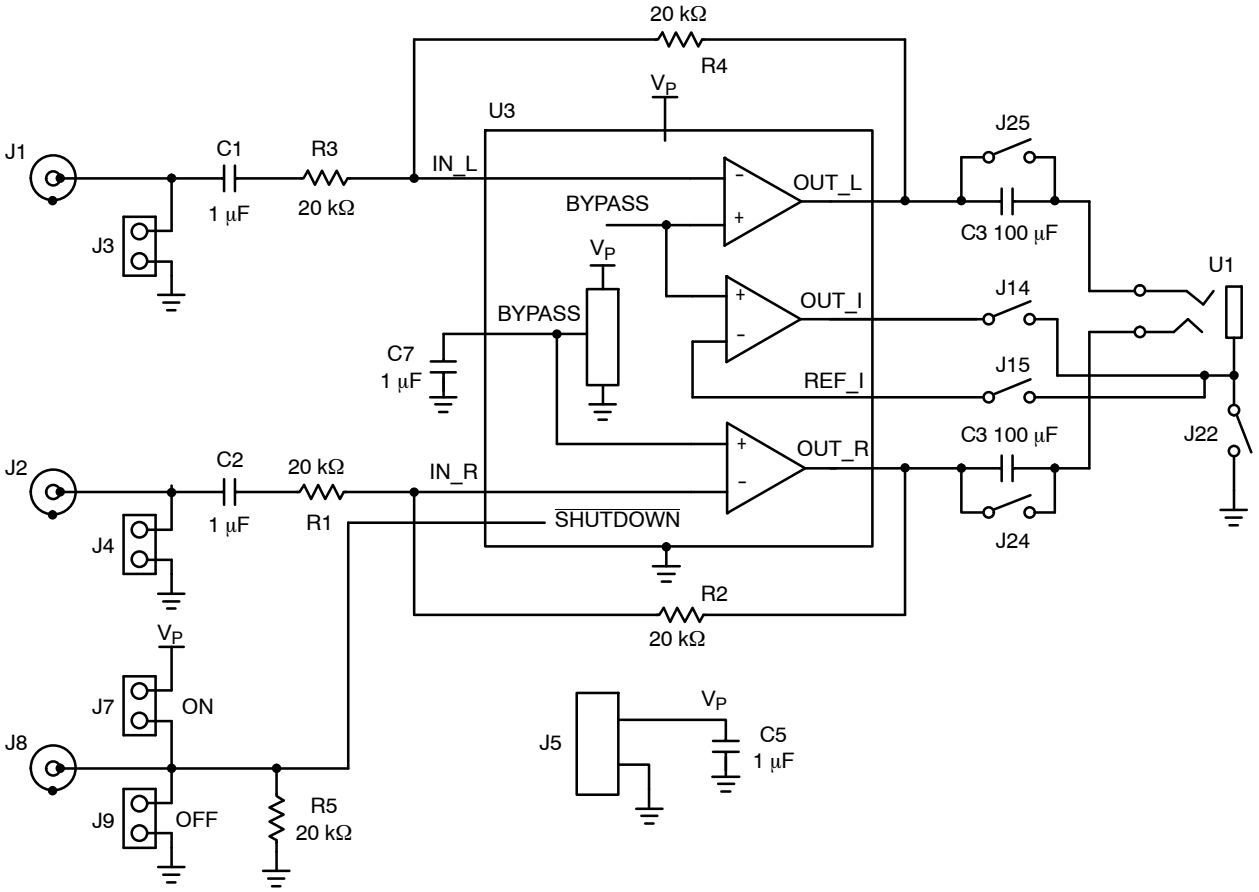


Figure 46. Schematic of the Demonstration Board for UDFN10 Device

Table 1. Bill of Material − Micro10

Item	Part Description	Ref.	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP2809 Audio Amplifier	U1,U3	Micro10	ON Semiconductor	NCP2809
2	SMD Resistor 100 KΩ	R1,R2	0805	Vishay−Draloric	D12CRCW Series
3	Ceramic Capacitor 390 nF 50 V Z5U	C2,C4, C6,C8	1812	Kemet	C1812C394M5UAC
4	Ceramic Capacitor 1.0 μF 16 V X7R Optimized Performance	C1,C3, C5,C7	1206	Murata	GRM42−6X7R105K16
5	Tantalum Capacitor 220 μF 10 V	C9,C10	−	Kemet	T495X227010AS
6	I/O Connector. It can be plugged by BLZ5.08/2 (Weidmüller Reference)	J4,J10	−	Weidmüller	SL5.08/2/90B
7	I/O Connector. It can be plugged by BLZ5.08/3 (Weidmüller Reference)	J2,J3, J8,J9	−	Weidmüller	SL5.08/3/90B
8	3.5 mm PCB Jack Connector	U2,U4	−	Decelect−Forgos	IES 101−3
9	Jumper Header Vertical Mount 2*1, 2.54 mm	J1,J7	−	−	−

Table 2. Bill of Material − UDFN10

Item	Part Description	Ref.	PCB Footprint	Manufacturer	Manufacturer Part Number
1	Stereo Headphone Amplifier	U1	UDFN10 3x3	ON Semiconductor	NCP2809B
2	Thick Film Chip Resistor	R1−R5	0805	Vishay	CRCW08052022FNEA
3	Ceramic Chip Capacitor	C1,C2,C5,C7	0805	TDK	C2012X7R1C105K
4	PCB Header, 2 Poles	J5	NA	Phoenix	MSTBA 2,5/2−G
5	SMB Connector	J1,J2,J8	NA	RS	RS 546−3406
6	3.5 mm PCB Jack Connector	U2	NA	CUI Inc	SJ−3515N
7	Short Connector	J14,J15	NA	NA	NA
8	Short Connector	J24,J25	NA	NA	NA

PCB LAYOUT GUIDELINES

How to Optimize the Accuracy of VMC

The main innovation of the NCP2809 stereo NOCAP audio amplifier is the use of a virtual ground that allows connecting directly the headset on the outputs of the device saving DC−blocking output capacitors. In order to have the best performances in terms of crosstalk, noise and supply current, the feedback connection on the virtual ground amplifier is not closed internally. To reach this goal of excellence, one must connect OUT_I and REF_I as close as possible from the middle point of the output jack connector. The most suitable place for this connection is directly on the pad of this middle point.

How to Optimize THD+N Performances

To get the best THD+N level on the headset speakers, the traces of the power supply, ground, OUT_R, OUT_L and OUT_I need the lowest resistance. Thus, the PCB traces for these nets should be as wide and short as possible.

You need to avoid ground loops, run digital and analog traces parallel to each other. Due to its internal structure, the amplifier can be sensitive to coupling capacitors between Ground and each output (OUT_R, OUT_L and OUT_I). Avoid running the output traces between two ground layers or if traces must cross over on different layers, do it at 90 degrees.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP2809ADMR2	MAE	Micro10	4000/Tape & Reel
NCP2809ADMR2G	MAE	Micro10 (Pb−Free)	4000/Tape & Reel
NCP2809BDMR2	MAC	Micro10	4000/Tape & Reel
NCP2809BDMR2G	MAC	Micro10 (Pb−Free)	4000/Tape & Reel
NCP2809BMUTXG	2809B	UDFN10 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

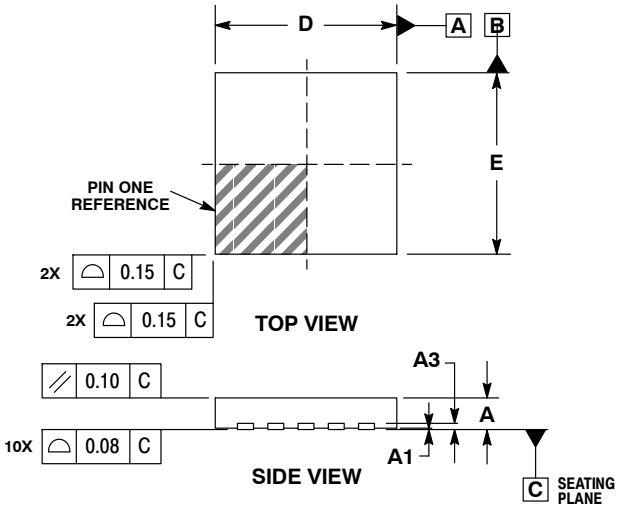
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

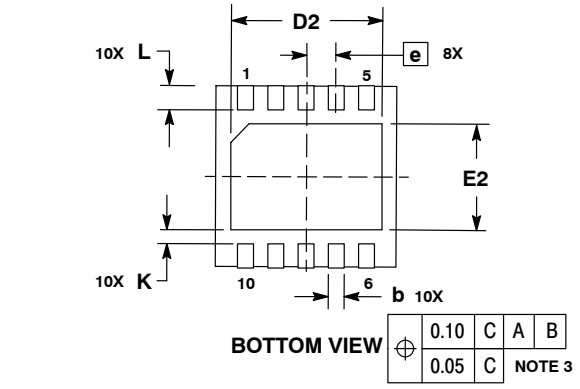
ON Semiconductor®

UDFN10 3x3, 0.5P
CASE 506AT−01
ISSUE A

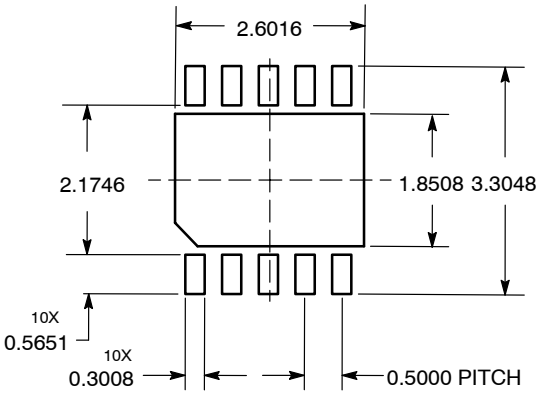
DATE 29 JUN 2007

SCALE 2:1





SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.19 TYP	
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*

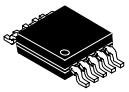
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON21330D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN10 3X3, 0.5P**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

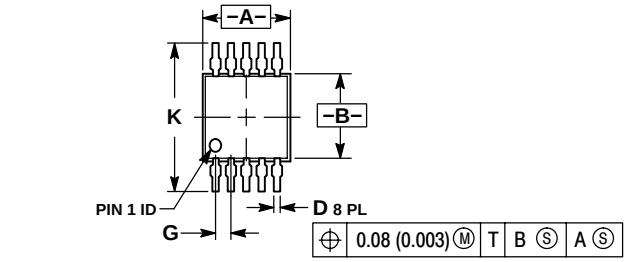
ON Semiconductor®

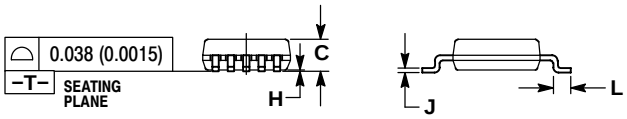


SCALE 2:1

Micro10
CASE 846B−03
ISSUE D

DATE 07 DEC 2004

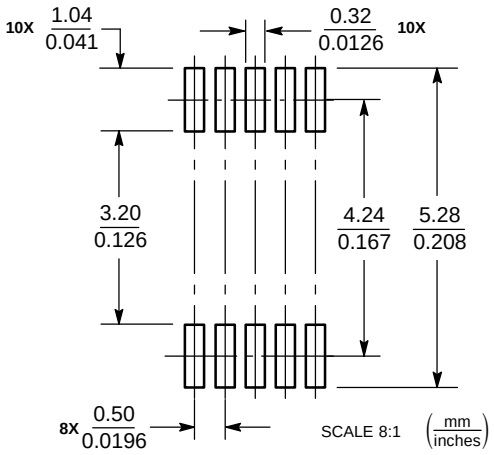




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT



Micro10

GENERIC MARKING DIAGRAM*

xxxx = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON03799D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	Micro10		PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ BY J. HOSKINS.	09 NOV 2000
A	DIM “D” WAS 0.25−0.4MM/0.10−0.016IN. ADDED NOTE 5. USED ON: WAS 10 LEAD TSSOP, PITCH 0.65 REQ BY J. HOSKINS.	13 NOV 2000
B	CHANGED “USED ON” WAS: 10 LEAD TSSOP, PITCH 0.50MM. REQ BY A. HAMID.	11 JUL 2001
C	CHANGED “D” DIMENSION MAX FROM 0.35 TO 0.30MM AND 0.014 TO 0.012IN. REQ BY D. TRUHITTE.	31 JUL 2003
D	ADDED FOOTPRINT INFORMATION. REQ. BY K. OPPEN.	07 DEC 2004

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