

# 4.5 V to 36 V Input, 5 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

## BD9F500QUZ

### General Description

BD9F500QUZ is a synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. It is capable of providing current up to 5 A. It features fast transient response due to Constant On-Time control system. The Light Load Mode control improves efficiency in light-load conditions. It is ideal for reducing standby power consumption of equipment. Power Good function makes it possible for system to control sequence. It achieves the high power density and offer a small footprint on the PCB by employing small package.

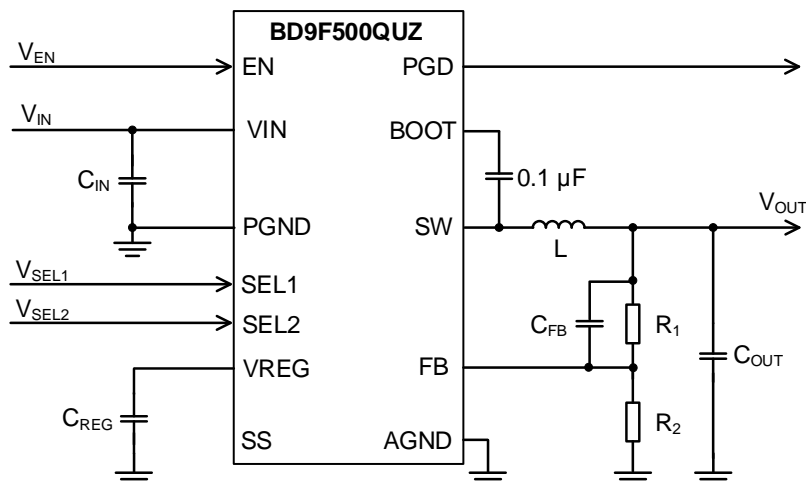
### Features

- Single Synchronous Buck DC/DC Converter
- Constant On-Time Control
- Light Load Mode Control
- Adjustable Soft Start
- Power Good Output
- Nano Pulse Control™
- Output Capacitor Discharge Function
- Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Short Circuit Protection (SCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lockout Protection (UVLO)
- VMMP16LZ3030 Package
- Backside Heat Dissipation, 0.5 mm Pitch

### Applications

- Step-down Power Supply for SoC, FPGA, Microprocessor
- Printer (MFP / LBP / IJP / POS)
- OA Equipment
- Laptop PC
- USB Type-C Applications

### Typical Application Circuit



### Key Specifications

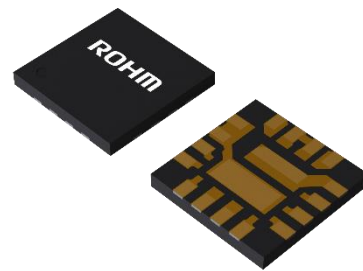
- Input Voltage Range: 4.5 V to 36 V
- Output Voltage Range: 0.6 V to 14 V
- Output Current: 5 A (Max)
- Switching Frequency: 600 kHz, 1 MHz, 2.2 MHz (Typ)
- High-Side FET ON Resistance: 40 mΩ (Typ)
- Low-Side FET ON Resistance: 22 mΩ (Typ)
- Shutdown Current: 2 μA (Typ)
- Operating Quiescent Current: 20 μA (Typ)

### Package

VMMP16LZ3030

W (Typ) x D (Typ) x H (Max)

3.0 mm x 3.0 mm x 0.40 mm

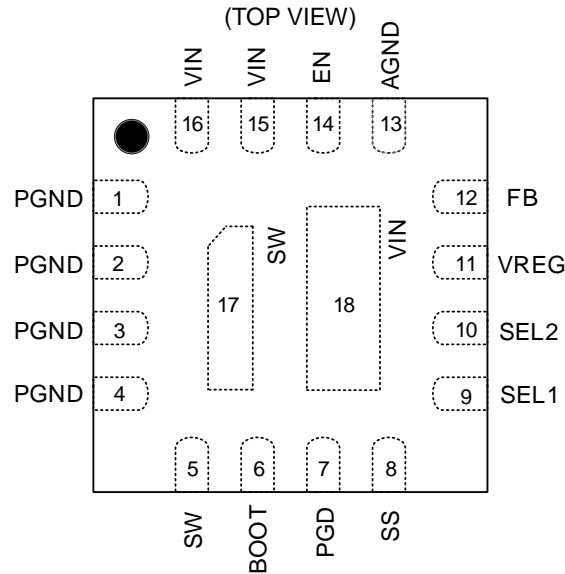


VMMP16LZ3030

Nano Pulse Control™ is a trademark or a registered trademark of ROHM Co., Ltd.

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

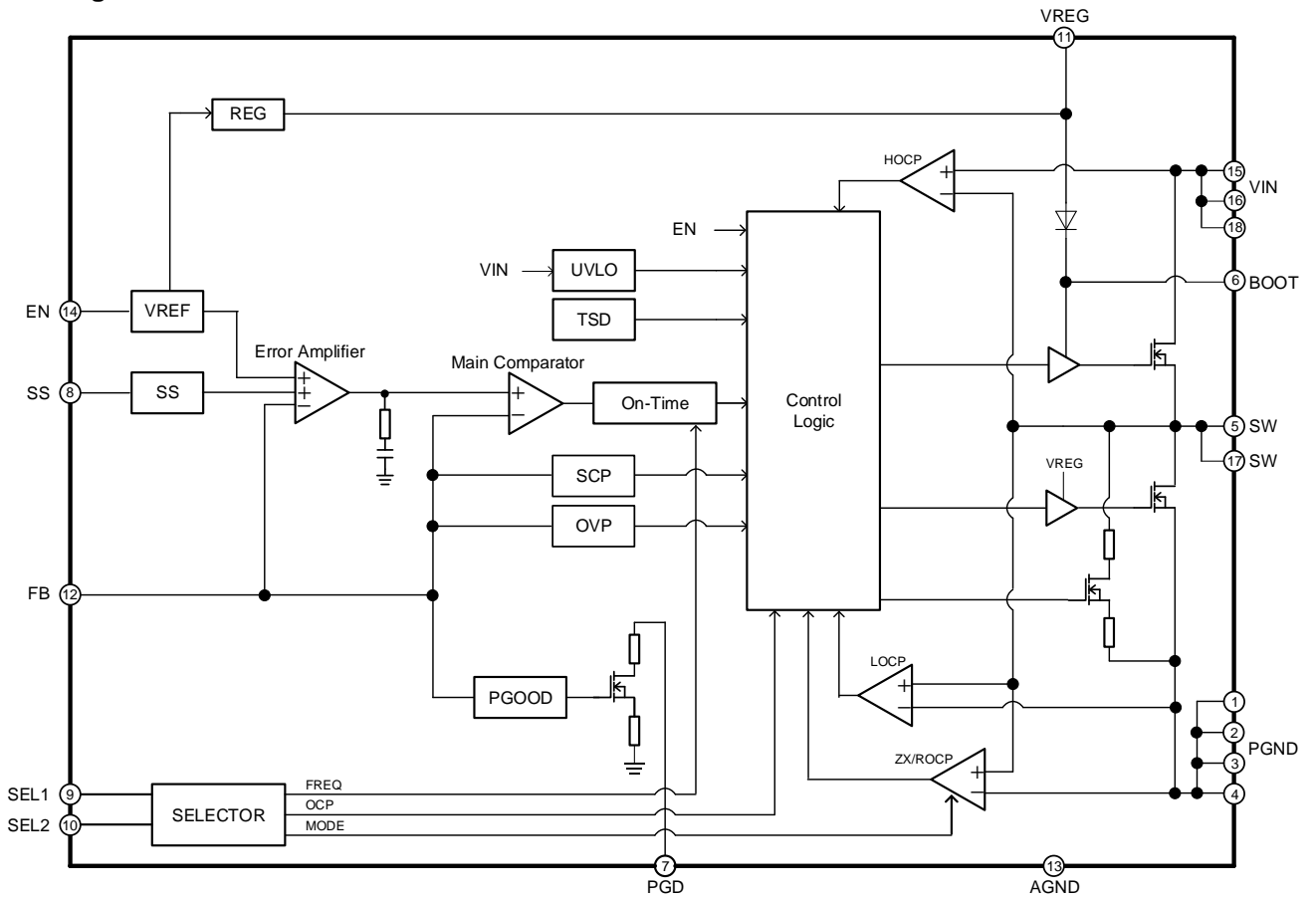
## Pin Configuration



## Pin Descriptions

Pin No.	Pin Name	Function
1-4	PGND	Ground pins for the output stage of the switching regulator.
5, 17	SW	Switch pin. This pin is connected to the source of the High-Side FET and the drain of the Low-Side FET. Connect a bootstrap capacitor of 0.1 $\mu\text{F}$ between this pin and the BOOT pin. In addition, connect an inductor considering the direct current superimposition characteristic.
6	BOOT	Pin for bootstrap. Connect a bootstrap capacitor of 0.1 $\mu\text{F}$ between this pin and the SW pin. The voltage of this pin is the gate drive voltage of the High-Side FET.
7	PGD	Power Good pin. This pin is an open drain output that requires a pull-up resistor. See <a href="#">Function Explanations (4) Power Good</a> for setting the resistance. If not used, this pin can be left floating or connected to the ground.
8	SS	Pin for setting the soft start time of output voltage. The soft start time is 2 ms (Typ) when the SS pin is open. A ceramic capacitor connected to the SS pin makes the soft start time more than 2 ms. See <a href="#">Selection of Components Externally Connected 4. Soft Start Capacitor</a> for how to calculate the capacitance.
9	SEL1	Pin for setting switching control mode. See <a href="#">Function Explanations (7) Control Mode Selectable Function</a> for how to control.
10	SEL2	Pin for setting switching control mode. See <a href="#">Function Explanations (7) Control Mode Selectable Function</a> for how to control.
11	VREG	Internal power supply output pin. This node supplies power 5.2 V (Typ) to other blocks which are mainly responsible for the control function of the switching regulator. Connecting 2.2 $\mu\text{F}$ (Typ) ceramic capacitor is recommended.
12	FB	Output voltage feedback pin. See <a href="#">Selection of Components Externally Connected 3. Output Voltage Setting, FB Capacitor</a> for the output voltage setting.
13	AGND	Ground pin for the control circuit.
14	EN	Enable pin. The device starts up with setting $V_{\text{EN}}$ to 1.2 V (Typ) or more. The device enters the shutdown mode with setting $V_{\text{EN}}$ to 1.1 V (Typ) or less. This pin must be terminated.
15, 16, 18	VIN	Power supply pin. Connecting 0.1 $\mu\text{F}$ (Typ) and 10 $\mu\text{F}$ (Typ) ceramic capacitors is recommended. The detail of a selection is described in <a href="#">Selection of Components Externally Connected 1. Input Capacitor</a> . Connecting to the PCB VIN pattern by using thermal vias provides excellent heat dissipation characteristics. See <a href="#">PCB Layout Design</a> for the detailed PCB layout design.

Block Diagram



## Description of Blocks

1. VREF  
This block generates the internal reference voltage.
2. REG  
This block generates the internal power supply.
3. Soft Start  
The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. The internal soft start time is 2 ms (Typ) when the SS pin is open. A capacitor connected to the SS pin makes the rising time more than 2 ms.
4. Error Amplifier  
The Error Amplifier adjusts the Main Comparator input voltage to make the internal reference voltage equal to FB voltage.
5. Main Comparator  
The Main Comparator compares the Error Amplifier output voltage and FB voltage ( $V_{FB}$ ). When  $V_{FB}$  becomes lower than the Error Amplifier output voltage, the output turns high and reports to the On-Time block that the output voltage has dropped below the control voltage.
6. On-Time  
This block generates On-Time. The designed On-Time is generated after the Main Comparator output turns high.
7. PGOOD  
The PGOOD block is for power good function. When the output voltage reaches within  $\pm 7\%$  (Typ) of the setting voltage, the built-in open drain Nch MOSFET connected to the PGD pin is turned off and the PGD pin becomes Hi-Z (High impedance). When the output voltage reaches outside  $\pm 10\%$  (Typ) of the setting voltage, the open drain Nch MOSFET is turned on and PGD pin is pulled down with 500  $\Omega$  (Typ).
8. UVLO  
The UVLO block is for under voltage lockout protection. The device is shutdown when input voltage ( $V_{IN}$ ) falls to 4.0 V (Typ) or less. The threshold voltage has the 200 mV (Typ) hysteresis.
9. TSD  
The TSD block is for thermal protection. The device is shutdown when the junction temperature  $T_j$  reaches to 175  $^{\circ}\text{C}$  (Typ) or more. The device is automatically restored to normal operation with a hysteresis of 25  $^{\circ}\text{C}$  (Typ) when the  $T_j$  goes down.
10. OVP  
The OVP block is for output over voltage protection. When the FB voltage ( $V_{FB}$ ) exceeds 120 % (Typ) or more of FB threshold voltage  $V_{FBTH}$ , the SW pin is pulled down with 400  $\Omega$  (Typ). After  $V_{FB}$  falls 115 % (Typ) or less of  $V_{FBTH}$ , the device is returned to normal operation condition.
11. HOCP  
This block is for over current protection of the High-Side FET. When the current that flows through the High-Side FET reaches the value of over current limit, it turns off the High-Side FET and turns on the Low-Side FET.
12. LOCP  
This block is for over current protection of the Low-Side FET. While the current that flows through the Low-Side FET over the value of over current limit, the condition that being turned on the Low-Side FET is continued.
13. SCP  
This block is for short circuit protection. After soft start is completed and in condition where  $V_{FB}$  is 90 % (Typ) of 0.6 V or less, this block counts the number of times of which current flowing in the Low-Side FET reaches over current limit. When 128 times is counted, the device is shutdown for 16 times of soft start time (Typ) and re-operates.
14. ZX/ROCP  
The ZX/ROCP is a comparator that monitors the inductor current. When inductor current falls below 0 A (Typ) while the Low-Side FET is on, it turns off the Low-Side FET (Light Load Mode). When the current that flows through the Low-Side FET reaches the value of over current limit, it turns off the Low-Side FET (Fixed PWM Mode).
15. Control Logic  
The Control Logic controls the switching operation and protection function operation.
16. SELECTOR  
This block controls switching frequency, maximum output current, and operating mode.

## Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Input Voltage	V <sub>IN</sub>	-0.3 to +39	V
SW Voltage	V <sub>SW</sub>	-0.3 to V <sub>IN</sub> + 0.3	V
SW Voltage (3 ns pulse width)	V <sub>SWAC1</sub>	-2 to V <sub>IN</sub> + 0.3	V
SW Voltage (30 ns pulse width)	V <sub>SWAC2</sub>	-1 to V <sub>IN</sub> + 0.3	V
Voltage from GND to BOOT	V <sub>BOOT</sub>	-0.3 to +45	V
Voltage from SW to BOOT	ΔV <sub>BOOT-SW</sub>	-0.3 to +7	V
FB Voltage	V <sub>FB</sub>	-0.3 to +7	V
VREG Voltage	V <sub>VREG</sub>	-0.3 to +7	V
SEL1 Voltage	V <sub>SEL1</sub>	-0.3 to V <sub>VREG</sub> + 0.3	V
SEL2 Voltage	V <sub>SEL2</sub>	-0.3 to V <sub>VREG</sub> + 0.3	V
PGD Voltage	V <sub>PGD</sub>	-0.3 to +45	V
EN Voltage	V <sub>EN</sub>	-0.3 to +39	V
SS Voltage	V <sub>SS</sub>	-0.3 to +7	V
Output Current	I <sub>OUT</sub>	6	A
Maximum Junction Temperature	T <sub>jmax</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance <sup>(Note 1)</sup>

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
VMMP16LZ3030				
Junction to Ambient	θ <sub>JA</sub>	125.1	50.7	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	12	8	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note 5)</sup>	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 5) This thermal via connects with the copper pattern of all layers.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V <sub>IN</sub>	4.5	-	36.0	V
Operating Temperature <sup>(Note 1)</sup>	Topr	-40	-	+85	°C
Output Current <sup>(Note 1)/(Note 2)</sup>	I <sub>OUT</sub>	0	-	5	A
		0	-	3	A
Output Voltage Setting <sup>(Note 3)</sup>	V <sub>OUT</sub>	0.6	-	14.0	V

(Note 1) T<sub>j</sub> must be 150 °C or less under the actual operating environment. Life time is derated at junction temperature greater than 125 °C.

(Note 2) The maximum value of the output current is determined by the control mode selection.

(Note 3) The switching frequency is reduced as needed to always ensure a proper regulation at low duty and high duty cycles. Use under the condition of V<sub>OUT</sub> ≤ V<sub>IN</sub> × 0.8 [V].

Electrical Characteristics (Unless otherwise specified Ta = 25 °C, V<sub>IN</sub> = 12 V, V<sub>EN</sub> = 3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Input Supply</b>						
Shutdown Current	I <sub>SDN</sub>	-	2	10	μA	V <sub>EN</sub> = 0 V
Operating Quiescent Current	I <sub>Q</sub>	-	20	40	μA	I <sub>OUT</sub> = 0 A, No switching
UVLO Detection Threshold Voltage	V <sub>UVLO1</sub>	3.7	4.0	4.3	V	V <sub>IN</sub> falling
UVLO Release Threshold Voltage	V <sub>UVLO2</sub>	3.9	4.2	4.5	V	V <sub>IN</sub> rising
UVLO Hysteresis Voltage	V <sub>UVLOHYS</sub>	100	200	400	mV	
<b>Enable</b>						
EN Threshold Voltage High	V <sub>ENH</sub>	1.1	1.2	1.3	V	V <sub>EN</sub> rising
EN Threshold Voltage Low	V <sub>ENL</sub>	1.0	1.1	1.2	V	V <sub>EN</sub> falling
EN Hysteresis Voltage	V <sub>ENHYS</sub>	50	100	200	mV	
EN Input Current	I <sub>EN</sub>	-	0	2	μA	V <sub>EN</sub> = 3 V
<b>VREG</b>						
VREG Shutdown Voltage	V <sub>VREG_SD</sub>	-	0	0.1	V	V <sub>EN</sub> = 0 V
VREG Output Voltage	V <sub>VREG</sub>	5.0	5.2	5.4	V	
<b>Reference Voltage, Error Amplifier, Soft Start</b>						
FB Threshold Voltage	V <sub>FBTH</sub>	0.594	0.600	0.606	V	PWM mode
FB Input Current	I <sub>FB</sub>	-	-	100	nA	V <sub>FB</sub> = 0.6 V
Soft Start Time	t <sub>SS</sub>	1.4	2.0	2.6	ms	The SS pin is open.
Soft Start Charge Current	I <sub>SS</sub>	1.6	2.0	2.4	μA	
<b>Control</b>						
SEL1, SEL2 High Level Voltage	V <sub>SELH</sub>	V <sub>VREG</sub> -0.3	-	V <sub>VREG</sub>	V	
SEL1, SEL2 Low Level Voltage	V <sub>SELL</sub>	0	-	0.3	V	
SEL1, SEL2 Input Current	I <sub>SEL</sub>	-	-	3	μA	
On-Time1	t <sub>ON1</sub>	-	458	-	ns	V <sub>OUT</sub> = 3.3 V, PWM mode, 600 kHz setting
On-Time2	t <sub>ON2</sub>	-	275	-	ns	V <sub>OUT</sub> = 3.3 V, PWM mode, 1 MHz setting
On-Time3	t <sub>ON3</sub>	-	125	-	ns	V <sub>OUT</sub> = 3.3 V, PWM mode, 2.2 MHz setting
Minimum On-Time <sup>(Note 4)</sup>	t <sub>MINON</sub>	-	48	-	ns	
<b>SW (MOSFET)</b>						
High-Side FET ON Resistance1	R <sub>ONH1</sub>	-	40	80	mΩ	V <sub>BOOT</sub> - V <sub>SW</sub> = 5 V, I <sub>OUTMAX</sub> = 5 A setting
High-Side FET ON Resistance2	R <sub>ONH2</sub>	-	65	130	mΩ	V <sub>BOOT</sub> - V <sub>SW</sub> = 5 V, I <sub>OUTMAX</sub> = 3 A setting
Low-Side FET ON Resistance1	R <sub>ONL1</sub>	-	22	44	mΩ	I <sub>OUTMAX</sub> = 5 A setting
Low-Side FET ON Resistance2	R <sub>ONL2</sub>	-	38	76	mΩ	I <sub>OUTMAX</sub> = 3 A setting

(Note 4) No tested on outgoing inspection.

Electrical Characteristics – continued (Unless otherwise specified Ta = 25 °C, V<sub>IN</sub> = 12 V, V<sub>EN</sub> = 3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Power Good</b>						
Power Good Rising Threshold Voltage	V <sub>PGDTHGR</sub>	90	93	96	%	V <sub>FB</sub> rising, V <sub>PGDTHGR</sub> = V <sub>FB</sub> / V <sub>FBTH</sub> X 100
Power Good Falling Threshold Voltage	V <sub>PGDTHGF</sub>	104	107	110	%	V <sub>FB</sub> falling, V <sub>PGDTHGF</sub> = V <sub>FB</sub> / V <sub>FBTH</sub> X 100
Power Fault Rising Threshold Voltage	V <sub>PGDTHFR</sub>	107	110	113	%	V <sub>FB</sub> rising, V <sub>PGDTHFR</sub> = V <sub>FB</sub> / V <sub>FBTH</sub> X 100
Power Fault Falling Threshold Voltage	V <sub>PGDTHFF</sub>	87	90	93	%	V <sub>FB</sub> falling, V <sub>PGDTHFF</sub> = V <sub>FB</sub> / V <sub>FBTH</sub> X 100
PGD Output Leakage Current	I <sub>LKPGD</sub>	-	0	1	μA	V <sub>PGD</sub> = 5 V
PGD MOSFET ON Resistance	R <sub>PGD</sub>	-	500	1000	Ω	
<b>Protection</b>						
Low-Side FET Over Current Detection Current 1 <sup>(Note 1)</sup>	I <sub>LOCP1</sub>	5.3	6.7	8.1	A	I <sub>OUTMAX</sub> = 5 A setting
Low-Side FET Over Current Detection Current 2 <sup>(Note 1)</sup>	I <sub>LOCP2</sub>	3.2	4.0	4.8	A	I <sub>OUTMAX</sub> = 3 A setting

(Note 1) No tested on outgoing inspection.

Typical Performance Curves

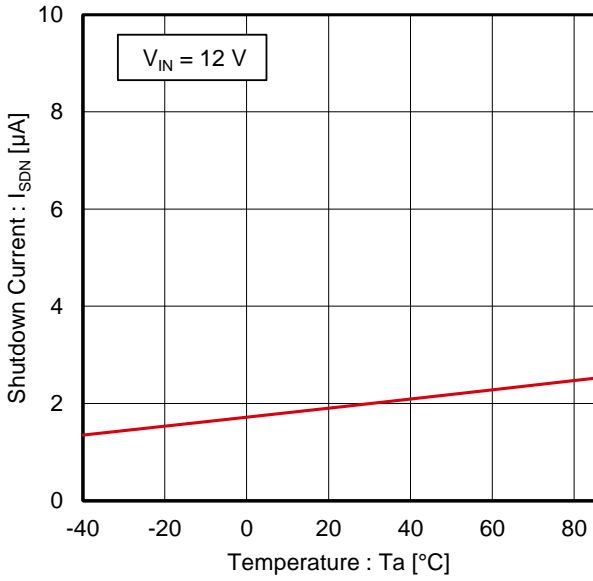


Figure 1. Shutdown Current vs Temperature

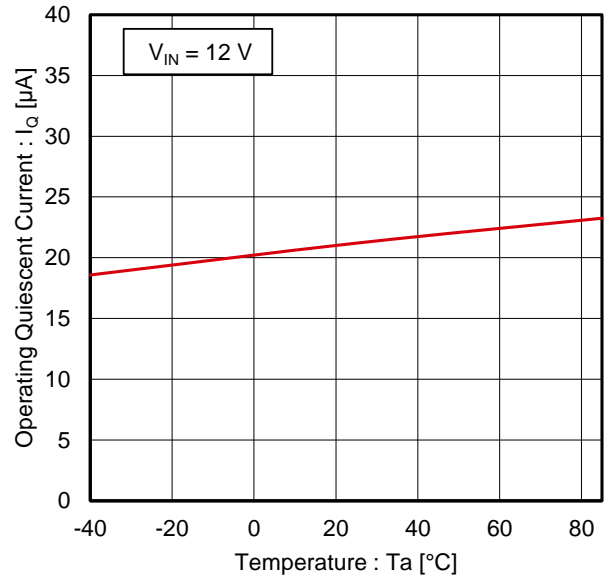


Figure 2. Operating Quiescent Current vs Temperature

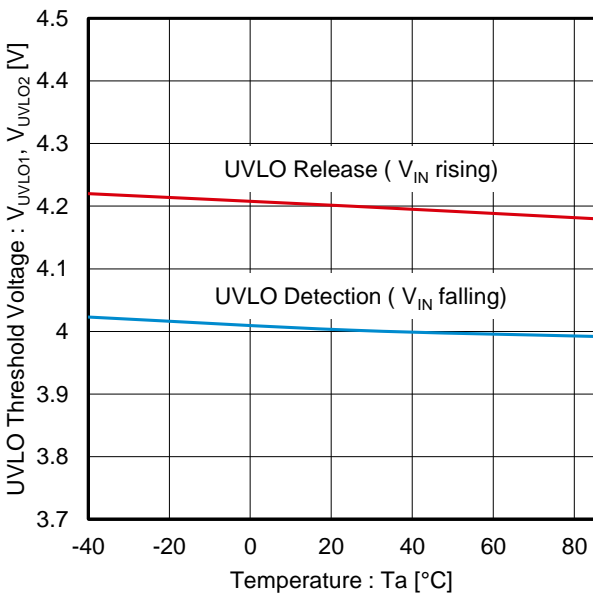


Figure 3. UVLO Threshold Voltage vs Temperature

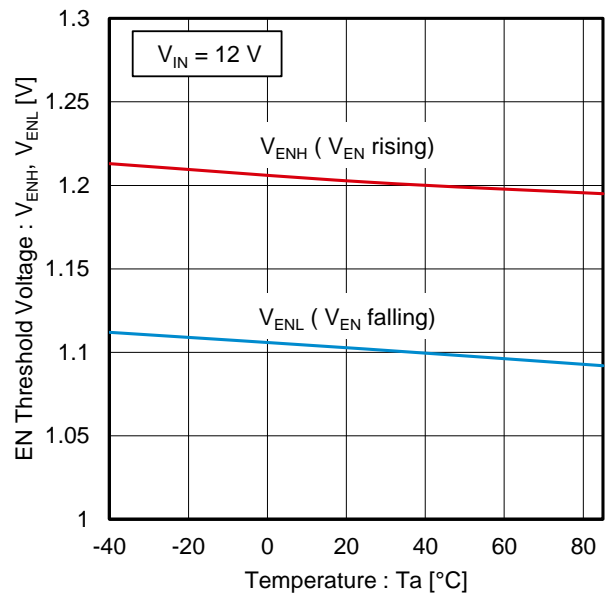


Figure 4. EN Threshold Voltage vs Temperature



Typical Performance Curves – continued

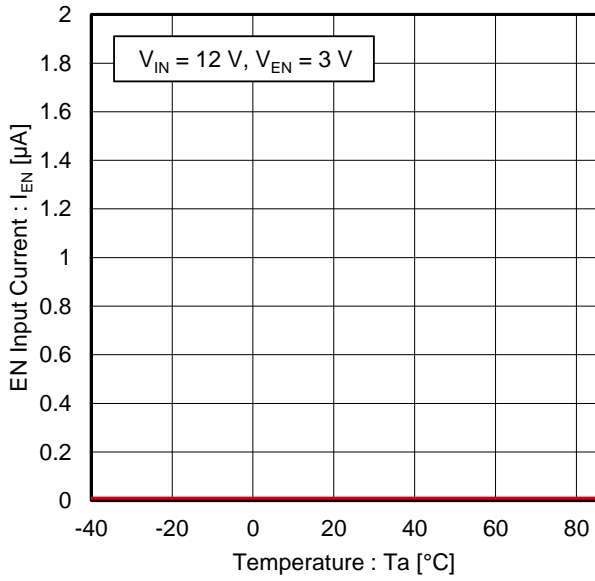


Figure 5. EN Input Current vs Temperature

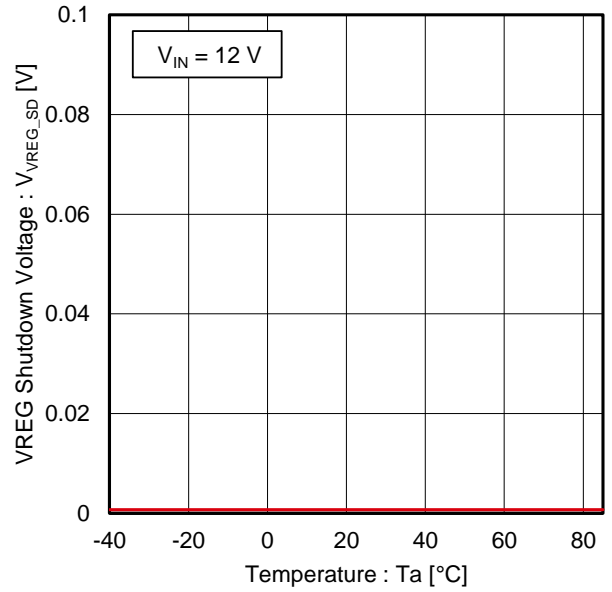


Figure 6. VREG Shutdown Voltage vs Temperature

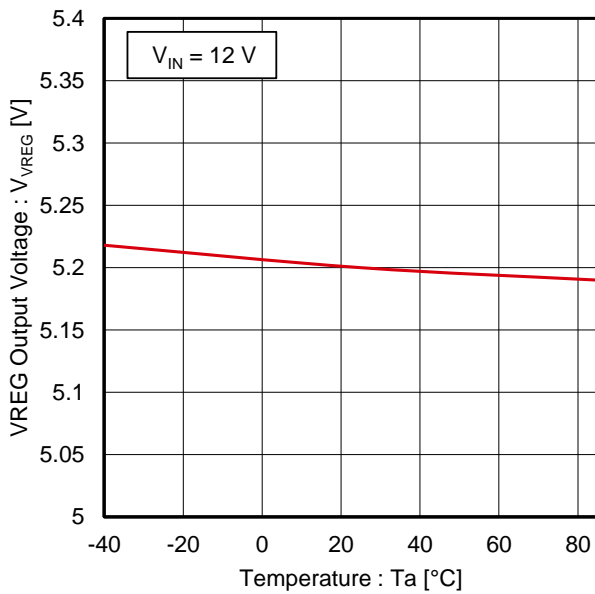


Figure 7. VREG Output Voltage vs Temperature

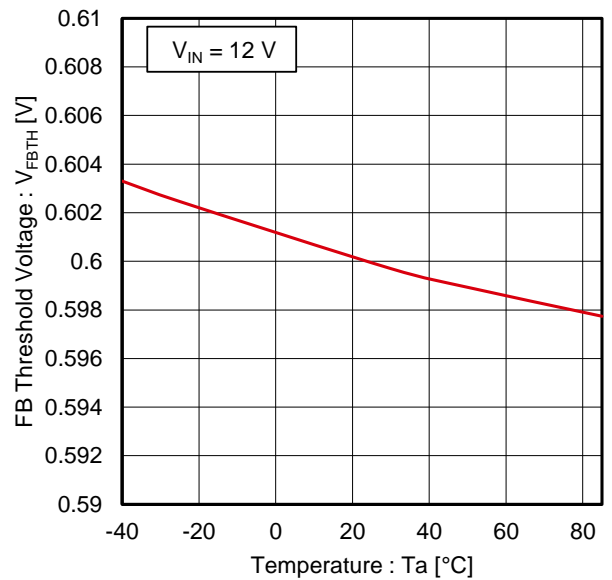


Figure 8. FB Threshold Voltage vs Temperature

Typical Performance Curves – continued

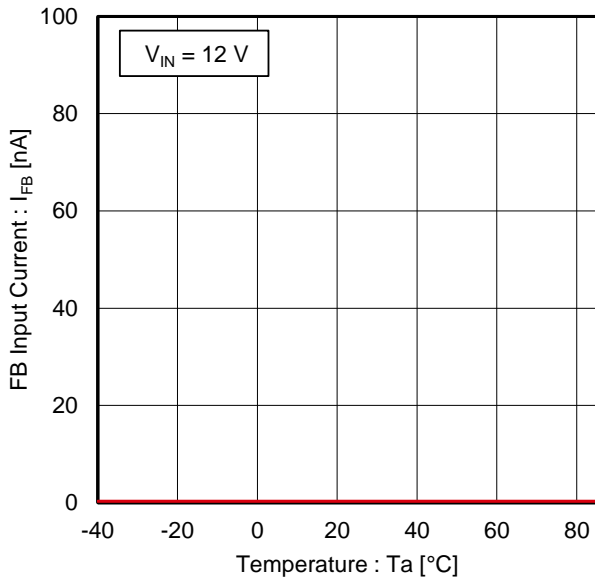


Figure 9. FB Input Current vs Temperature

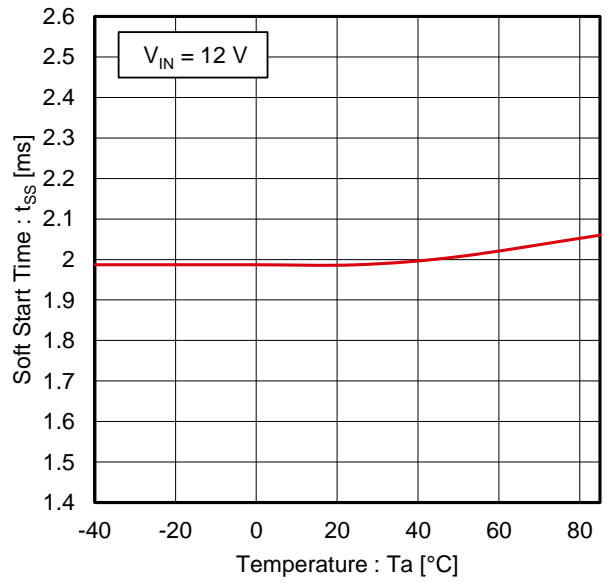


Figure 10. Soft Start Time vs Temperature

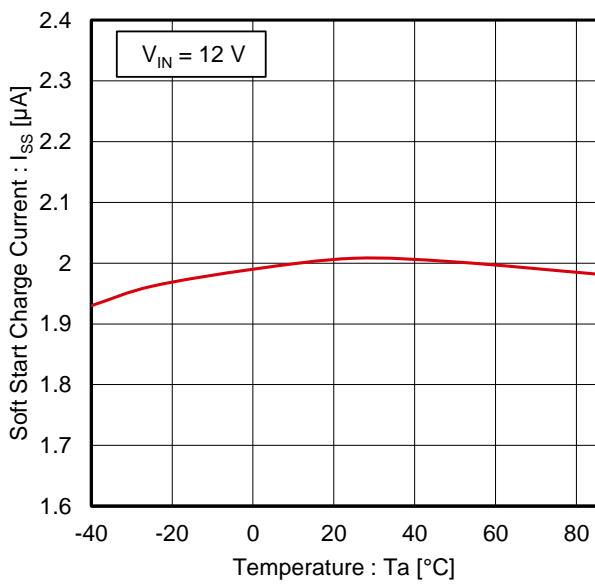


Figure 11. Soft Start Charge Current vs Temperature

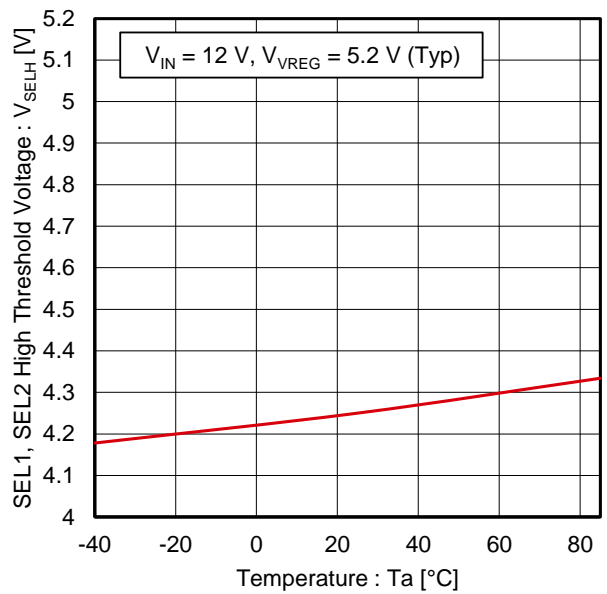


Figure 12. SEL1, SEL2 High Threshold Voltage vs Temperature

Typical Performance Curves – continued

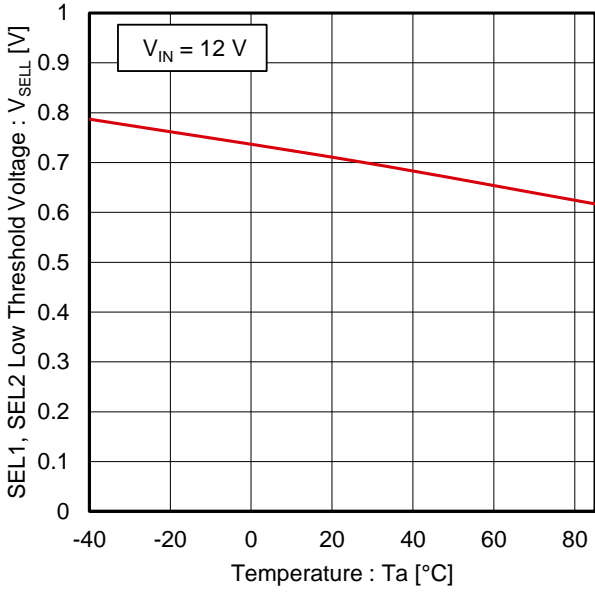


Figure 13. SEL1, SEL2 Low Threshold Voltage vs Temperature

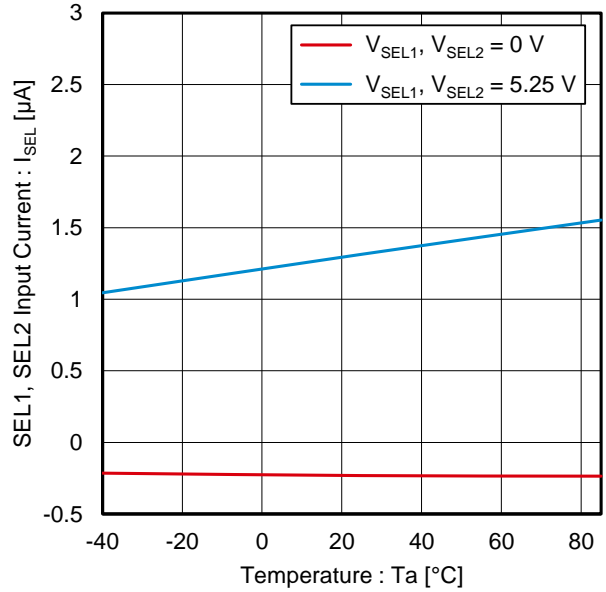


Figure 14. SEL1, SEL2 Input Current vs Temperature

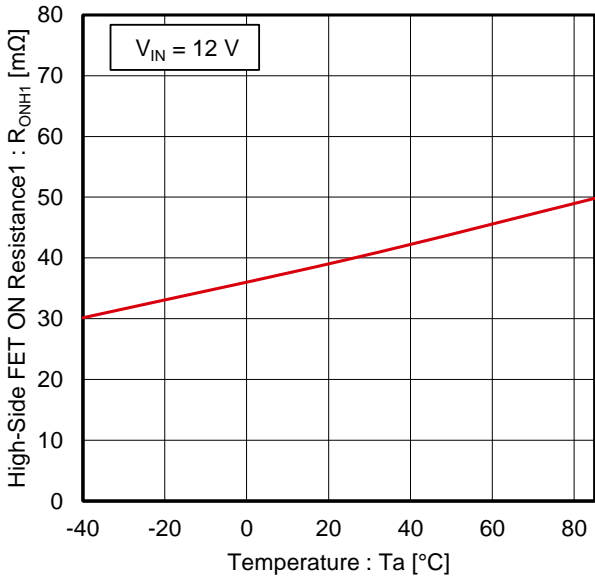


Figure 15. High-Side FET ON Resistance1 vs Temperature

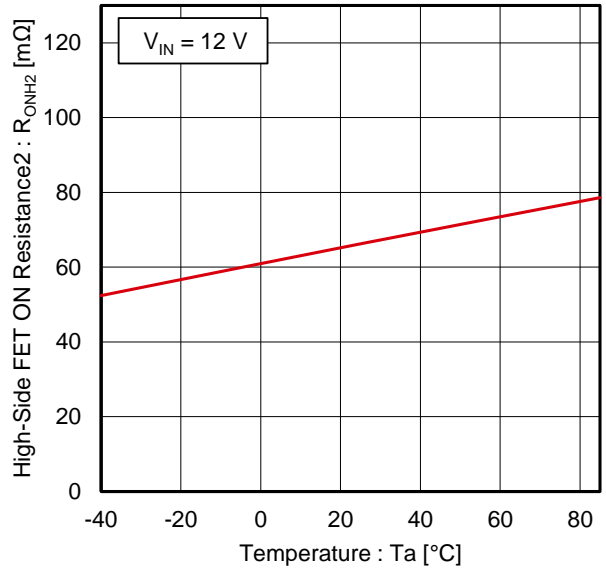


Figure 16. High-Side FET ON Resistance2 vs Temperature

Typical Performance Curves – continued

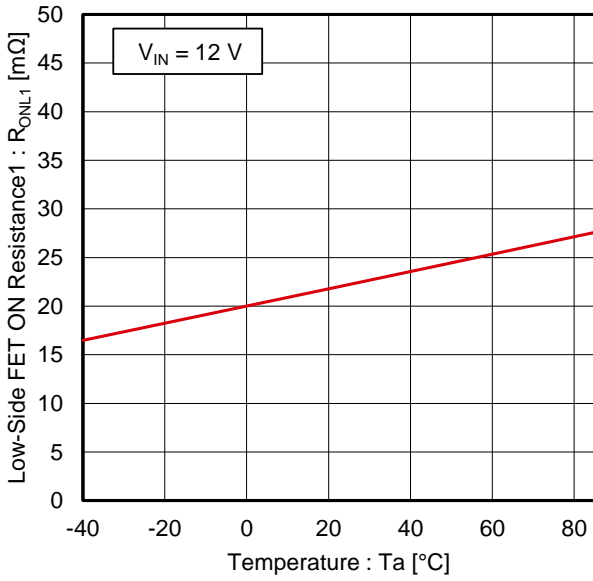


Figure 17. Low-Side FET ON Resistance1 vs Temperature

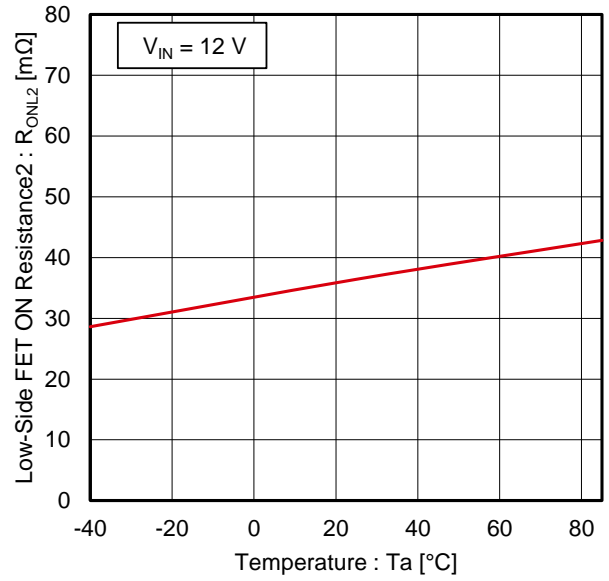


Figure 18. Low-Side FET ON Resistance2 vs Temperature

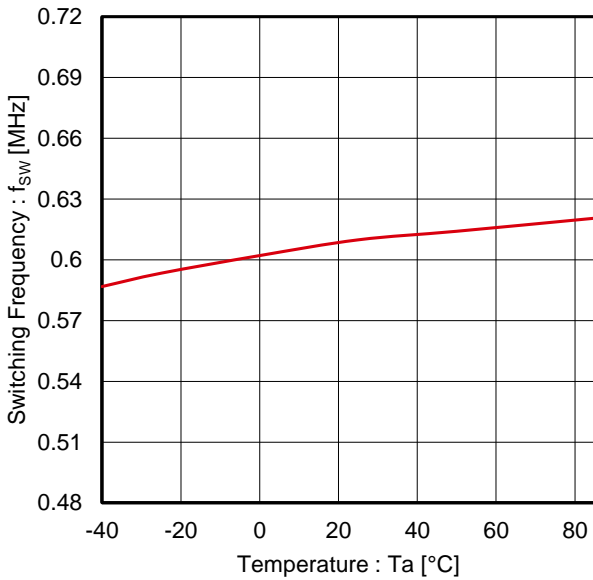


Figure 19. Switching Frequency vs Temperature  
(V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, I<sub>OUT</sub> = 2 A,  
600 kHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)

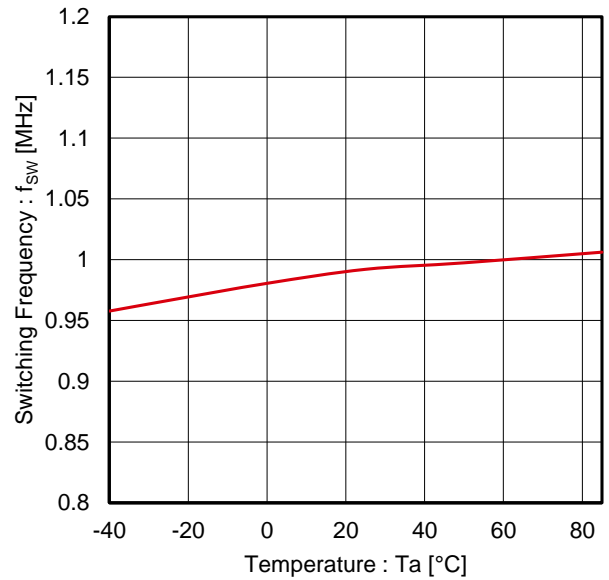


Figure 20. Switching Frequency vs Temperature  
(V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, I<sub>OUT</sub> = 2 A,  
1 MHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)

Typical Performance Curves – continued

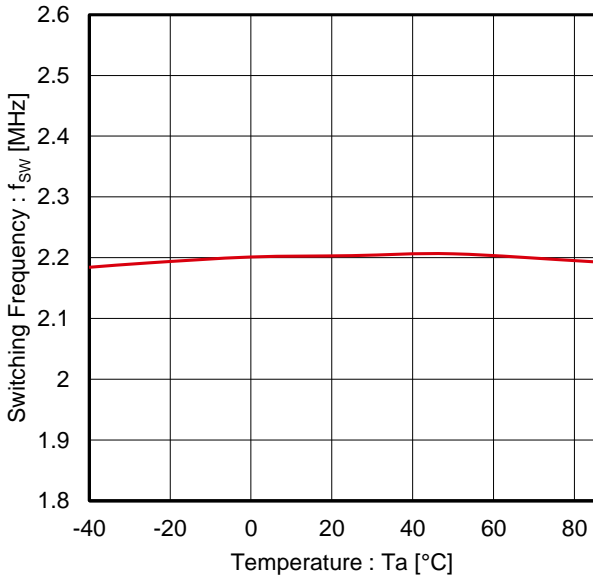


Figure 21. Switching Frequency vs Temperature ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$ , 2.2 MHz setting)

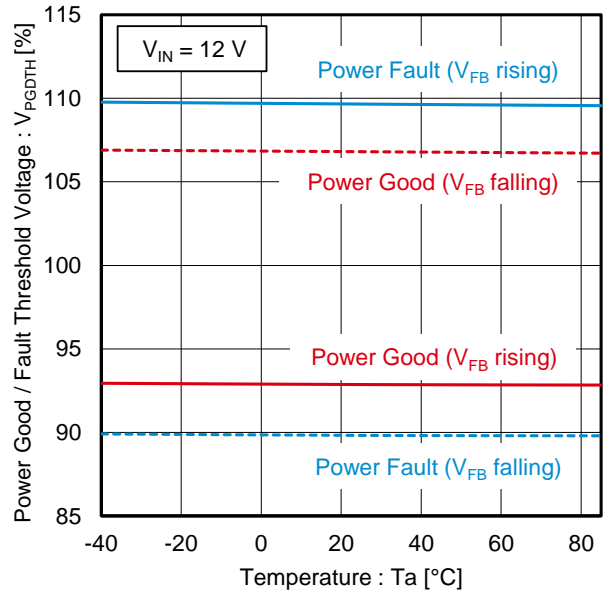


Figure 22. Power Good / Fault Threshold Voltage vs Temperature

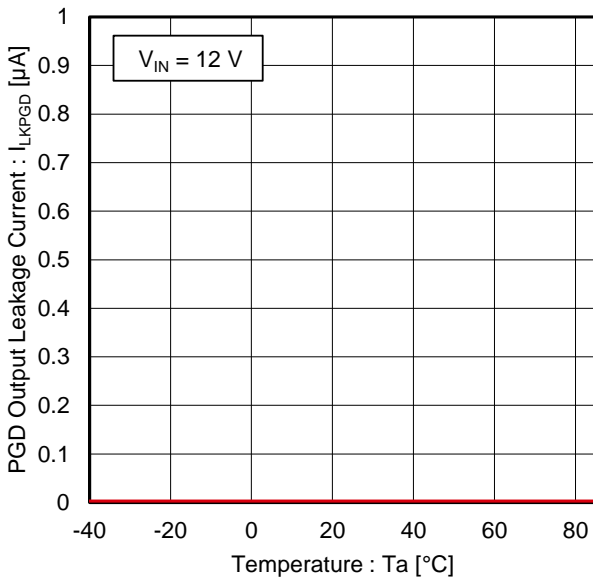


Figure 23. PGD Output Leakage Current vs Temperature

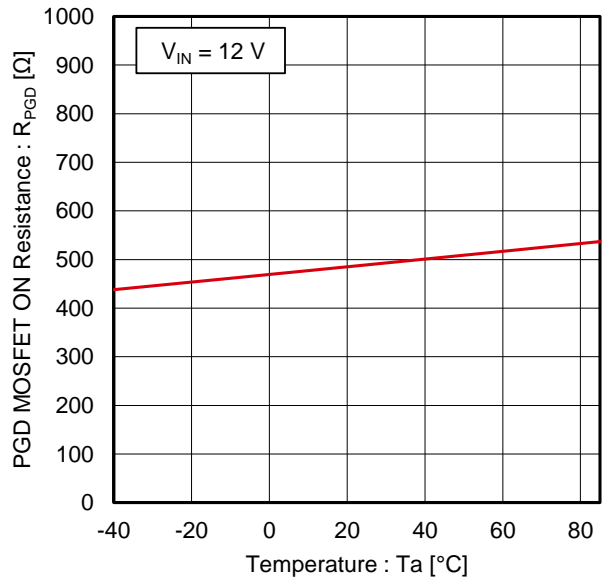


Figure 24. PGD MOSFET ON Resistance vs Temperature

Typical Performance Curves – continued

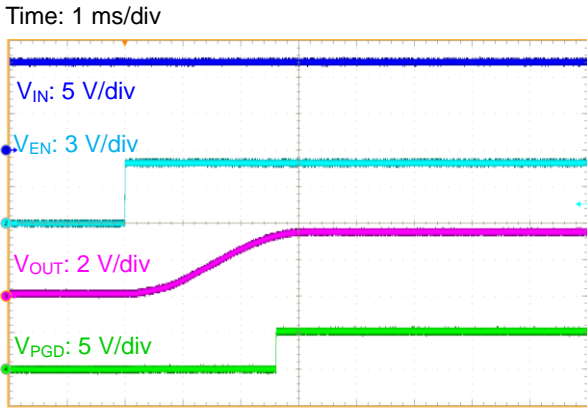


Figure 25. Start-up at No Load:  $V_{EN} = 0\text{ V}$  to  $5\text{ V}$   
 ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{SS} = \text{OPEN}$ ,  
 1 MHz\_ $I_{OUTMAX} = 5\text{ A\_LLM}$  setting)

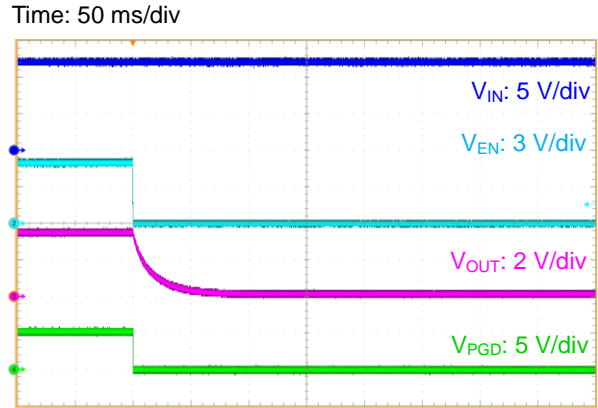


Figure 26. Shutdown at No Load:  $V_{EN} = 5\text{ V}$  to  $0\text{ V}$   
 ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{SS} = \text{OPEN}$ ,  
 1 MHz\_ $I_{OUTMAX} = 5\text{ A\_LLM}$  setting)

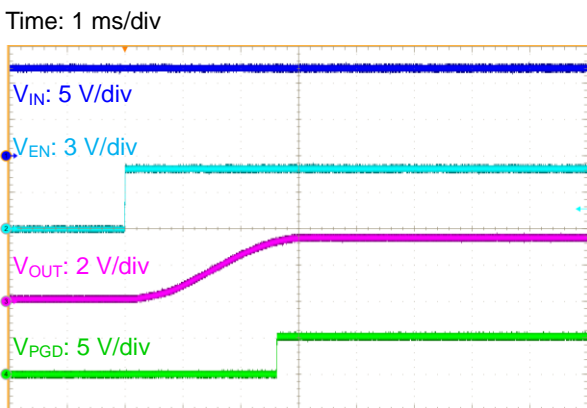


Figure 27. Start-up at  $R_{LOAD} = 0.66\ \Omega$ :  $V_{EN} = 0\text{ V}$  to  $5\text{ V}$   
 ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{SS} = \text{OPEN}$ ,  
 1 MHz\_ $I_{OUTMAX} = 5\text{ A\_LLM}$  setting)

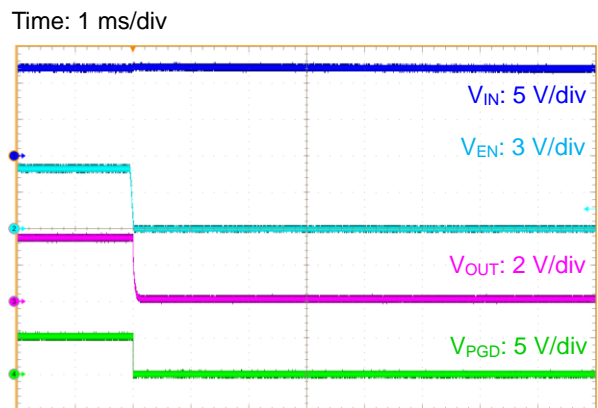


Figure 28. Shutdown at  $R_{LOAD} = 0.66\ \Omega$ :  $V_{EN} = 5\text{ V}$  to  $0\text{ V}$   
 ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{SS} = \text{OPEN}$ ,  
 1 MHz\_ $I_{OUTMAX} = 5\text{ A\_LLM}$  setting)

Typical Performance Curves – continued

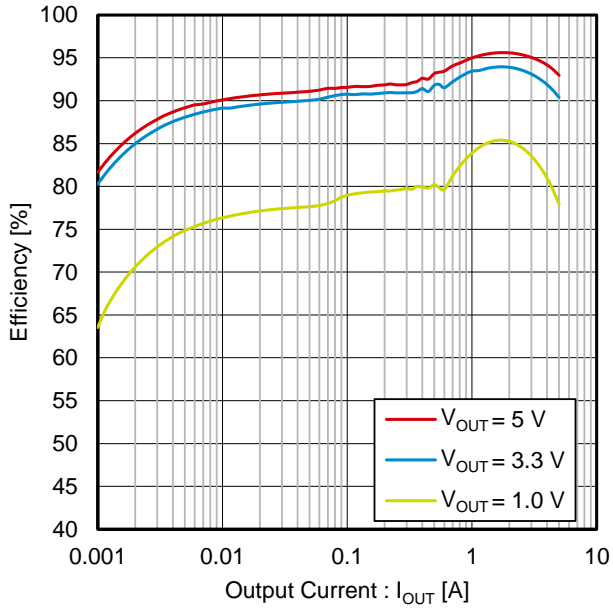


Figure 29. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 600 kHz\_I<sub>OUTMAX</sub> = 5 A\_LLM setting)

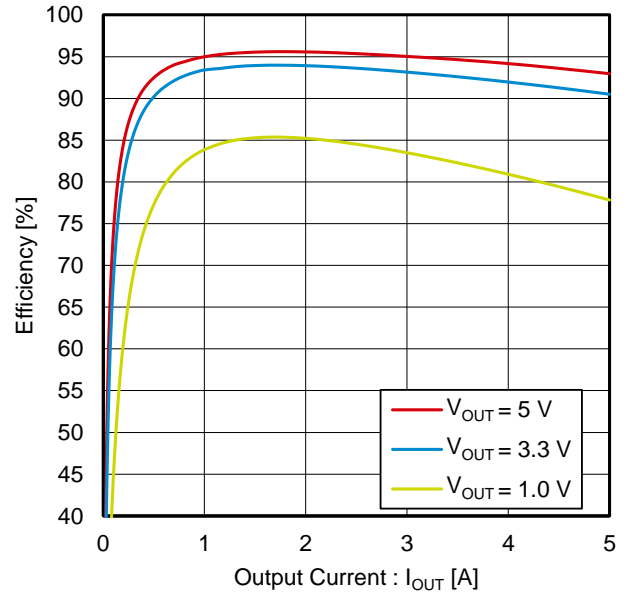


Figure 30. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 600 kHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)

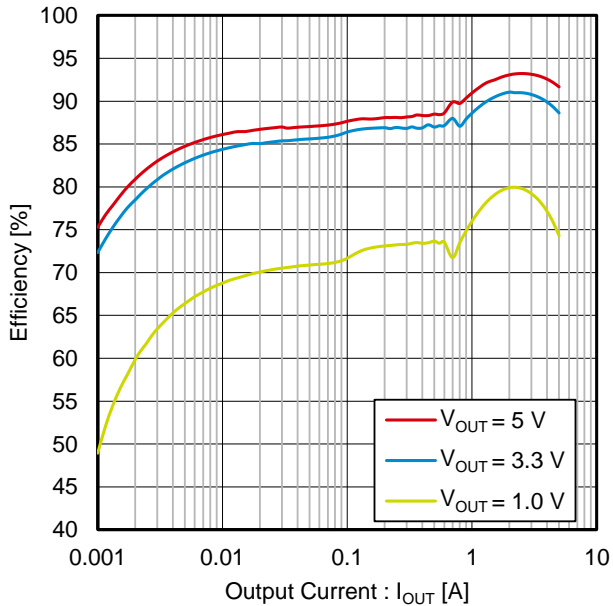


Figure 31. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 600 kHz\_I<sub>OUTMAX</sub> = 5 A\_LLM setting)

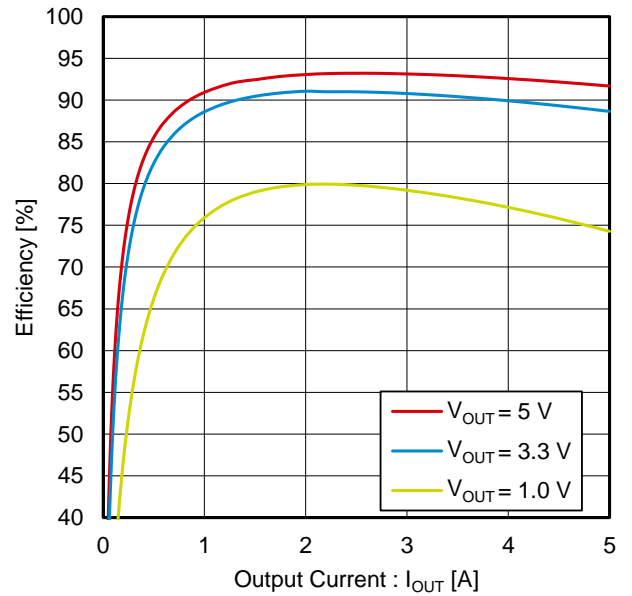


Figure 32. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 600 kHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)

Typical Performance Curves – continued

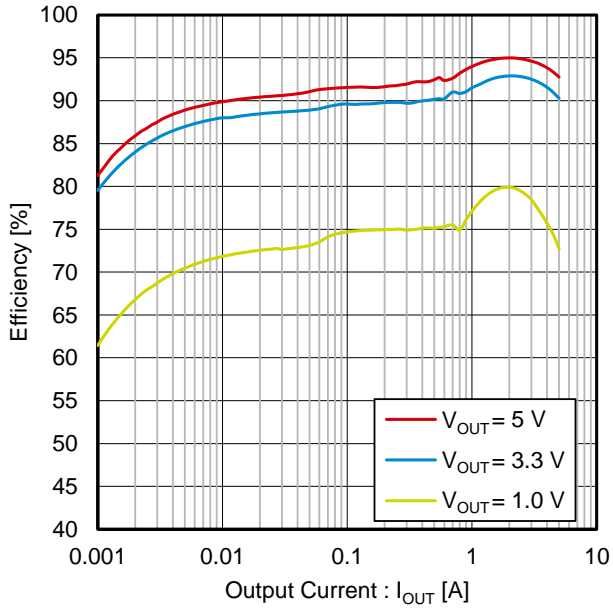


Figure 33. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 1 MHz\_I<sub>OUTMAX</sub> = 5 A\_LLM setting)

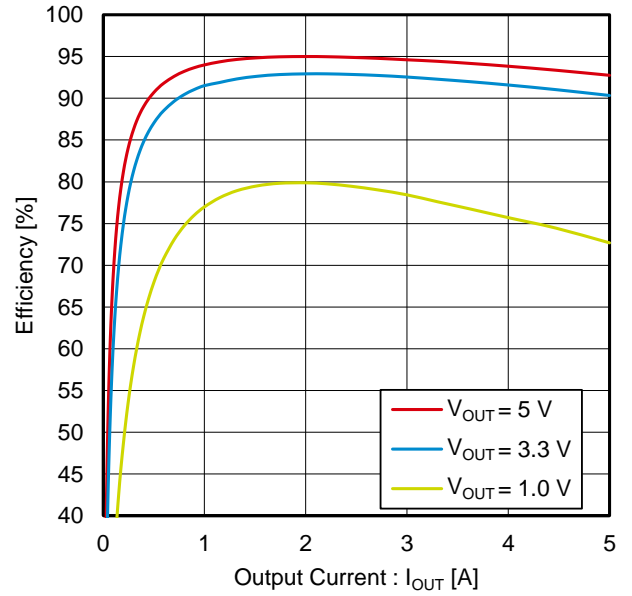


Figure 34. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 1 MHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)

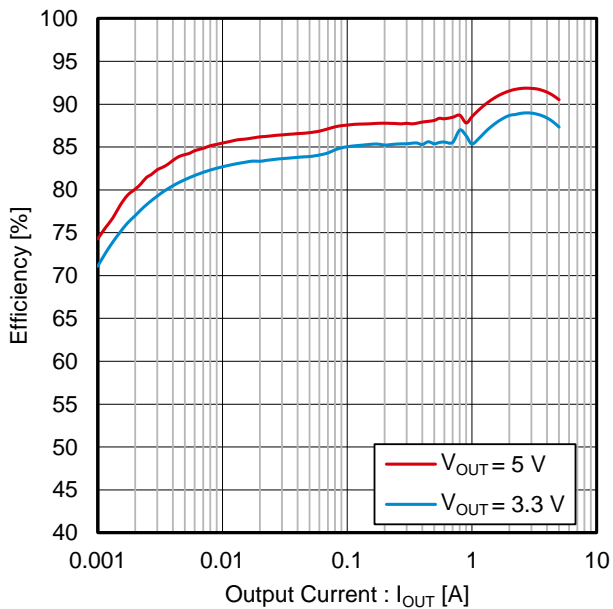


Figure 35. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 1 MHz\_I<sub>OUTMAX</sub> = 5 A\_LLM setting)

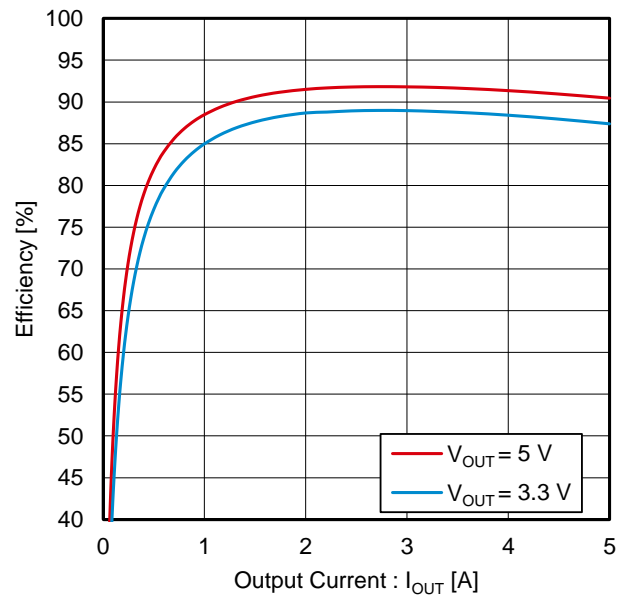


Figure 36. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 1 MHz\_I<sub>OUTMAX</sub> = 5 A\_PWM setting)



Typical Performance Curves – continued

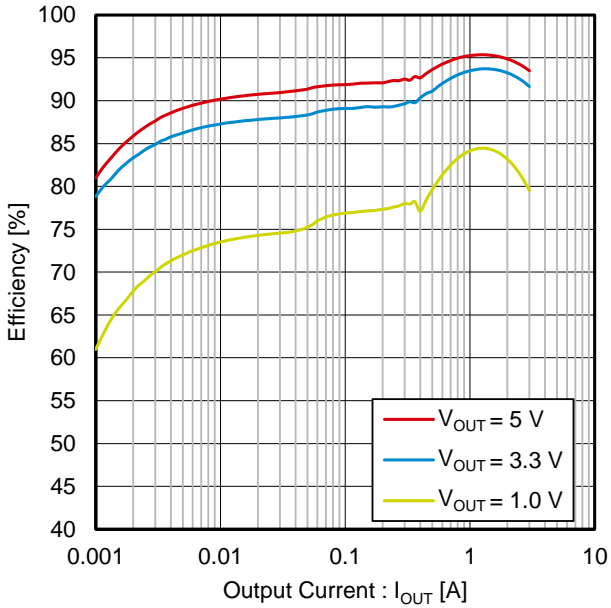


Figure 37. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 600 kHz\_I<sub>OUTMAX</sub> = 3 A\_LLM setting)

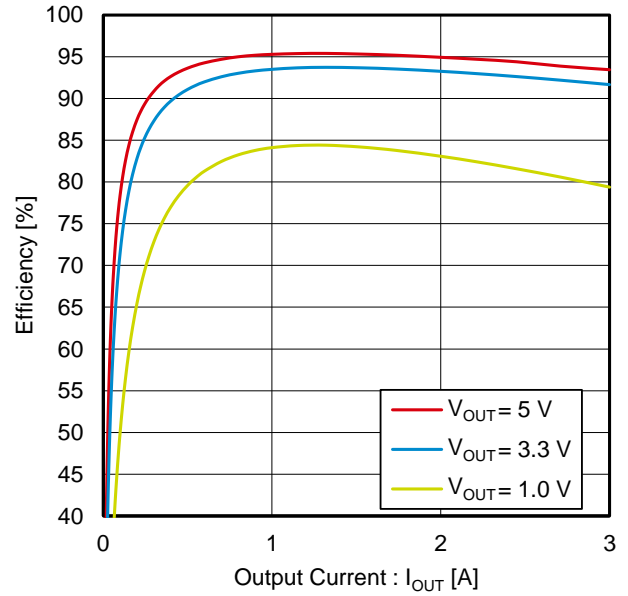


Figure 38. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 600 kHz\_I<sub>OUTMAX</sub> = 3 A\_PWM setting)

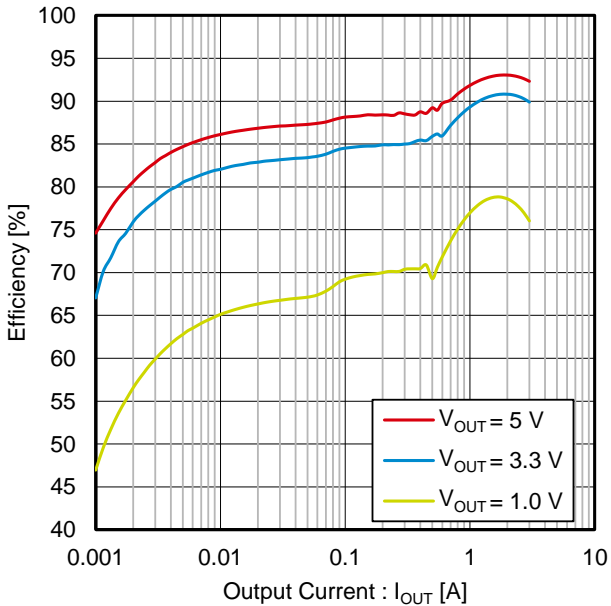


Figure 39. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 600 kHz\_I<sub>OUTMAX</sub> = 3 A\_LLM setting)

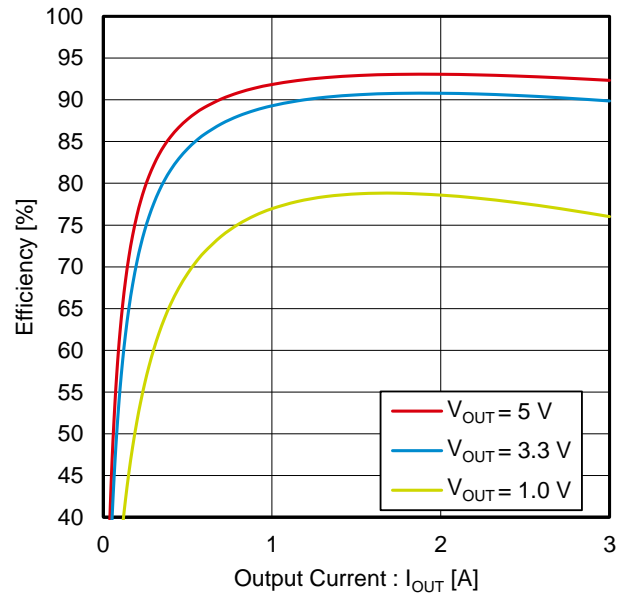


Figure 40. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 600 kHz\_I<sub>OUTMAX</sub> = 3 A\_PWM setting)

Typical Performance Curves – continued

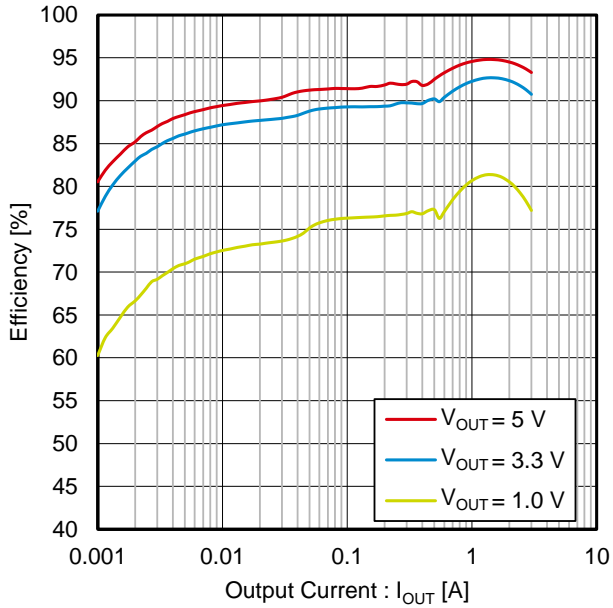


Figure 41. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 1 MHz\_I<sub>OUTMAX</sub> = 3 A\_LLM setting)

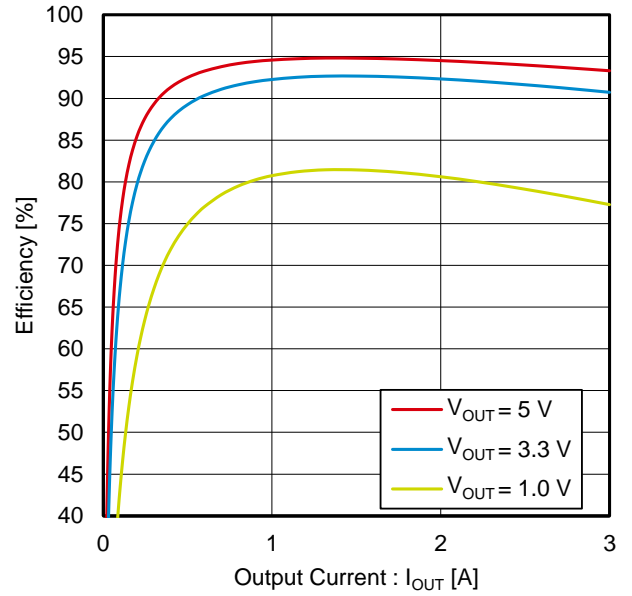


Figure 42. Efficiency vs Output Current  
(V<sub>IN</sub> = 12 V, 1 MHz\_I<sub>OUTMAX</sub> = 3 A\_PWM setting)

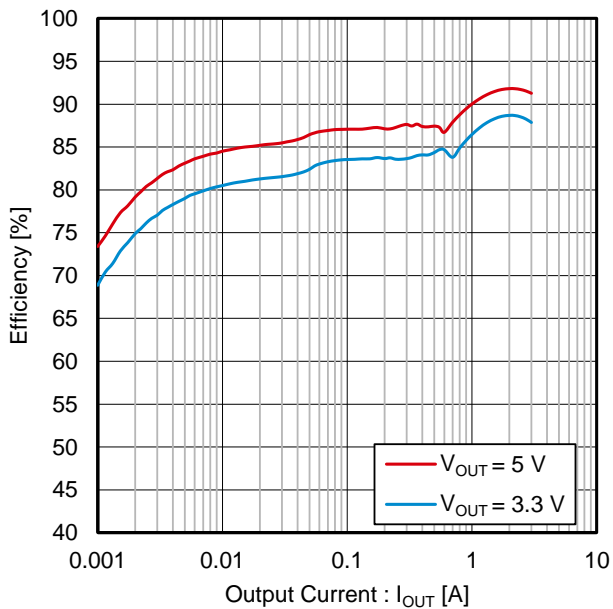


Figure 43. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 1 MHz\_I<sub>OUTMAX</sub> = 3 A\_LLM setting)

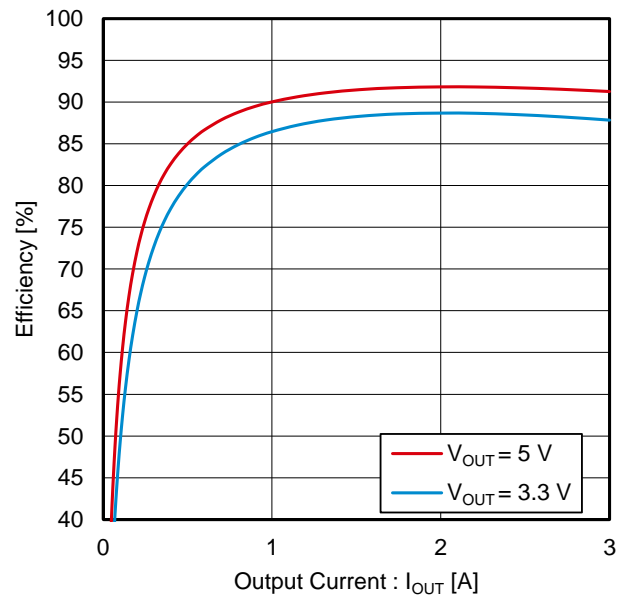


Figure 44. Efficiency vs Output Current  
(V<sub>IN</sub> = 24 V, 1 MHz\_I<sub>OUTMAX</sub> = 3 A\_PWM setting)

Typical Performance Curves – continued

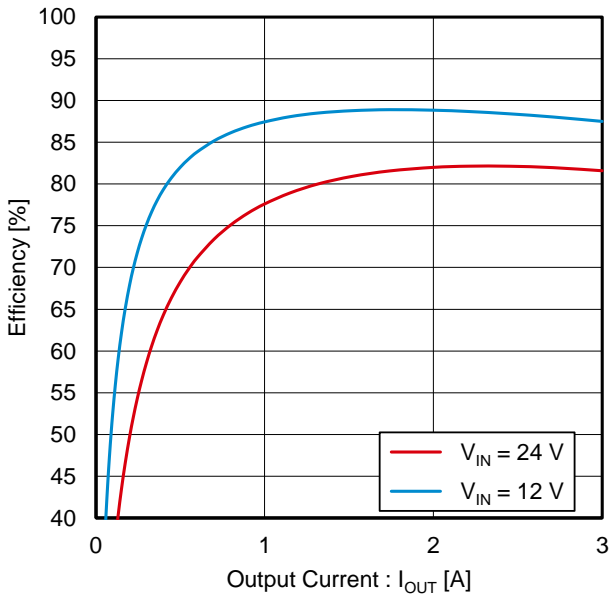


Figure 45. Efficiency vs Output Current  
(V<sub>OUT</sub> = 3.3 V, 2.2 MHz setting)

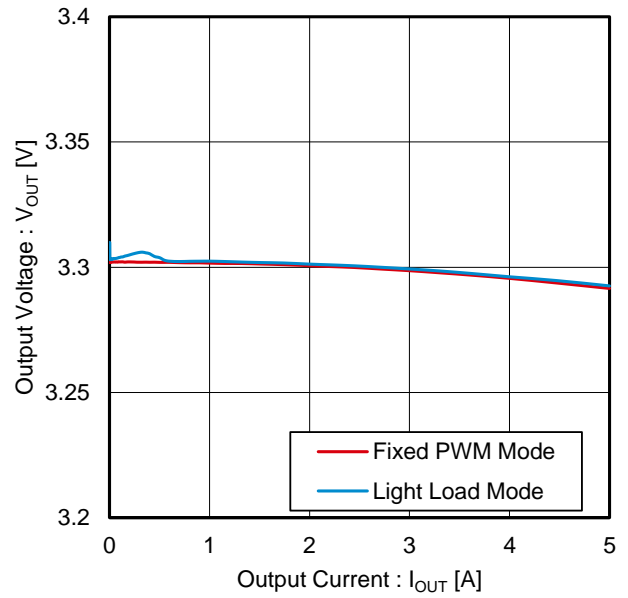


Figure 46. Load Regulation  
(V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, 600 kHz\_I<sub>OUTMAX</sub> = 5 A setting)

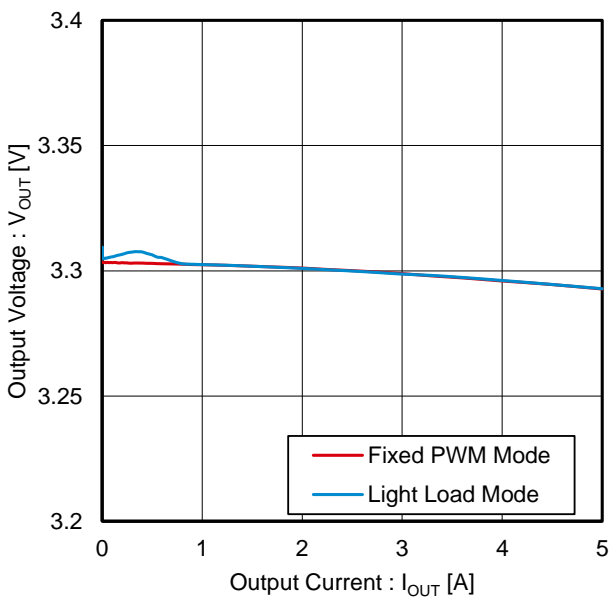


Figure 47. Load Regulation  
(V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, 1 MHz\_I<sub>OUTMAX</sub> = 5 A setting)

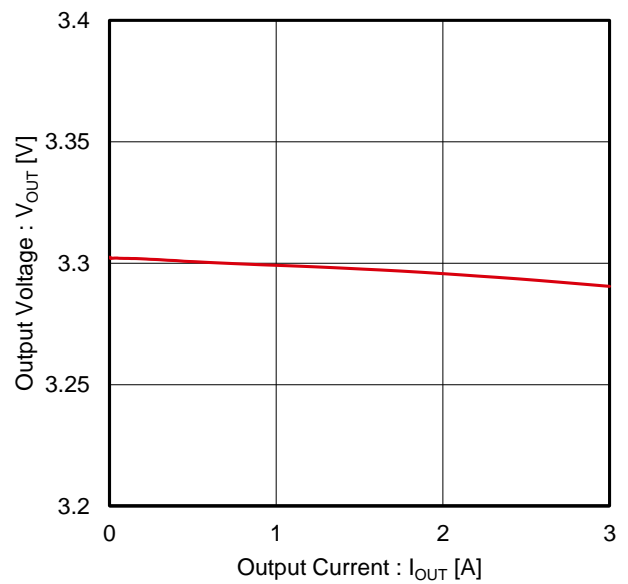


Figure 48. Load Regulation  
(V<sub>IN</sub> = 12 V, V<sub>OUT</sub> = 3.3 V, 2.2 MHz setting)

Typical Performance Curves – continued

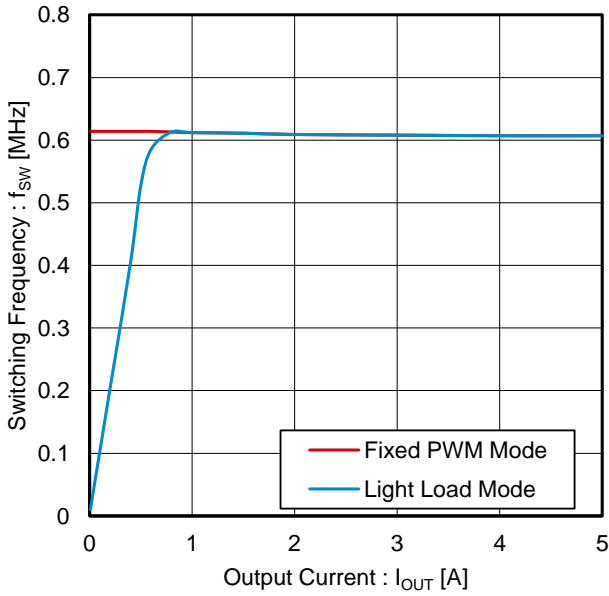


Figure 49. Switching Frequency vs Output Current  
( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $600\text{ kHz\_IOUTMAX} = 5\text{ A}$  setting)

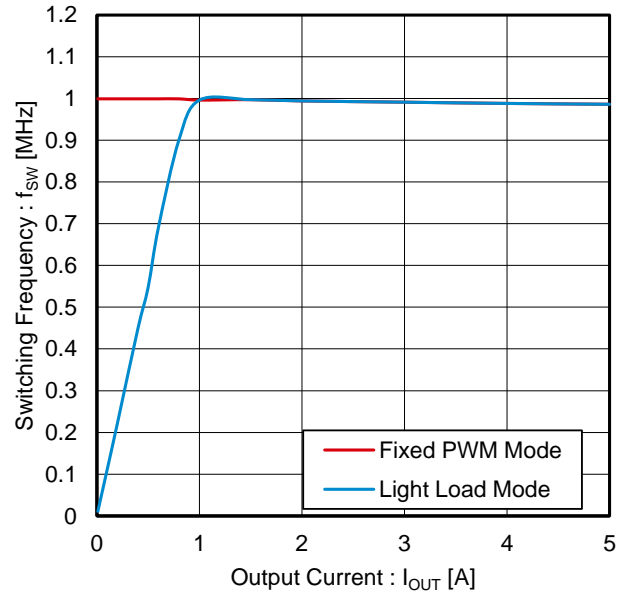


Figure 50. Switching Frequency vs Output Current  
( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $1\text{ MHz\_IOUTMAX} = 5\text{ A}$  setting)

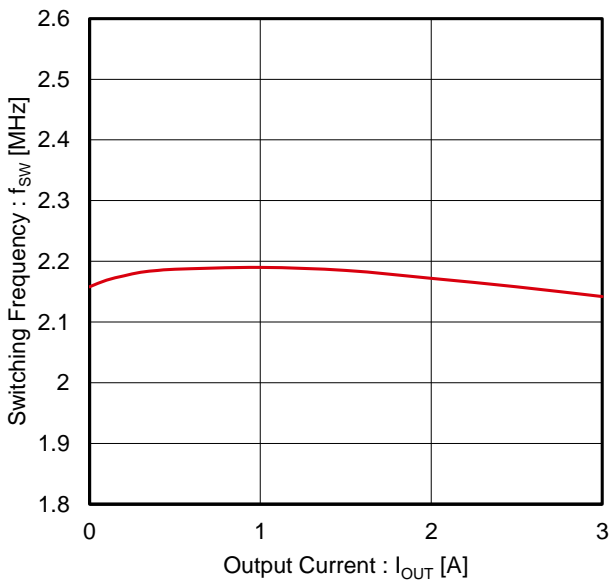


Figure 51. Switching Frequency vs Output Current  
( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $2.2\text{ MHz}$  setting)

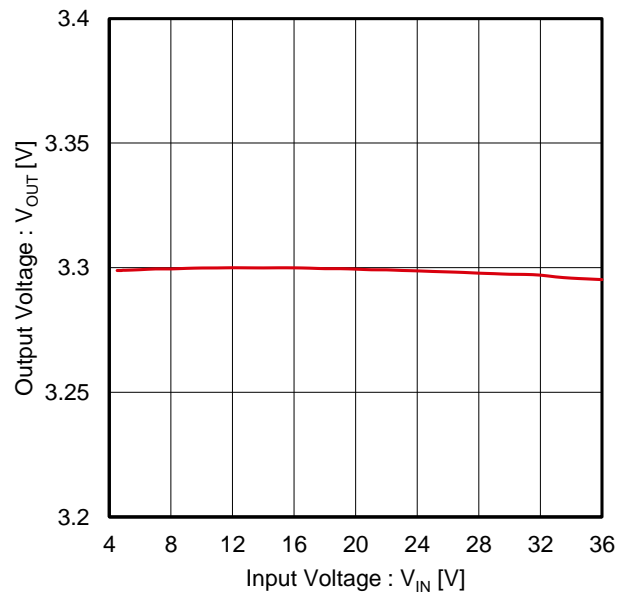


Figure 52. Line Regulation  
( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$ ,  $600\text{ kHz\_IOUTMAX} = 5\text{ A\_PWM}$  setting)

Typical Performance Curves – continued

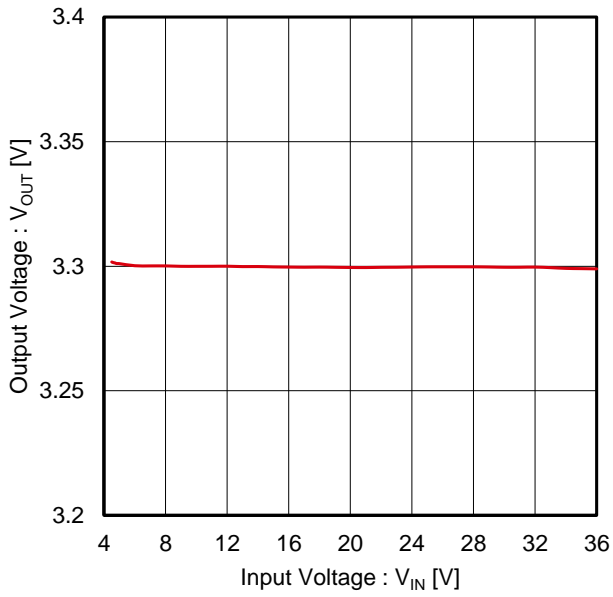


Figure 53. Line Regulation  
( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$ ,  $1\text{ MHz\_}I_{OUTMAX} = 5\text{ A\_PWM}$  setting)

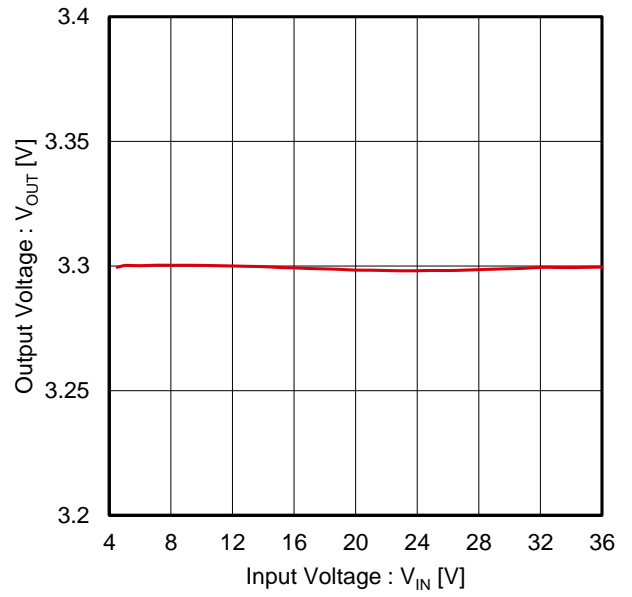


Figure 54. Line regulation  
( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $2.2\text{ MHz}$  setting)

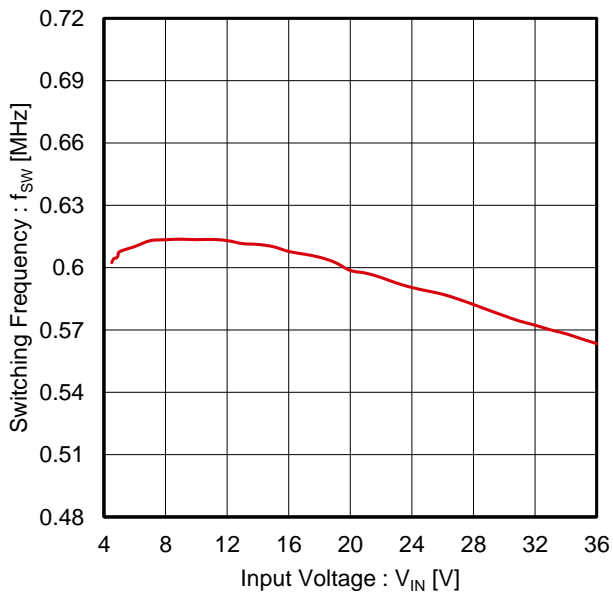


Figure 55. Switching Frequency vs Input Voltage  
( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$ ,  $600\text{ kHz\_}I_{OUTMAX} = 5\text{ A\_PWM}$  setting)

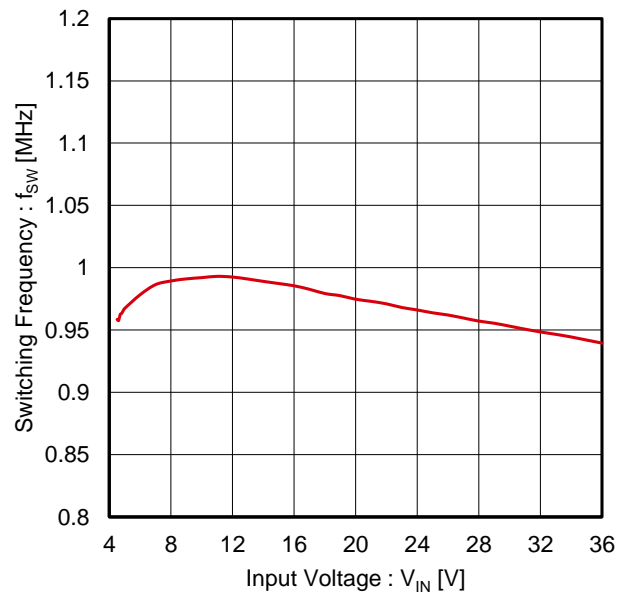


Figure 56. Switching Frequency vs Input Voltage  
( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 2\text{ A}$ ,  $1\text{ MHz\_}I_{OUTMAX} = 5\text{ A\_PWM}$  setting)

Typical Performance Curves – continued

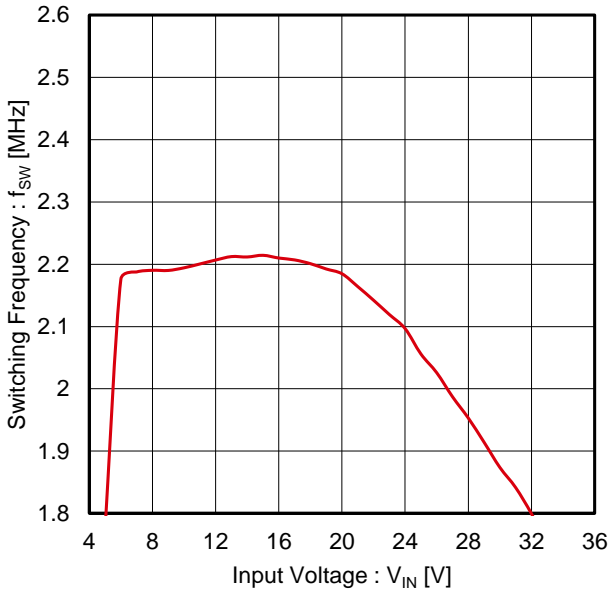


Figure 57. Switching Frequency vs Input Voltage ( $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ , 2.2 MHz setting)

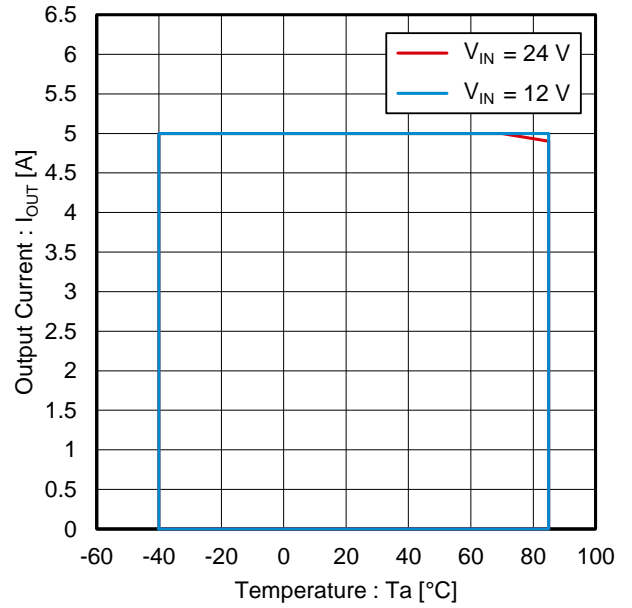


Figure 58. Output Current vs Temperature <sup>(Note 1)</sup>  
Operating Range:  $T_j < 150\text{ °C}$  ( $V_{OUT} = 3.3\text{ V}$ , 600 kHz setting)

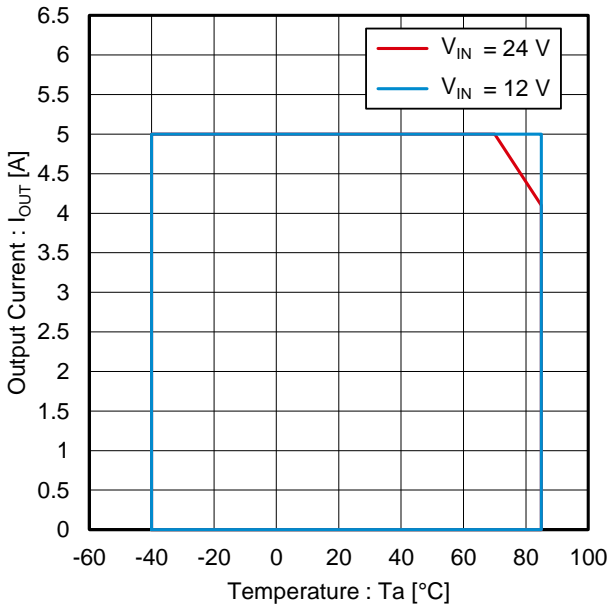


Figure 59. Output Current vs Temperature <sup>(Note 1)</sup>  
Operating Range:  $T_j < 150\text{ °C}$  ( $V_{OUT} = 3.3\text{ V}$ , 1 MHz setting)

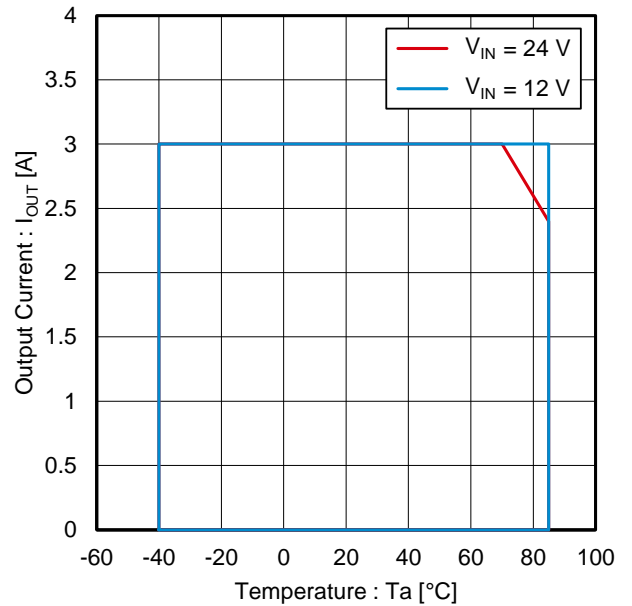


Figure 60. Output Current vs Temperature <sup>(Note 1)</sup>  
Operating Range:  $T_j < 150\text{ °C}$  ( $V_{OUT} = 3.3\text{ V}$ , 2.2 MHz setting)

(Note 1) Measured on FR-4 board 85 mm x 85 mm, Copper Thickness: Top and Bottom 70  $\mu\text{m}$ , 2 Internal Layers 35  $\mu\text{m}$ .

Function Explanations

1. Basic Operation

(1) DC/DC Converter Operation

BD9F500QUZ is a synchronous rectifying step-down switching regulator that has original On-Time control method. Device operates as the SEL1 pin and the SEL2 pin setting. When the operating mode is Light Load Mode, it utilizes switching operation in Pulse Width Modulation (PWM) mode control at heavier load, and it operates in Light Load mode (LLM) control at lighter load to improve efficiency. When the operating mode is Fixed PWM Mode, the device operates in PWM mode control regardless of the load.

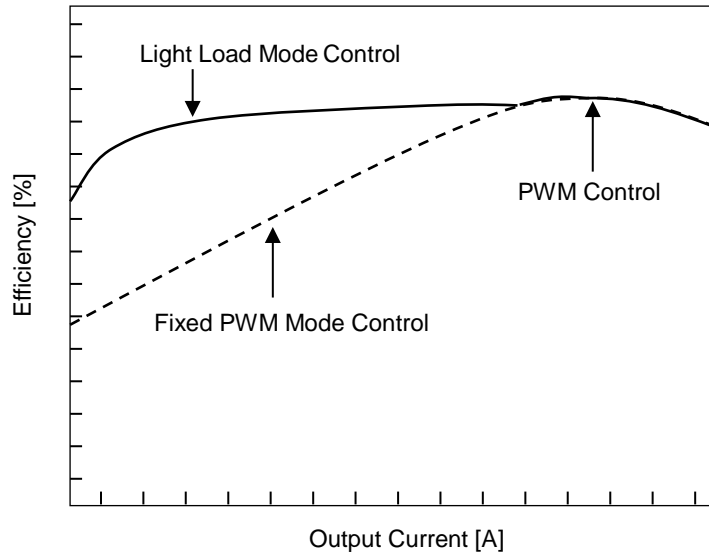


Figure 61. Efficiency Image between Light Load Mode Control and PWM Mode Control

(2) Enable Control

The startup and shutdown can be controlled by the EN voltage ( $V_{EN}$ ). When  $V_{EN}$  becomes 1.2 V (Typ) or more, the internal circuit is activated and the device starts up. When  $V_{EN}$  becomes 1.1 V (Typ) or less, the device is shutdown. In this shutdown mode, the High-Side FET and the Low-Side FET are turned off and the SW pin is connected to GND through an internal resistor 400  $\Omega$  (Typ) to discharge the output. The start-up with  $V_{EN}$  must be at the same time of the input voltage  $V_{IN}$  ( $V_{IN} = V_{EN}$ ) or after supplying  $V_{IN}$ .

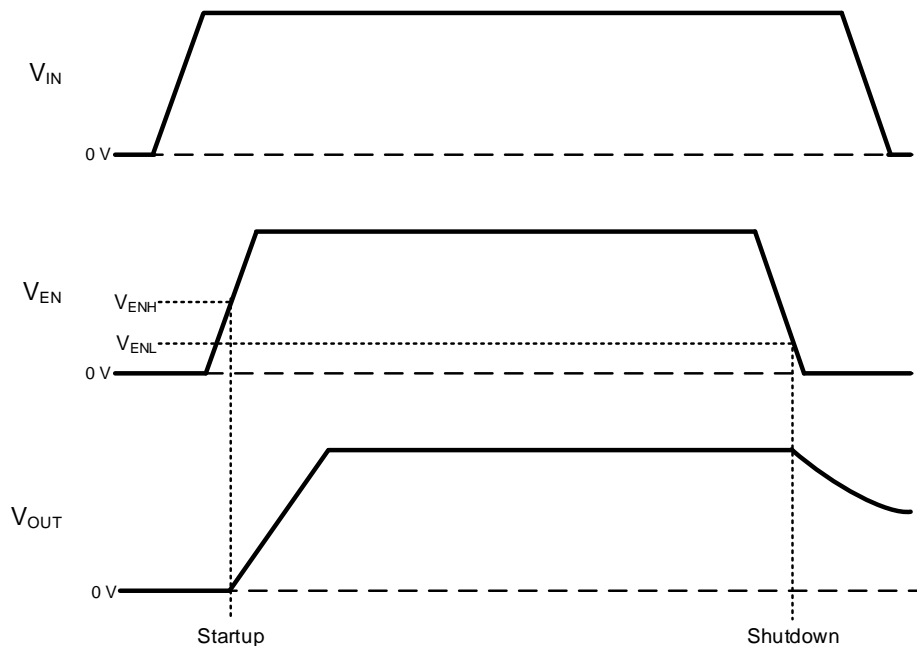


Figure 62. Startup and Shutdown with Enable Control Timing Chart

1. Basic Operation – continued

(3) Soft Start

When  $V_{EN}$  goes high, soft start function operates and output voltage gradually rises. This soft start function can prevent overshoot of the output voltage and excessive inrush current. The soft start time  $t_{SS}$  is 2 ms (Typ) when the SS pin is left floating. A capacitor connected to the SS pin makes  $t_{SS}$  more than 2 ms. See [Selection of Components Externally Connected 4. Soft Start Capacitor](#) for how to set the soft start time.

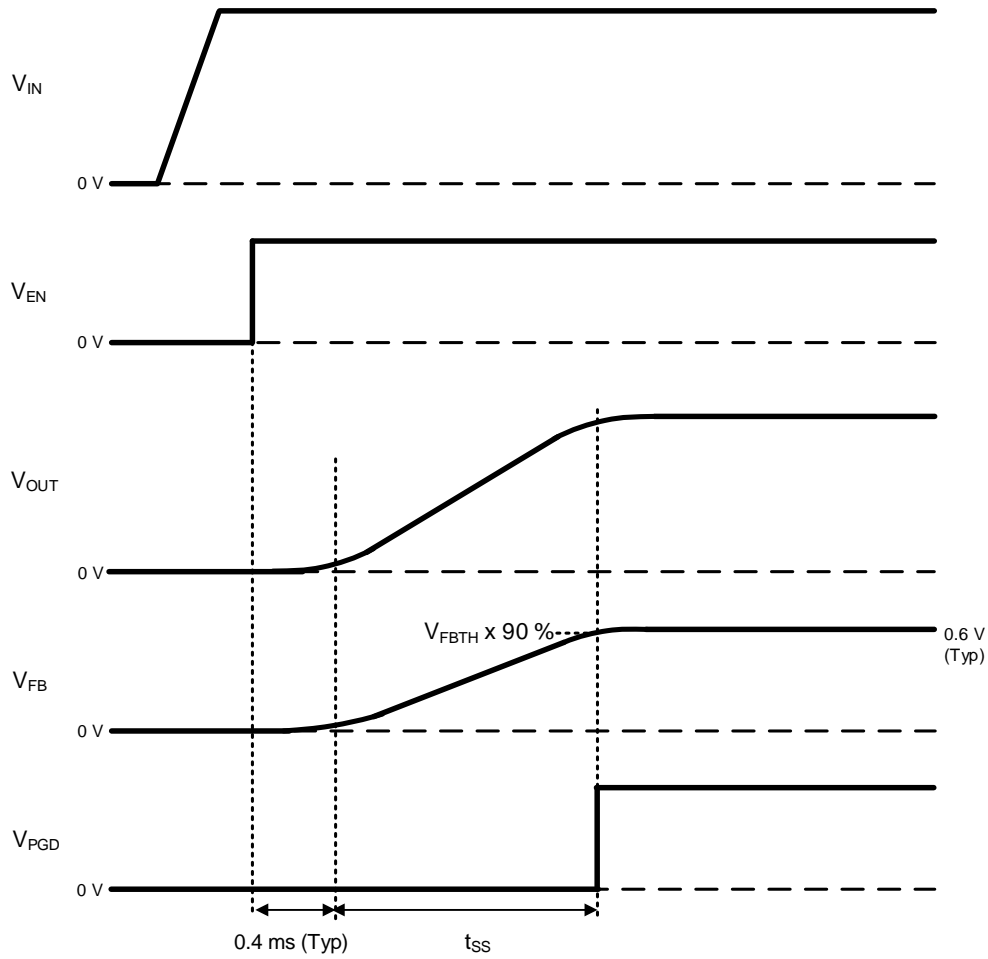


Figure 63. Soft Start Timing Chart



1. Basic Operation – continued

(4) Power Good

When the output voltage  $V_{OUT}$  reaches within  $\pm 7\%$  (Typ) of the voltage setting, the built-in open drain Nch MOSFET connected to the PGD pin is turned off, and the PGD pin goes Hi-Z (High impedance). When  $V_{OUT}$  reaches outside  $\pm 10\%$  (Typ) of the voltage setting, the open drain Nch MOSFET is turned on and PGD pin is pulled down with  $500\ \Omega$  (Typ). It is recommended to connect a pull-up resistor of  $20\ \text{k}\Omega$  to  $100\ \text{k}\Omega$ .

Table 1. PGD Output

State	Condition	PGD Output
Before Supply Input Voltage	$V_{IN} < 2.5\ \text{V (Typ)}$	Hi-Z
Shutdown	$V_{EN} \leq 1.1\ \text{V (Typ)}$	Low (Pull-down)
Enable $V_{EN} \geq 1.2\ \text{V (Typ)}$	$93\% \text{ (Typ)} \leq V_{FB} / V_{FBTH} \leq 107\% \text{ (Typ)}$	Hi-Z
	$V_{FB} / V_{FBTH} \leq 90\% \text{ (Typ)}$ or $110\% \text{ (Typ)} \leq V_{FB} / V_{FBTH}$	Low (Pull-down)
UVLO	$2.5\ \text{V (Typ)} < V_{IN} \leq 4.0\ \text{V (Typ)}$	Low (Pull-down)
TSD	$T_j \geq 175\ \text{°C (Typ)}$	Low (Pull-down)

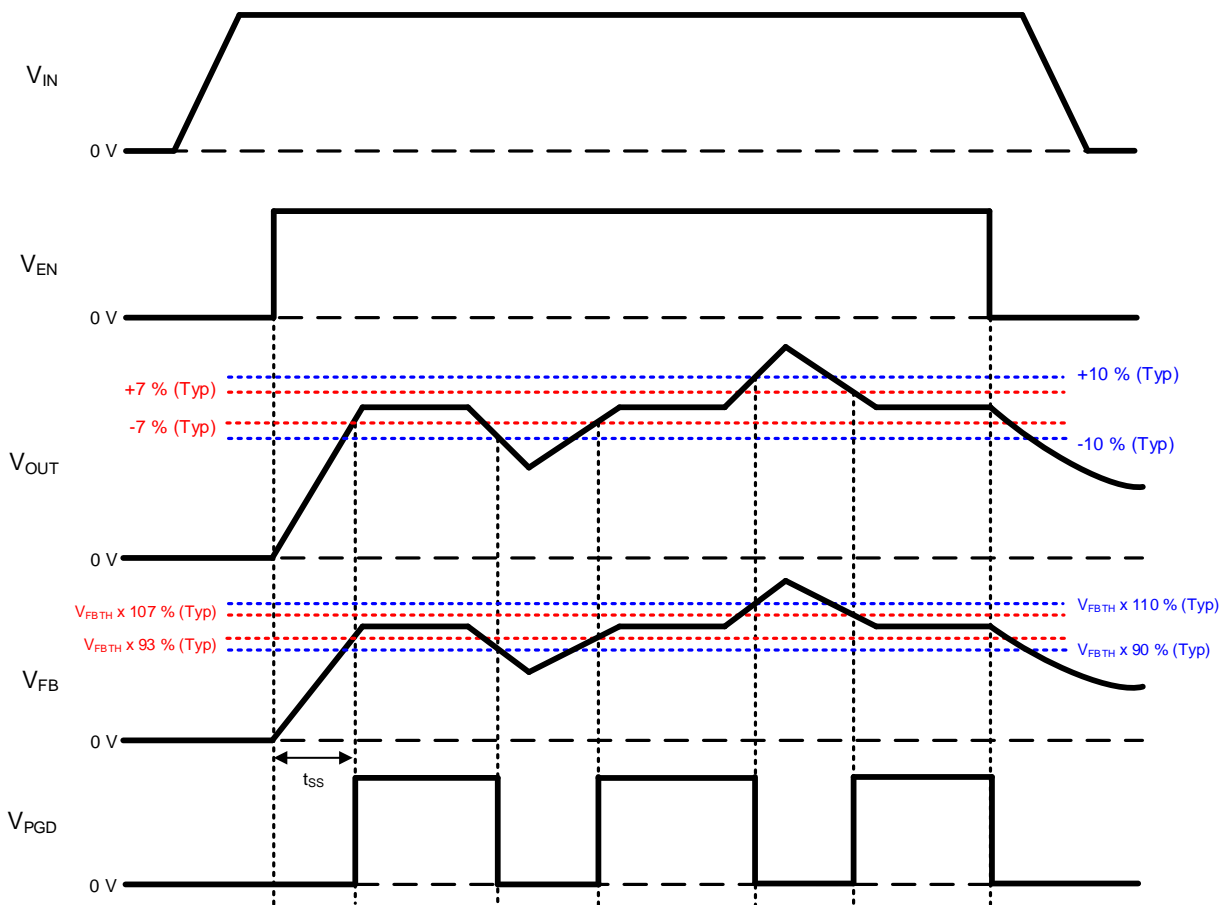


Figure 64. Power Good Timing Chart  
(Connecting a pull-up resistor to the PGD pin)

(5) Nano Pulse Control™

Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition.

## 1. Basic Operation – continued

### (6) Output Capacitor Discharge Function

When even one of the following conditions is satisfied, output is discharged with 400 Ω (Typ) resistor through the SW pin.

- Shutdown:  $V_{EN} \leq 1.1 \text{ V (Typ)}$
- UVLO:  $V_{IN} \leq 4.0 \text{ V (Typ)}$
- TSD:  $T_j \geq 175 \text{ °C (Typ)}$
- OVP:  $V_{FB} / V_{FBTH} \geq 120 \% \text{ (Typ)}$

When all of the above conditions are released, output discharge is stopped.

### (7) Control Mode Selectable Function

BD9F500QUZ has the SEL1 pin and the SEL2 pin that can offer 9 different states of operation as a combination of Switching Frequency, Maximum Output Current and Operation mode. It can operate at two different current limits to support an output continuous current of 5 A, 3 A respectively. It can operate at three different frequencies of 600 kHz, 1 MHz and 2.2 MHz and also can choose between Light Load Mode and Fixed PWM mode for 600 kHz and 1 MHz operation. Do not change the mode control of Switching Frequency and Maximum Output Current during operation.

Table 2. Control Mode Selection

SEL1 pin condition	SEL2 pin condition	Switching Frequency	Maximum Output Current ( $I_{OUTMAX}$ )	Operation Mode
GND	GND	1 MHz (Typ)	5 A	Light Load Mode (LLM)
GND	OPEN			Fixed PWM Mode
VREG	GND		3 A	Light Load Mode (LLM)
VREG	OPEN			Fixed PWM Mode
OPEN	GND	600 kHz (Typ)	5 A	Light Load Mode (LLM)
OPEN	OPEN			Fixed PWM Mode
GND	VREG		3 A	Light Load Mode (LLM)
OPEN	VREG			Fixed PWM Mode
VREG	VREG	2.2 MHz (Typ)	3 A	Fixed PWM Mode

Table 3. OCP Value

Maximum Output Current ( $I_{OUTMAX}$ )	Low-Side OCP	High-Side OCP	Low-Side Sink OCP (Fixed PWM mode)
5 A	$I_{LOCP1} = 6.7 \text{ A (Typ)}$	$I_{HOCP1} = 8.25 \text{ A (Typ)}$	$I_{ROCP1} = 4.2 \text{ A (Typ)}$
3 A	$I_{LOCP2} = 4.0 \text{ A (Typ)}$	$I_{HOCP2} = 5.0 \text{ A (Typ)}$	$I_{ROCP2} = 2.5 \text{ A (Typ)}$

Function Explanations – continued

2. Protection

The protection circuits are intended for prevention of damage caused by unexpected accidents. Do not use the continuous protection.

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Over Current Protection (OCP) restricts the flowing current through the Low-Side FET and the High-Side FET for every switching period. If the inductor current exceeds the Low-Side OCP  $I_{LOCP1} = 6.7 \text{ A (Typ)}$ ,  $I_{LOCP2} = 4.0 \text{ A (Typ)}$  while the Low-Side FET is on, the Low-Side FET remains on even with FB voltage  $V_{FB}$  falls to  $V_{FBTH} = 0.6 \text{ V (Typ)}$  or less. If the inductor current becomes less than  $I_{LOCP1}$ ,  $I_{LOCP2}$ , the High-Side FET is able to be turned on. When the inductor current becomes the High-Side OCP  $I_{HOCP1} = 8.25 \text{ A (Typ)}$ ,  $I_{HOCP2} = 5.0 \text{ A (Typ)}$  or more while the High-Side FET is on, the High-Side FET is turned off. Output voltage may decrease by changing frequency and duty due to the OCP operation. Short Circuit Protection (SCP) function is a Hiccup mode. When Low-Side OCP 128 times is counted while  $V_{FB}$  is  $V_{FBTH} \times 90\%$  or less ( $V_{PGD} = \text{Low}$ ), the device stops the switching operation for 16 times of Soft Start Time (Typ). After that, the device restarts. SCP does not operate during the soft start even if the device is in the SCP conditions. Do not exceed the maximum junction temperature ( $T_{jmax} = 150 \text{ }^\circ\text{C}$ ) during OCP and SCP operation.

Table 4. The Operating Condition of OCP and SCP

$V_{EN}$	$V_{FB}$	Start-up	OCP	SCP
$\geq 1.2 \text{ V (Typ)}$	$\leq V_{FBTH} \times 90\% \text{ (Typ)}$	During Soft Start	Enable	Disable
	$> V_{FBTH} \times 93\% \text{ (Typ)}$	Complete Soft Start	Enable	Disable
	$\leq V_{FBTH} \times 90\% \text{ (Typ)}$		Enable	Enable
$\leq 1.1 \text{ V (Typ)}$	-	Shutdown	Disable	Disable

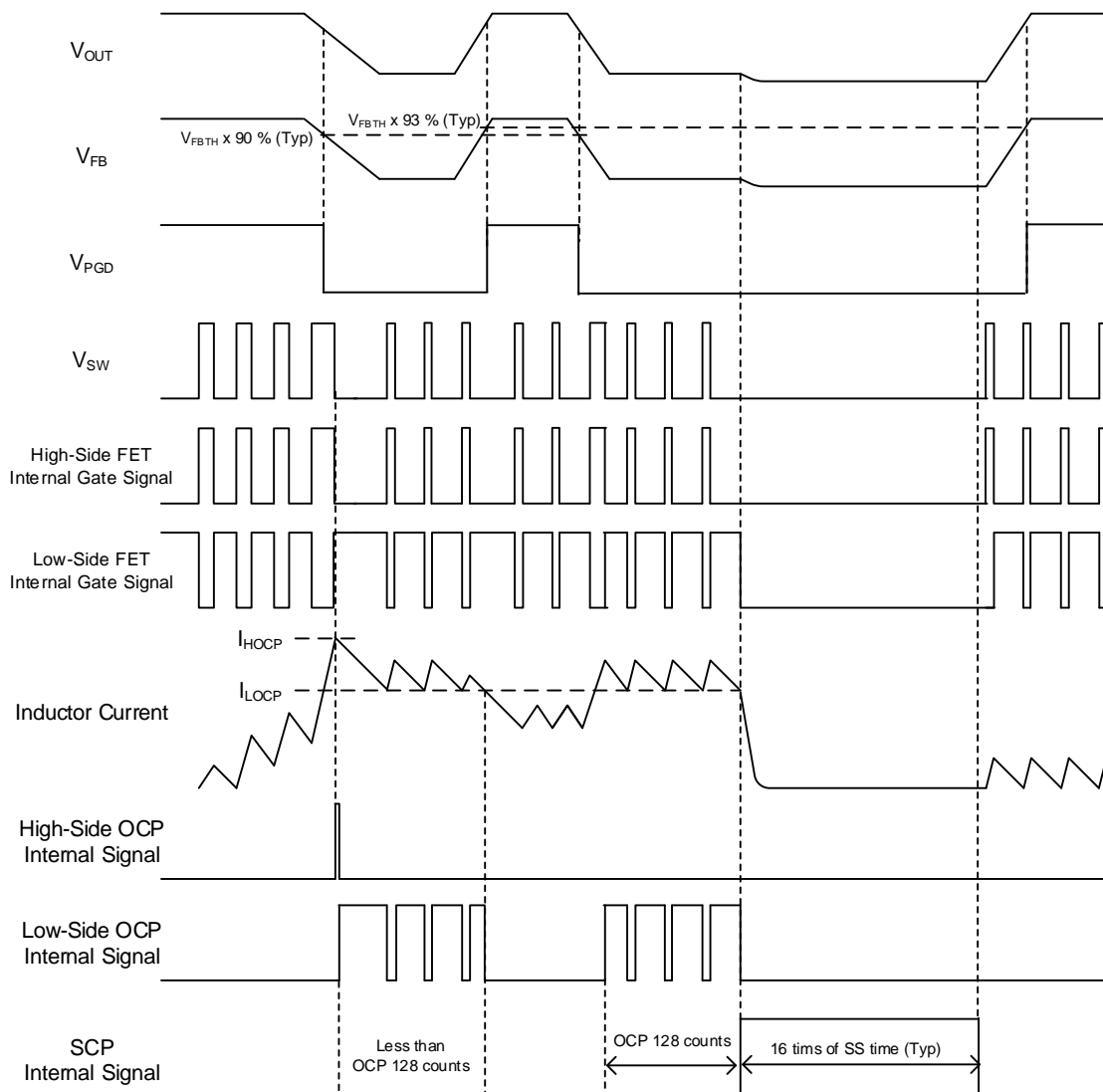


Figure 65. OCP and SCP Timing Chart

## 2. Protection – continued

### (2) Low-Side Sink (Reverse) Over Current Protection (ROCP)

When operating mode is Fixed PWM and inductor current exceeds the sink current limit threshold value  $I_{ROCP1} = 4.2 \text{ A}$  (Typ),  $I_{ROCP2} = 2.5 \text{ A}$  (Typ) while Low-Side FET is ON, the Low-Side FET turns OFF.

### (3) Under Voltage Lockout Protection (UVLO)

When input voltage  $V_{IN}$  falls to  $4.0 \text{ V}$  (Typ) or less, the device is shutdown. When  $V_{IN}$  becomes  $4.2 \text{ V}$  (Typ) or more, the device starts up. The hysteresis is  $200 \text{ mV}$  (Typ).

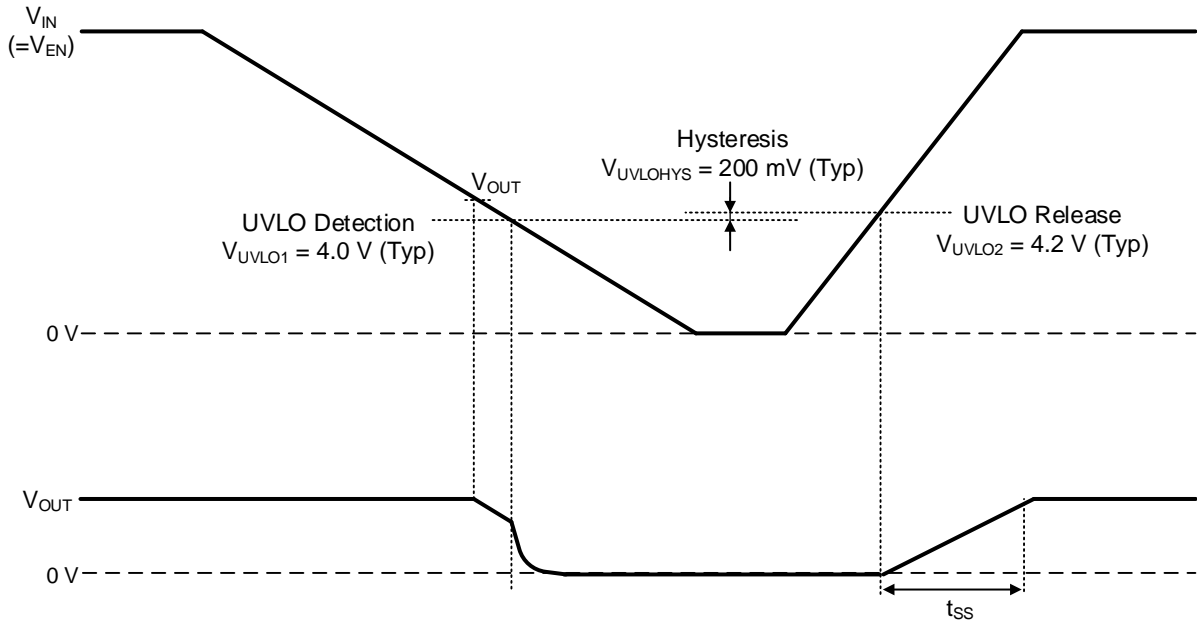


Figure 66. UVLO Timing Chart

### (4) Thermal Shutdown Protection (TSD)

Thermal shutdown circuit prevents heat damage to the IC. The device should always operate within the IC's maximum junction temperature rating ( $T_{jmax} = 150 \text{ }^{\circ}\text{C}$ ). However, if it continues exceeding the rating and the junction temperature  $T_j$  rises to  $175 \text{ }^{\circ}\text{C}$  (Typ), the TSD circuit is activated and it turns the output MOSFETs off. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation. The TSD threshold has a hysteresis of  $25 \text{ }^{\circ}\text{C}$  (Typ). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

### (5) Over Voltage Protection (OVP)

When the FB voltage  $V_{FB}$  exceeds  $V_{FBTH} \times 120 \%$  (Typ) or more, output is discharged with  $400 \Omega$  (Typ) resistor through the SW pin to prevent the increase in the output voltage. After the  $V_{FB}$  falls  $V_{FBTH} \times 115 \%$  (Typ) or less, the output MOSFETs are returned to normal operation condition. Switching operation restarts after  $V_{FB}$  falls below  $V_{FBTH}$  (Typ).

## Application Examples

1.  $V_{IN} = 12\text{ V to }24\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$ 

Table 5. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	12 V to 24 V (Typ)
Output Voltage	$V_{OUT}$	3.3 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	1 MHz (Typ)
Operation Mode	-	Light Load Mode
Temperature	$T_a$	25 °C

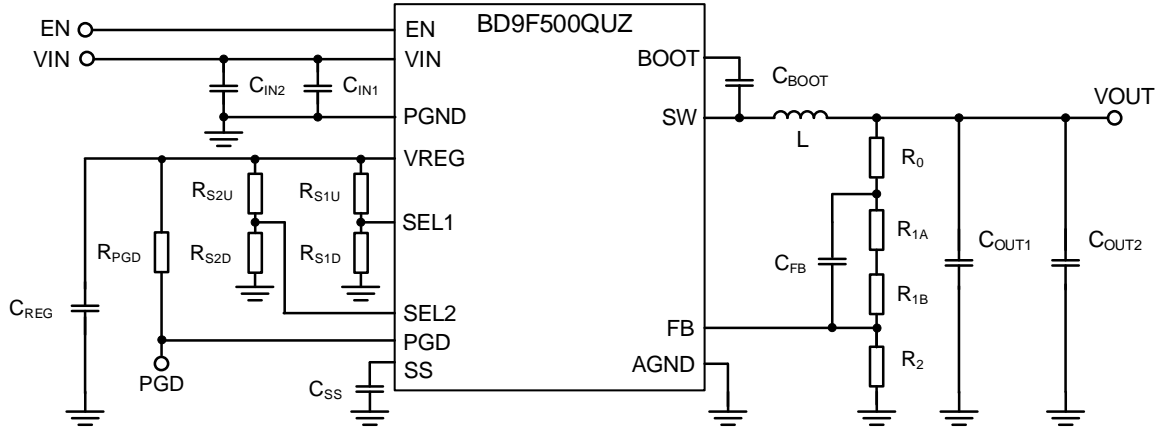


Figure 67. Application Circuit

Table 6. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	1.5 $\mu\text{H}$	1217AS-H-1R5N	8080	Murata
$C_{IN1}$ <sup>(Note 1)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ <sup>(Note 2)</sup>	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ <sup>(Note 3)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ <sup>(Note 5)</sup>	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	82 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H820JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	1.5 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1500	1005	ROHM
$R_{1B}$	120 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1203	1005	ROHM
$R_2$	27 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF2702	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	Short	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	Short	-	-	-
$R_0$ <sup>(Note 6)</sup>	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

1.  $V_{IN} = 12\text{ V}$  to  $24\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$  – continued

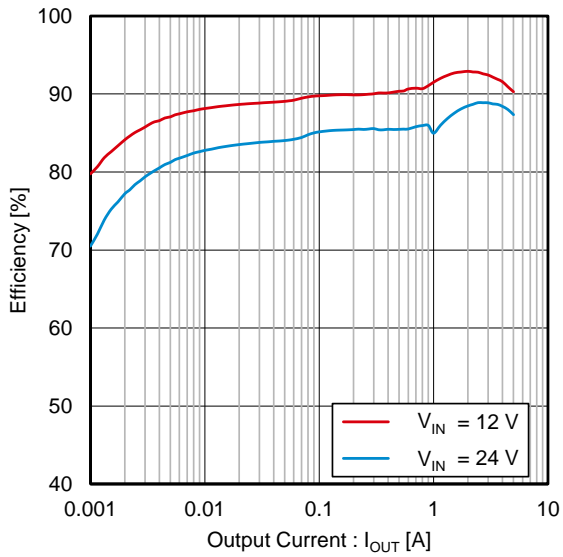


Figure 68. Efficiency vs Output Current

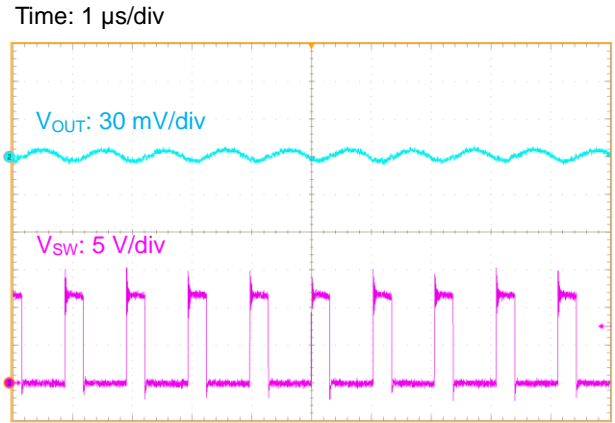


Figure 69. Output Ripple Voltage ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 5\text{ A}$ )

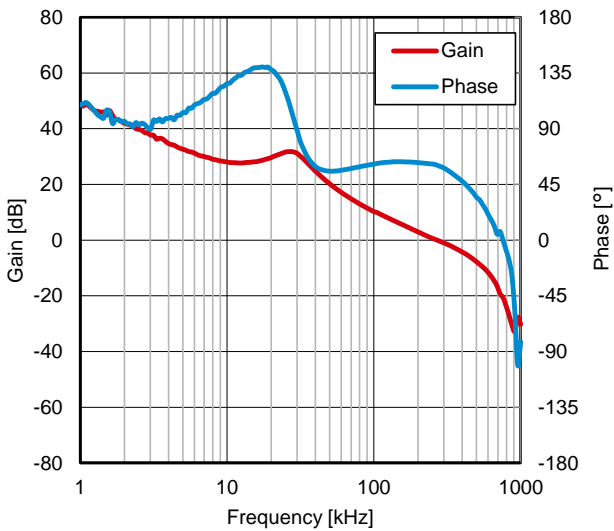


Figure 70. Frequency Characteristics ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 3\text{ A}$ )

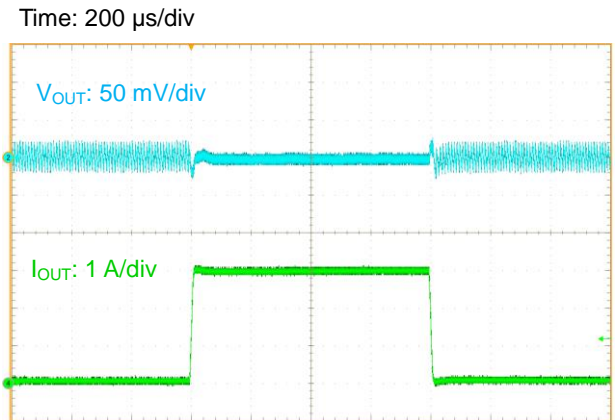


Figure 71. Load Transient Response ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 0.1\text{ A}$  to  $3.0\text{ A}$ )

## Application Examples – continued

2.  $V_{IN} = 12\text{ V to }24\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$ 

Table 7. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	12 V to 24 V (Typ)
Output Voltage	$V_{OUT}$	3.3 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	600 kHz (Typ)
Operation Mode	-	Light Load Mode
Temperature	$T_a$	25 °C

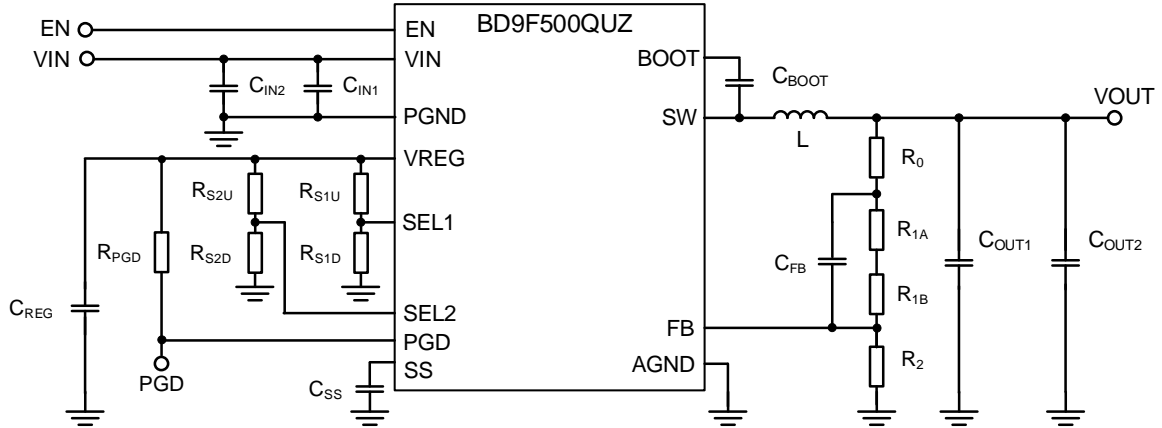


Figure 72. Application Circuit

Table 8. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	3.3 $\mu\text{H}$	1217AS-H-3R3N	8080	Murata
$C_{IN1}$ <sup>(Note 1)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ <sup>(Note 2)</sup>	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ <sup>(Note 3)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ <sup>(Note 5)</sup>	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	82 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H820JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	1.5 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1500	1005	ROHM
$R_{1B}$	120 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1203	1005	ROHM
$R_2$	27 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF2702	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	-	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	Short	-	-	-
$R_0$ <sup>(Note 6)</sup>	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

2.  $V_{IN} = 12\text{ V}$  to  $24\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$  – continued

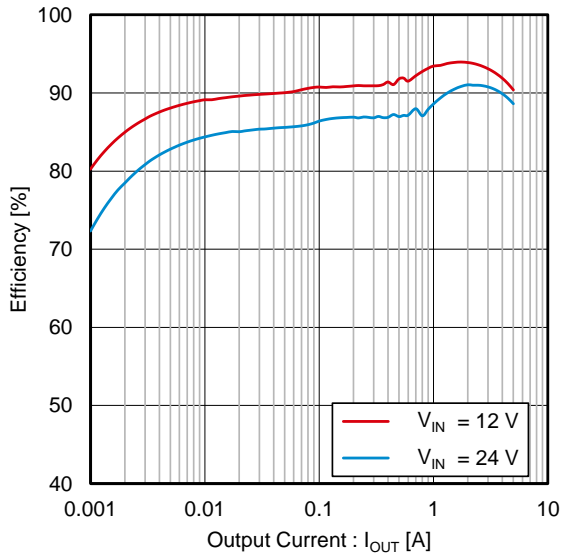


Figure 73. Efficiency vs Output Current

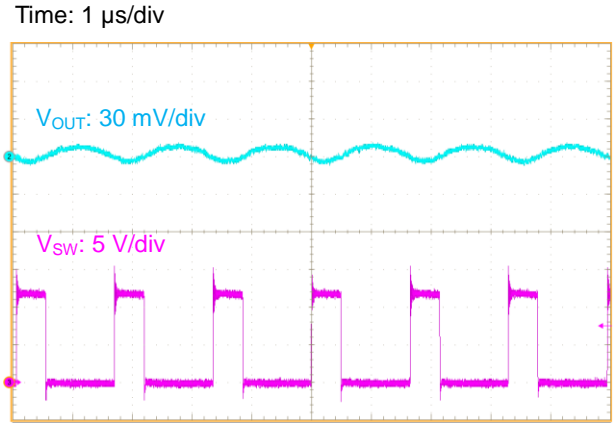


Figure 74. Output Ripple Voltage ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 5\text{ A}$ )

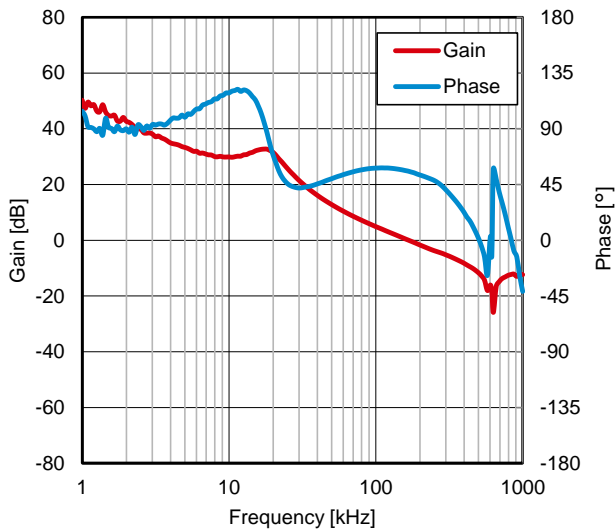


Figure 75. Frequency Characteristics ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 3\text{ A}$ )

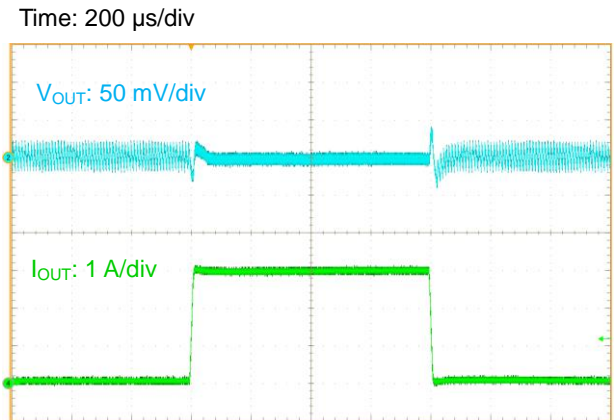


Figure 76. Load Transient Response ( $V_{IN} = 12\text{ V}$ ,  $I_{OUT} = 0.1\text{ A}$  to  $3.0\text{ A}$ )



## Application Examples – continued

3.  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$ 

Table 9. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	5 V (Typ)
Output Voltage	$V_{OUT}$	3.3 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	1 MHz (Typ)
Operation Mode	-	Light Load Mode
Temperature	$T_a$	25 °C

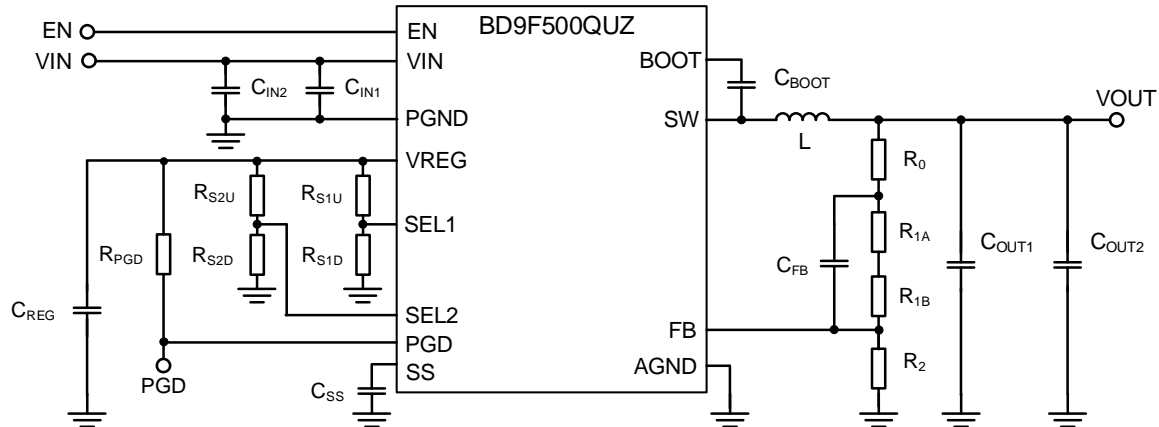


Figure 77. Application Circuit

Table 10. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	1.0 $\mu\text{H}$	FDSD0518-H-1R0M	5249	Murata
$C_{IN1}$ (Note 1)	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ (Note 2)	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ (Note 3)	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ (Note 4)	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ (Note 4)	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ (Note 5)	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	33 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H330JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	120 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1203	1005	ROHM
$R_{1B}$	330 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF3303	1005	ROHM
$R_2$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	Short	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	Short	-	-	-
$R_0$ (Note 6)	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

3.  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$  – continued

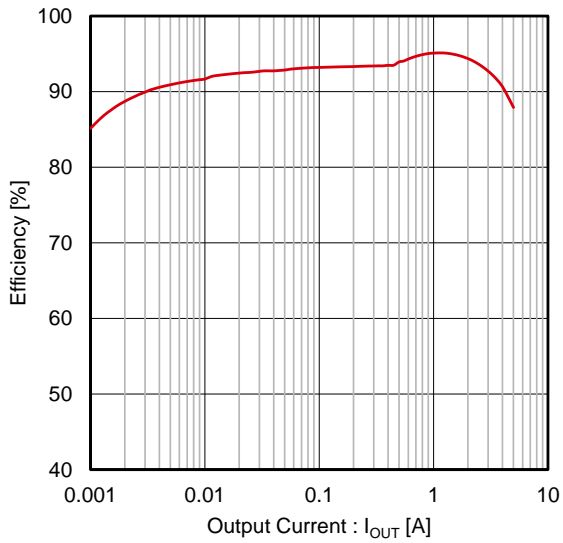


Figure 78. Efficiency vs Output Current

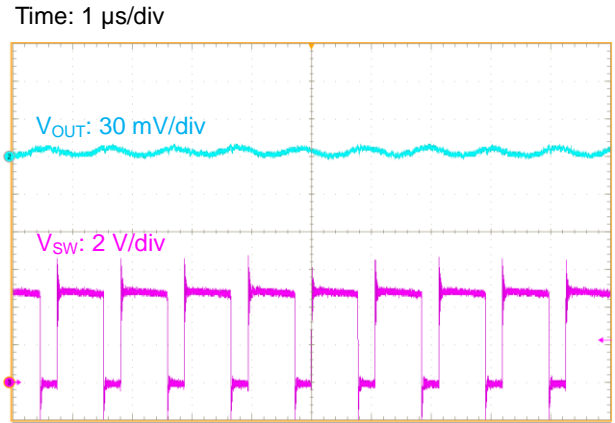


Figure 79. Output Ripple Voltage ( $I_{OUT} = 5\text{ A}$ )

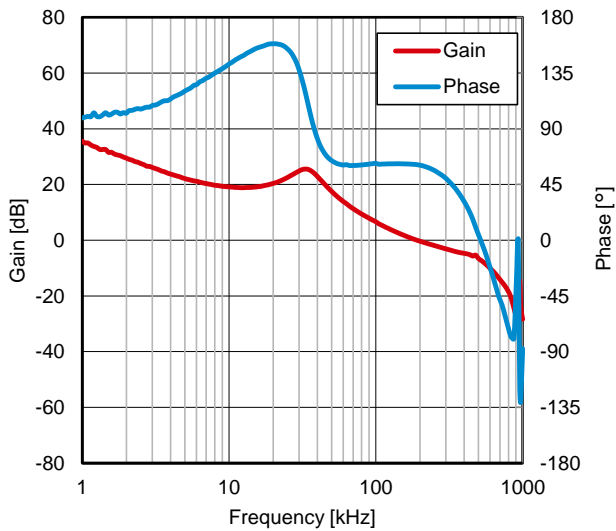


Figure 80. Frequency Characteristics ( $I_{OUT} = 3\text{ A}$ )

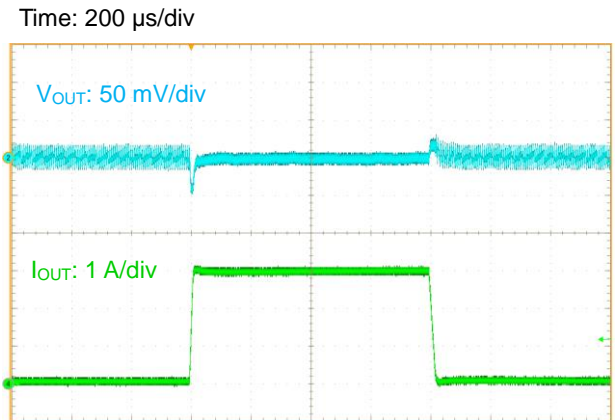


Figure 81. Load Transient Response ( $I_{OUT} = 0.1\text{ A}$  to  $3.0\text{ A}$ )

## Application Examples – continued

4.  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$ 

Table 11. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	5 V (Typ)
Output Voltage	$V_{OUT}$	3.3 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	600 kHz (Typ)
Operation Mode	-	Light Load Mode
Temperature	$T_a$	25 °C

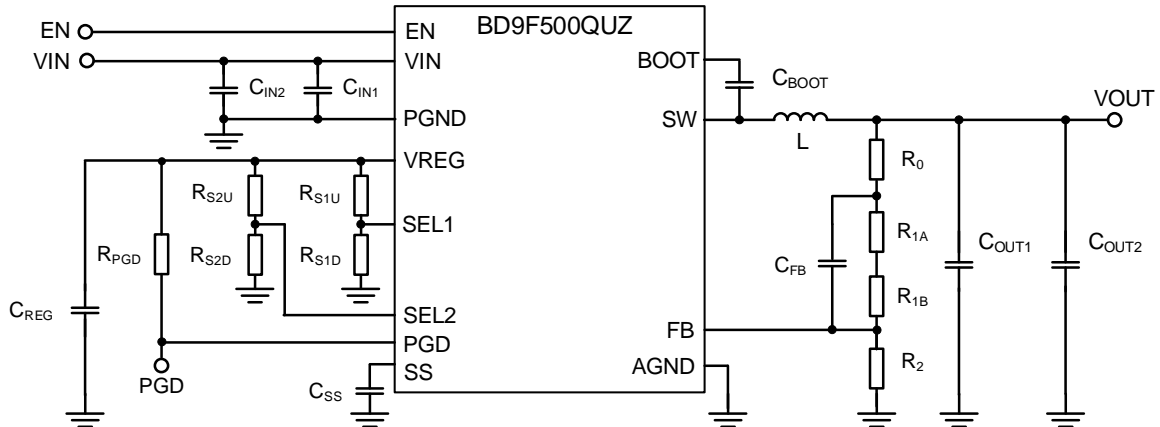


Figure 82. Application Circuit

Table 12. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	2.2 $\mu\text{H}$	FDSD0630-H-2R2M	7066	Murata
$C_{IN1}$ (Note 1)	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ (Note 2)	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ (Note 3)	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ (Note 4)	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ (Note 4)	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ (Note 5)	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	39 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H390JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	120 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1203	1005	ROHM
$R_{1B}$	330 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF3303	1005	ROHM
$R_2$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	-	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	Short	-	-	-
$R_0$ (Note 6)	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

4.  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$  – continued

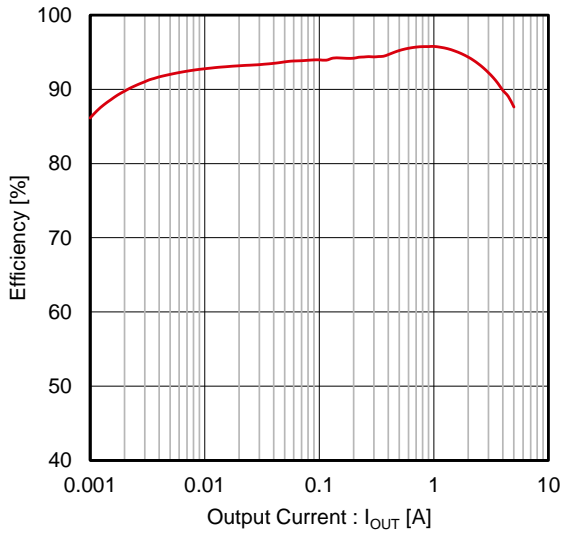


Figure 83. Efficiency vs Output Current

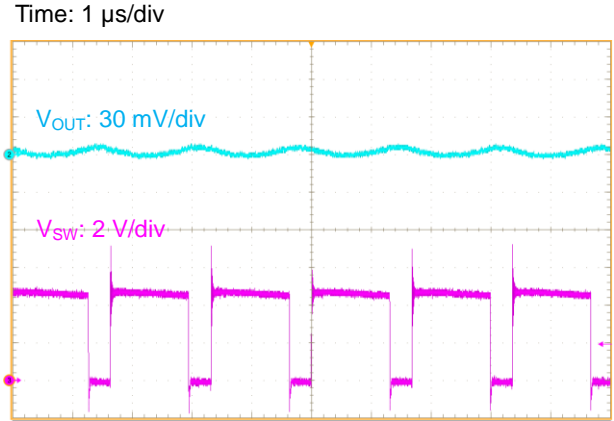


Figure 84. Output Ripple Voltage ( $I_{OUT} = 5\text{ A}$ )

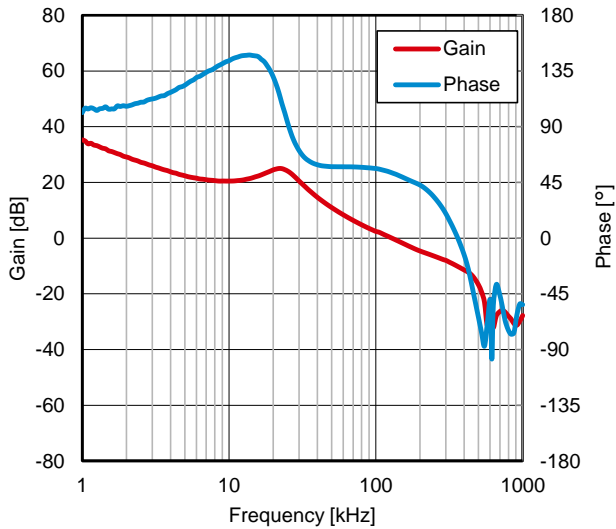


Figure 85. Frequency Characteristics ( $I_{OUT} = 3\text{ A}$ )

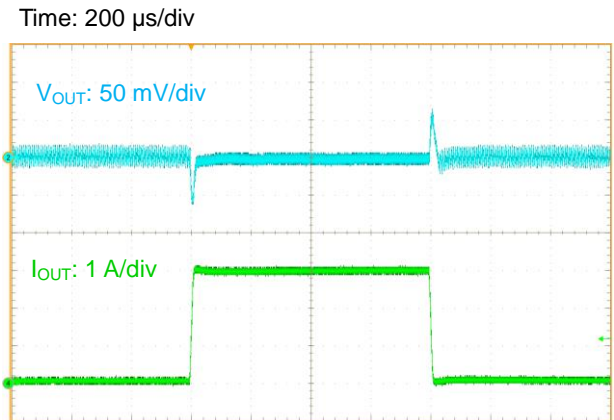


Figure 86. Load Transient Response ( $I_{OUT} = 0.1\text{ A to } 3.0\text{ A}$ )

## Application Examples – continued

5.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$ 

Table 13. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	12 V (Typ)
Output Voltage	$V_{OUT}$	1 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	1 MHz (Typ)
Operation Mode	-	Fixed PWM Mode
Temperature	$T_a$	25 °C

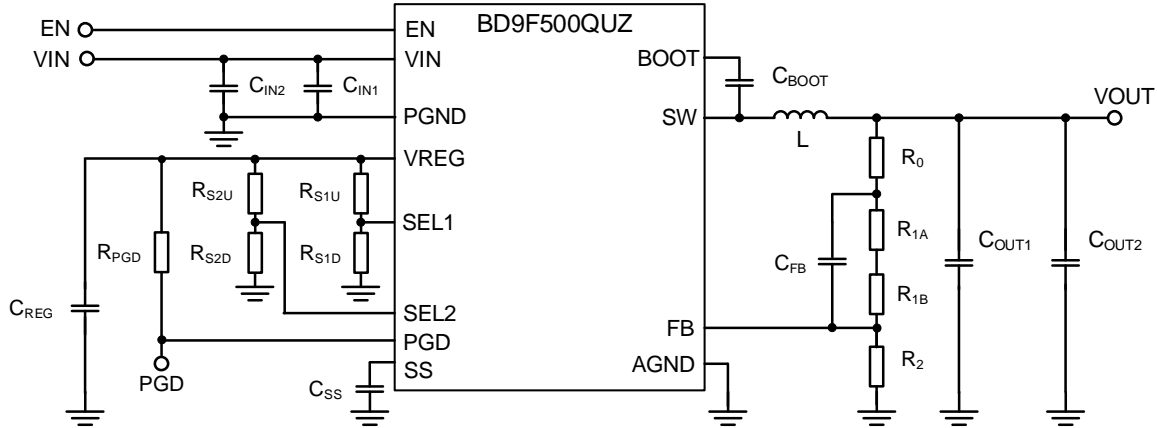


Figure 87. Application Circuit

Table 14. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	0.68 $\mu\text{H}$	FDSD0518-H-R68M	5249	Murata
$C_{IN1}$ <sup>(Note 1)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ <sup>(Note 2)</sup>	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ <sup>(Note 3)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ <sup>(Note 5)</sup>	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	27 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H270JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	Short	-	-	-
$R_{1B}$	180 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1803	1005	ROHM
$R_2$	270 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF2703	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	Short	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	-	-	-	-
$R_0$ <sup>(Note 6)</sup>	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

5.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $f_{SW} = 1\text{ MHz}$  – continued

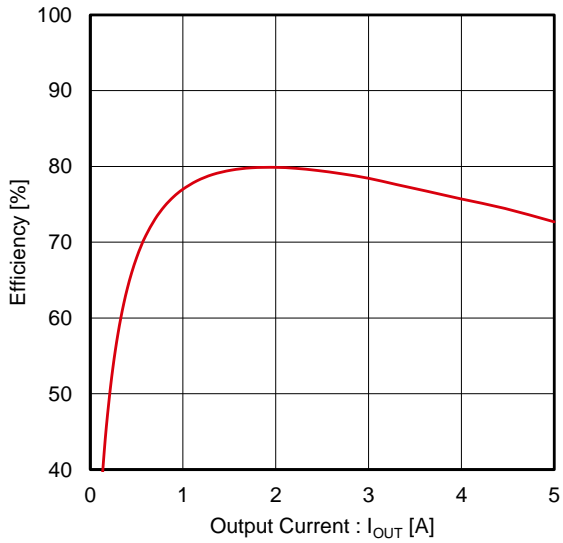


Figure 88. Efficiency vs Output Current

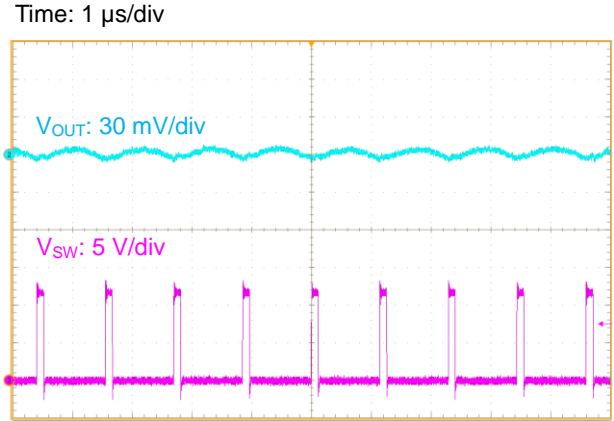


Figure 89. Output Ripple Voltage ( $I_{OUT} = 5\text{ A}$ )

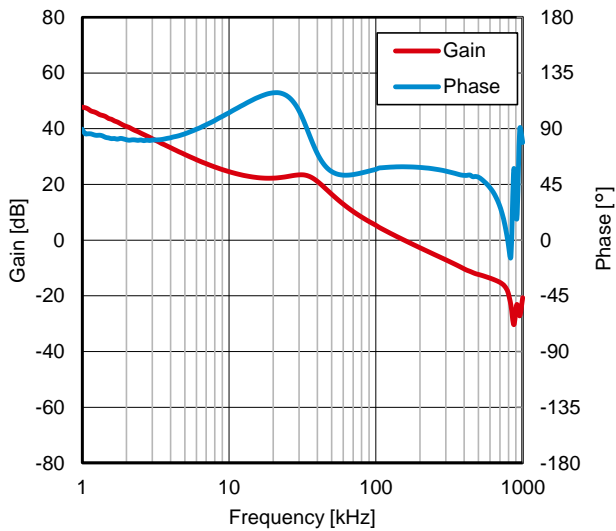


Figure 90. Frequency Characteristics ( $I_{OUT} = 3\text{ A}$ )

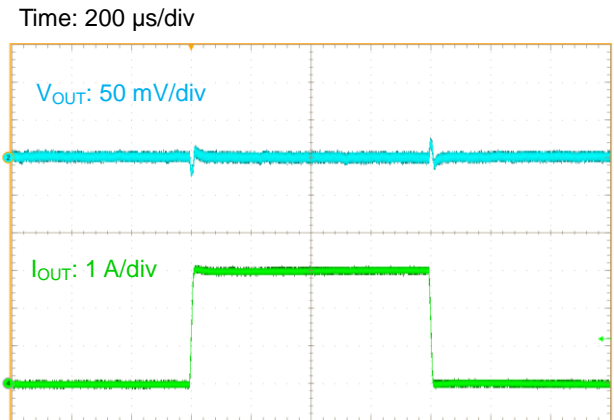


Figure 91. Load Transient Response ( $I_{OUT} = 0\text{ A}$  to 3 A)

## Application Examples – continued

6.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$ 

Table 15. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	12 V (Typ)
Output Voltage	$V_{OUT}$	1 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	5 A
Switching Frequency	$f_{SW}$	600 kHz (Typ)
Operation Mode	-	Fixed PWM Mode
Temperature	$T_a$	25 °C

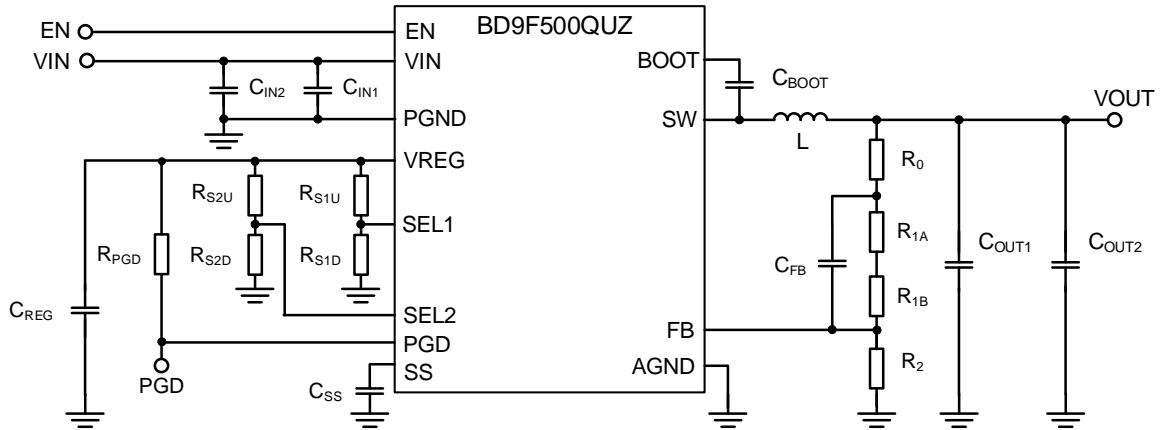


Figure 92. Application Circuit

Table 16. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	1.5 $\mu\text{H}$	FDSD0630-H-1R5N	7066	Murata
$C_{IN1}$ <sup>(Note 1)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ <sup>(Note 2)</sup>	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ <sup>(Note 3)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ <sup>(Note 5)</sup>	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	33 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H330JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	Short	-	1005	ROHM
$R_{1B}$	180 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1803	1005	ROHM
$R_2$	270 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF2703	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	-	-	-	-
$R_{S1D}$	-	-	-	-
$R_{S2U}$	-	-	-	-
$R_{S2D}$	-	-	-	-
$R_0$ <sup>(Note 6)</sup>	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

6.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $f_{SW} = 600\text{ kHz}$  – continued

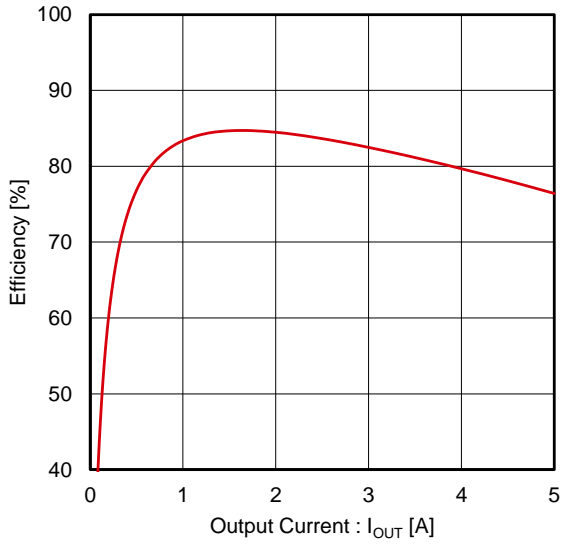


Figure 93. Efficiency vs Output Current

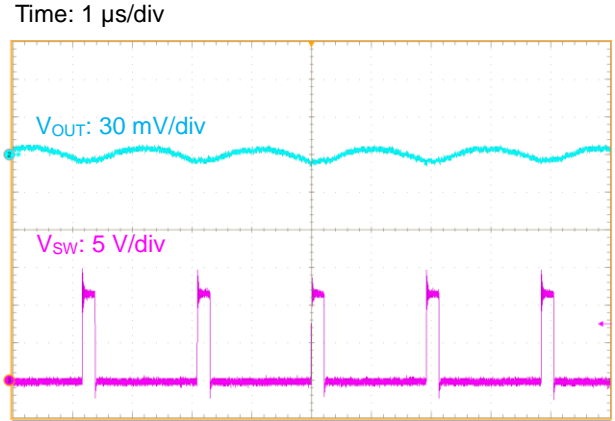


Figure 94. Output Ripple Voltage ( $I_{OUT} = 5\text{ A}$ )

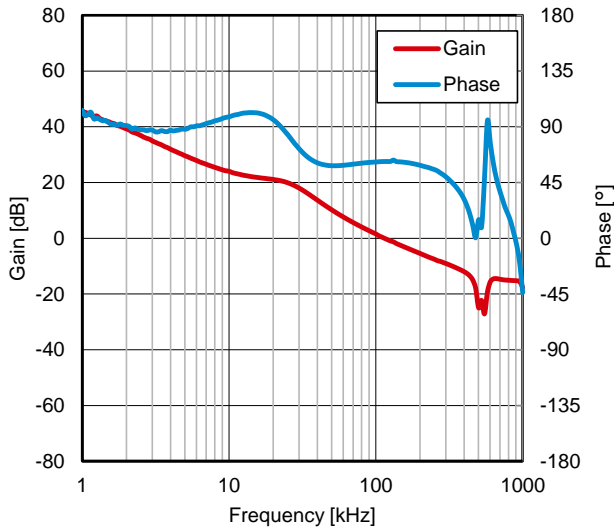


Figure 95. Frequency Characteristics ( $I_{OUT} = 3\text{ A}$ )

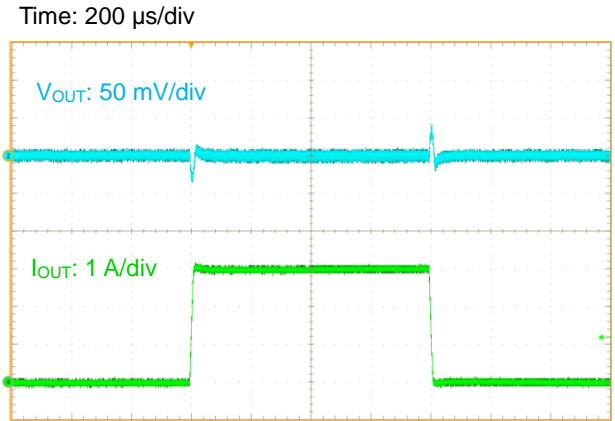


Figure 96. Load Transient Response ( $I_{OUT} = 0\text{ A}$  to  $3\text{ A}$ )



## Application Examples – continued

7.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{SW} = 2.2\text{ MHz}$ 

Table 17. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	$V_{IN}$	12 V (Typ)
Output Voltage	$V_{OUT}$	3.3 V (Typ)
Maximum Output Current	$I_{OUTMAX}$	3 A
Switching Frequency	$f_{SW}$	2.2 MHz (Typ)
Operation Mode	-	Fixed PWM Mode
Temperature	$T_a$	25 °C

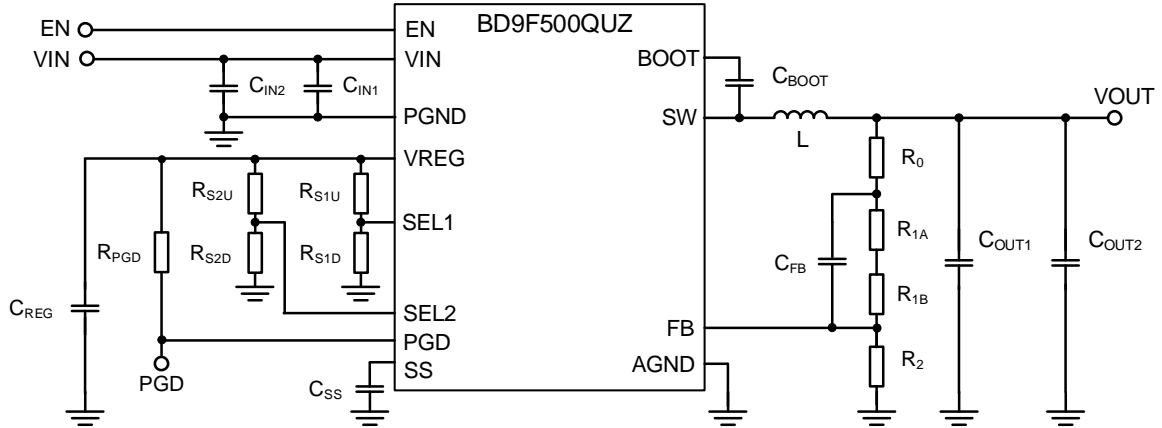


Figure 97. Application Circuit

Table 18. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L	1.0 $\mu\text{H}$	FDSD0518-H-1R0M	5249	Murata
$C_{IN1}$ <sup>(Note 1)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{IN2}$ <sup>(Note 2)</sup>	10 $\mu\text{F}$ (50 V, X5R, $\pm 20\%$ )	UMK325BJ106MM-P	3225	TAIYO YUDEN
$C_{BOOT}$ <sup>(Note 3)</sup>	0.1 $\mu\text{F}$ (50 V, X5R, $\pm 10\%$ )	UMK105BJ104KV-F	1005	TAIYO YUDEN
$C_{OUT1}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{OUT2}$ <sup>(Note 4)</sup>	22 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK212BBJ226MG-TT	2012	TAIYO YUDEN
$C_{REG}$ <sup>(Note 5)</sup>	2.2 $\mu\text{F}$ (25 V, X5R, $\pm 20\%$ )	TMK105CBJ225MV-F	1005	TAIYO YUDEN
$C_{FB}$	33 pF (50 V, C0G, $\pm 5\%$ )	GRM0335C1H330JA01	0603	Murata
$C_{SS}$	-	-	-	-
$R_{1A}$	1.5 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1500	1005	ROHM
$R_{1B}$	120 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1203	1005	ROHM
$R_2$	27 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF2702	1005	ROHM
$R_{PGD}$	100 k $\Omega$ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
$R_{S1U}$	Short	-	-	-
$R_{S1D}$	-	-	-	-
$R_{S2U}$	Short	-	-	-
$R_{S2D}$	-	-	-	-
$R_0$ <sup>(Note 6)</sup>	Short	-	-	-

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1  $\mu\text{F}$  ceramic capacitor  $C_{IN1}$  as close as possible to the VIN pin and the PGND pin.

(Note 2) For the input capacitor  $C_{IN2}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3  $\mu\text{F}$ .

(Note 3) For the bootstrap capacitor  $C_{BOOT}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu\text{F}$ .

(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor  $C_{OUT1}$  and  $C_{OUT2}$ , the loop response characteristics may change. Confirm with the actual application.

(Note 5) For the VREG capacitor  $C_{REG}$ , take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu\text{F}$ .

(Note 6)  $R_0$  is an option, used for feedback's frequency response measurement. By inserting a resistor at  $R_0$ , it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

7.  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $f_{sw} = 2.2\text{ MHz}$  – continued

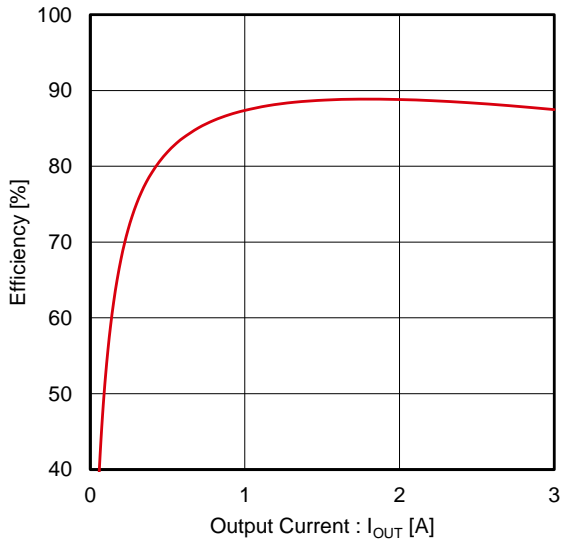


Figure 98. Efficiency vs Output Current

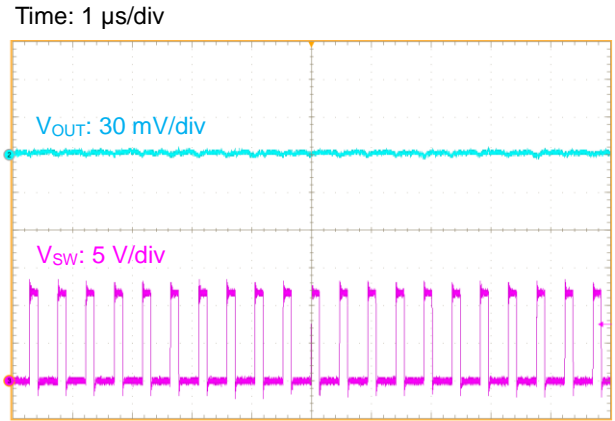


Figure 99. Output Ripple Voltage ( $I_{OUT} = 3\text{ A}$ )

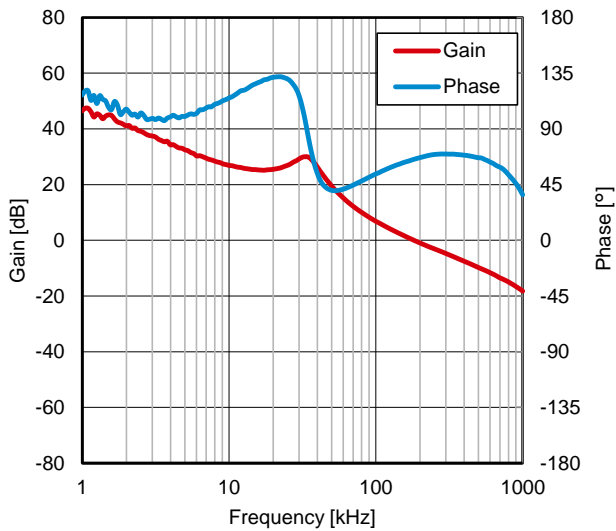


Figure 100. Frequency Characteristics ( $I_{OUT} = 2\text{ A}$ )

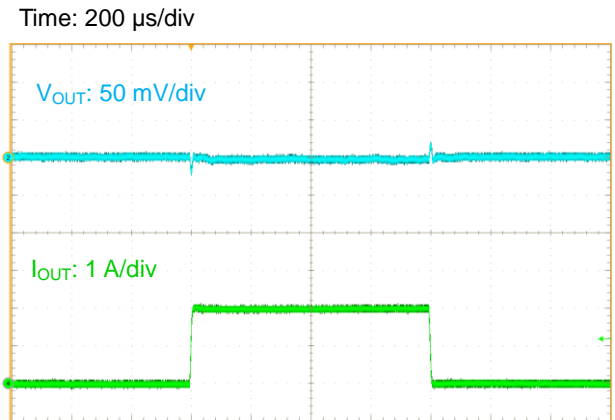


Figure 101. Load Transient Response ( $I_{OUT} = 0\text{ A}$  to  $2\text{ A}$ )

## Selection of Components Externally Connected

Contact us if not use the recommended component values in [Application Examples](#).

### 1. Input Capacitor

Use ceramic type capacitor for the input capacitor. The input capacitor is used to reduce the input ripple noise and it is effective by being placed as close as possible to the VIN pin. Set the capacitor value so that it does not fall to 3  $\mu\text{F}$  considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. The PCB layout and the position of the capacitor may lead to IC malfunction. Refer to the notes on the PCB layout on [PCB Layout Design](#) when designing PCB layout. In addition, the capacitor with value 0.1  $\mu\text{F}$  can be connected as close as possible to the VIN pin and the PGND pin in order to reduce the high frequency noise.

### 2. Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. For recommended inductance, use the values listed in Table 19.

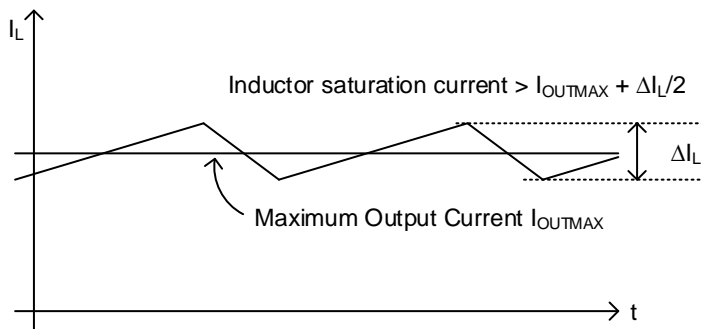


Figure 102. Waveform of Inductor Current

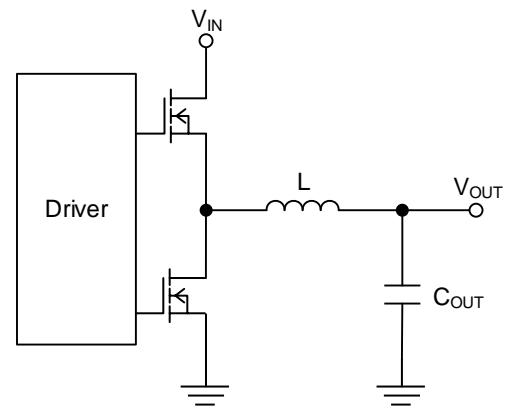


Figure 103. Output LC Filter Circuit

For example, given that  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $L = 1.5\text{ }\mu\text{H}$ , and the switching frequency  $f_{SW} = 1.0\text{ MHz}$ , Inductor current  $\Delta I_L$  can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L} = 1.595\text{ [A]}$$

The rated current of the inductor (Inductor saturation current) must be larger than the sum of the maximum output current  $I_{OUTMAX}$  and 1/2 of the inductor ripple current  $\Delta I_L$ .

Use ceramic type capacitor for the output capacitor  $C_{OUT}$ . For recommended actual capacitance, use the values listed in Table 19.  $C_{OUT}$  affects the output ripple voltage. Select  $C_{OUT}$  so that it must satisfy the required ripple voltage characteristics.

The output ripple voltage can be estimated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left( R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

where:

$R_{ESR}$  is the Equivalent Series Resistance (ESR) of the output capacitor.

For example, given that  $C_{OUT} = 44\text{ }\mu\text{F}$  and  $R_{ESR} = 3\text{ m}\Omega$ ,  $\Delta V_{RPL}$  can be calculated as below.

$$\Delta V_{RPL} = 1.595\text{ A} \times \left( 3\text{ m}\Omega + \frac{1}{8 \times 44\text{ }\mu\text{F} \times 1\text{ MHz}} \right) = 9.3\text{ [mV]}$$

## 2. Output LC Filter – continued

In addition, the total capacitance connected to  $V_{OUT}$  needs to satisfy the value obtained by the following equation.

$$C_{OUTMAX} < \frac{t_{SSMIN}}{V_{OUT}} \times (I_{OUTMAX} + \frac{\Delta I_L}{2} - I_{OUTSS}) \text{ [F]}$$

where:

$t_{SSMIN}$  is the minimum soft start time.

$V_{OUT}$  is the output voltage.

$I_{OUTMAX}$  is the maximum output current.

$\Delta I_L$  is the inductor current.

$I_{OUTSS}$  is the maximum output current during soft start.

For example, given that  $V_{IN} = 12 \text{ V}$ ,  $V_{OUT} = 3.3 \text{ V}$ ,  $L = 1.5 \mu\text{H}$ ,  $f_{SW} = 1 \text{ MHz}$  (Typ),  $t_{SSMIN} = 1.4 \text{ ms}$  ( $C_{SS} = \text{OPEN}$ ),  $I_{OUTMAX} = 5 \text{ A}$ , and  $I_{OUTSS} = 5 \text{ A}$ ,  $C_{OUTMAX}$  can be calculated as below.

$$C_{OUTMAX} < \frac{1.4 \text{ ms}}{3.3 \text{ V}} \times (5 \text{ A} + \frac{1.595 \text{ A}}{2} - 5 \text{ A}) = 338 \text{ } [\mu\text{F}]$$

If the total capacitance connected to  $V_{OUT}$  is larger than  $C_{OUTMAX}$ , over current protection may be activated by the inrush current at startup and prevented to turn on the output. Confirm this on the actual application.

Table 19. Recommended inductance and output capacitance

Frequency [MHz]	$V_{IN}$ [V]	$V_{OUT}$ [V]	$I_{OUTMAX}$ [A]	Inductor L [ $\mu\text{H}$ ]	$C_{OUT\_EFF}$ <sup>(Note 1)</sup> [ $\mu\text{F}$ ]
0.6	12	3.3	5	3.3	25 to 50
0.6	12	3.3	3	4.7	25 to 50
0.6	24	3.3	5	3.3	25 to 50
0.6	24	3.3	3	4.7	25 to 50
0.6	5	3.3	5	2.2	25 to 50
0.6	5	3.3	3	2.2	25 to 50
0.6	12	1	5	1.5	35 to 50
0.6	12	1	3	1.5	35 to 50
0.6	5	1	5	1.5	35 to 50
0.6	5	1	3	1.5	35 to 50
0.6	12	5	5	4.7	30 to 50
0.6	12	5	3	5.6	30 to 50
0.6	24	5	5	4.7	30 to 50
0.6	24	5	3	5.6	30 to 50
0.6	24	12	5	6.8	45 to 60
0.6	24	12	3	8.2	45 to 60
1	12	3.3	5	1.5	25 to 50
1	12	3.3	3	2.2	25 to 50
1	24	3.3	5	1.5	25 to 50
1	24	3.3	3	2.2	25 to 50
1	5	3.3	5	1	25 to 50
1	5	3.3	3	1.5	25 to 50
1	12	1	5	0.68	25 to 50
1	12	1	3	1	25 to 50
1	5	1	5	0.68	25 to 50
1	5	1	3	1	25 to 50
1	12	5	5	3.3	20 to 50
1	12	5	3	3.3	20 to 50
1	24	5	5	3.3	20 to 50
1	24	5	3	3.3	20 to 50
1	24	12	5	4.7	30 to 50
1	24	12	3	5.6	30 to 50
2.2	12	3.3	3	1	20 to 50
2.2	24	3.3	3	1	20 to 50

(Note 1)  $C_{OUT\_EFF}$  is the sum of actual output capacitance.

## Selection of Components Externally Connected – continued

### 3. Output Voltage Setting, FB Capacitor

The output voltage can be set by the feedback resistance ratio connected to the FB pin. For recommended  $R_1$  and  $R_2$ , use the values listed in Table 20.

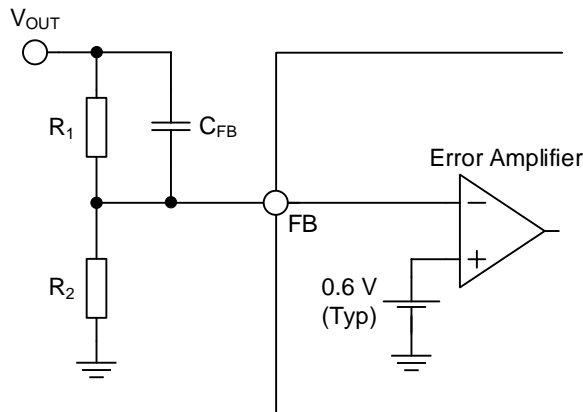


Figure 104. Feedback Resistor Circuit

The output voltage  $V_{OUT}$  can be calculated as below.

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 0.6 \text{ [V]}$$

$$0.6 \leq V_{OUT} \leq 14 \text{ [V]}$$

$$V_{OUT} \leq (V_{IN} \times 0.8) \text{ [V]}$$

The Constant On-Time control required the sufficient ripple voltage on FB voltage for the operation stability. This device is designed to correspond to low ESR output capacitors by injecting the ripple voltage to FB voltage inside the IC. The FB capacitor  $C_{FB}$  should be set with the following expression as typical value in order to inject an appropriate ripple. For recommended  $C_{FB}$ , use the values listed in Table 20.

600 kHz setting

$$C_{FB} = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN})}{f_{SW} \times 5.25 \times 10^4} \text{ [F]}$$

where:

$V_{IN}$  is the input voltage.

$V_{OUT}$  is the output voltage.

$f_{SW}$  is the switching frequency 600 kHz (Typ).

1MHz, 2.2MHz setting

$$C_{FB} = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN})}{f_{SW} \times 3.5 \times 10^4} \text{ [F]}$$

where:

$V_{IN}$  is the input voltage.

$V_{OUT}$  is the output voltage.

$f_{SW}$  is the switching frequency 1 MHz, 2.2 MHz (Typ).

Load transient response and the loop stability depends on  $L$ ,  $C_{OUT}$ ,  $R_1$ ,  $R_2$ , and  $C_{FB}$ . Actually, these characteristics may change depending on PCB layout, wiring, the type of components, and the conditions (temperature, etc.). Be sure to check them on the actual application.

### 3. Output Voltage Setting, FB Capacitor – continued

Table 20. Recommended feedback resistance, C<sub>FB</sub> capacitance

Frequency [MHz]	V <sub>IN</sub> [V]	V <sub>OUT</sub> [V]	R <sub>1</sub> [kΩ]	R <sub>2</sub> [kΩ]	C <sub>FB</sub> [pF]
0.6	12	3.3	1.5 + 120	27	82
0.6	24	3.3	1.5 + 120	27	82
0.6	5	3.3	120 + 330	100	39
0.6	12	1	180	270	33
0.6	5	1	180	270	27
0.6	12	5	220	30	100
0.6	24	5	220	30	100
0.6	24	12	68 + 560	33	180
1	12	3.3	1.5 + 120	27	82
1	24	3.3	1.5 + 120	27	82
1	5	3.3	120 + 330	100	33
1	12	1	180	270	27
1	5	1	180	270	22
1	12	5	220	30	100
1	24	5	220	30	100
1	24	12	68 + 560	33	180
2.2	12	3.3	1.5 + 120	27	33
2.2	24	3.3	1.5 + 120	27	33

### 4. Soft Start Capacitor (Soft Start Time Setting)

The soft start time  $t_{SS}$  depends on the value of the capacitor connected to the SS pin. The  $t_{SS}$  is 2 ms (Typ) when the SS pin is left floating. The capacitor connected to the SS pin makes  $t_{SS}$  more than 2 ms. The  $t_{SS}$  and  $C_{SS}$  can be calculated using below equation. The  $C_{SS}$  should be set in the range between 0.01  $\mu$ F and 0.1  $\mu$ F.

$$t_{SS} = \frac{C_{SS} \times 0.6 \times 1.3}{I_{SS}} \text{ [s]}$$

where:

$I_{SS}$  is the Soft Start Charge Current 2.0  $\mu$ A (Typ).

With  $C_{SS} = 0.022 \mu$ F,  $t_{SS}$  can be calculated as below.

$$t_{SS} = \frac{0.022 \mu\text{F} \times 0.6 \times 1.3}{2.0 \mu\text{A}} = 8.58 \text{ [ms]}$$

### 5. VREG Capacitor

The VREG capacitor 2.2  $\mu$ F is recommended. Connect the capacitor between the VREG pin and the AGND pin. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the actual capacitance of no less than 0.82  $\mu$ F.

### 6. Bootstrap Capacitor

The bootstrap capacitor 0.1  $\mu$ F is recommended. Connect the capacitor between the SW pin and the BOOT pin. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the actual capacitance of no less than 0.022  $\mu$ F.

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 105-a to Figure 105-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 105-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 105-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 105-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

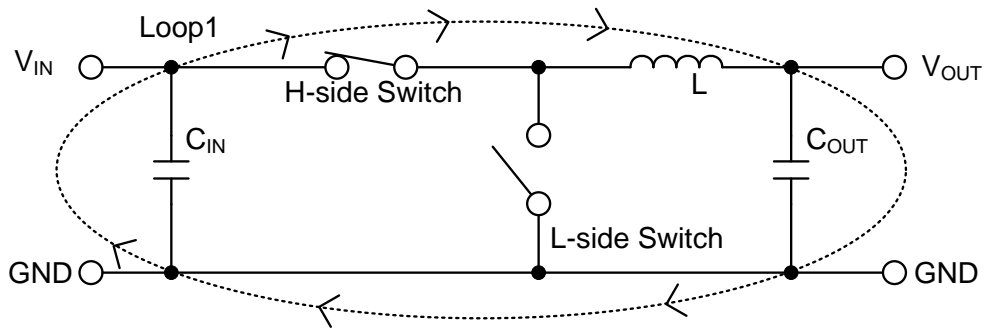


Figure 105-a. Current Path when H-side Switch = ON, L-side Switch = OFF

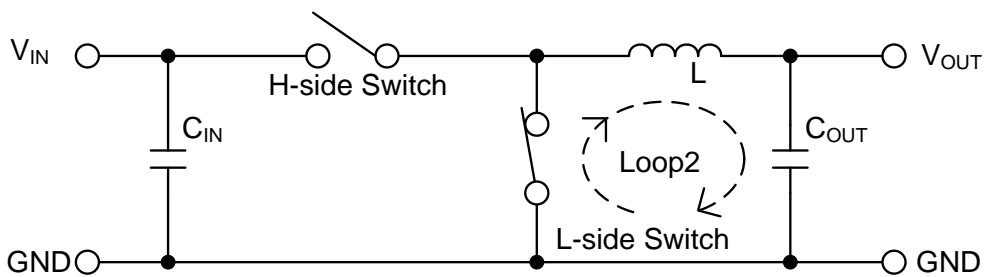


Figure 105-b. Current Path when H-side Switch = OFF, L-side Switch = ON

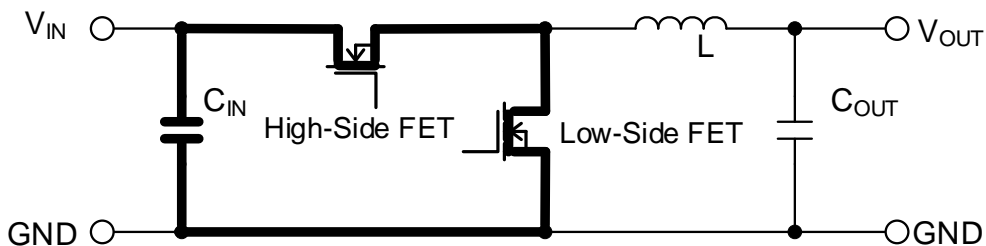


Figure 105-c. Difference of Current and Critical Area in Layout

## PCB Layout Design – continued

When designing the PCB layout, pay attention to the following points:

- Connect the input capacitor  $C_{IN1}$  and  $C_{IN2}$  as close as possible to the VIN pin and the PGND pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern L as thick and as short as possible.
- The feedback line connected to the FB pin should be as far away from the SW nodes as possible.
- Place the output capacitor  $C_{OUT}$  away from input capacitor  $C_{IN1}$  and  $C_{IN2}$  to avoid harmonics noise from the input.
- Separate the reference ground and the power ground and connect them through VIA. The reference ground should be connected to the power ground that is close to the output capacitor  $C_{OUT}$ . It is because  $C_{OUT}$  has less high frequency switching noise.
- To provide excellent heat dissipation characteristics connect the VIN pins to the PCB VIN pattern by using thermal vias.
- Place the bypass capacitor between the VREG and AGND pins at a position as close as possible to the pin.
- When the SEL1 and SEL2 pins are left open, the parasitic capacitance with the VIN, SW, and BOOT pins should be 0.2 pF or less.
- $R_0$  is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into  $R_0$ , it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc.  $R_0$  is short-circuited for normal use.



PCB Layout Design – continued

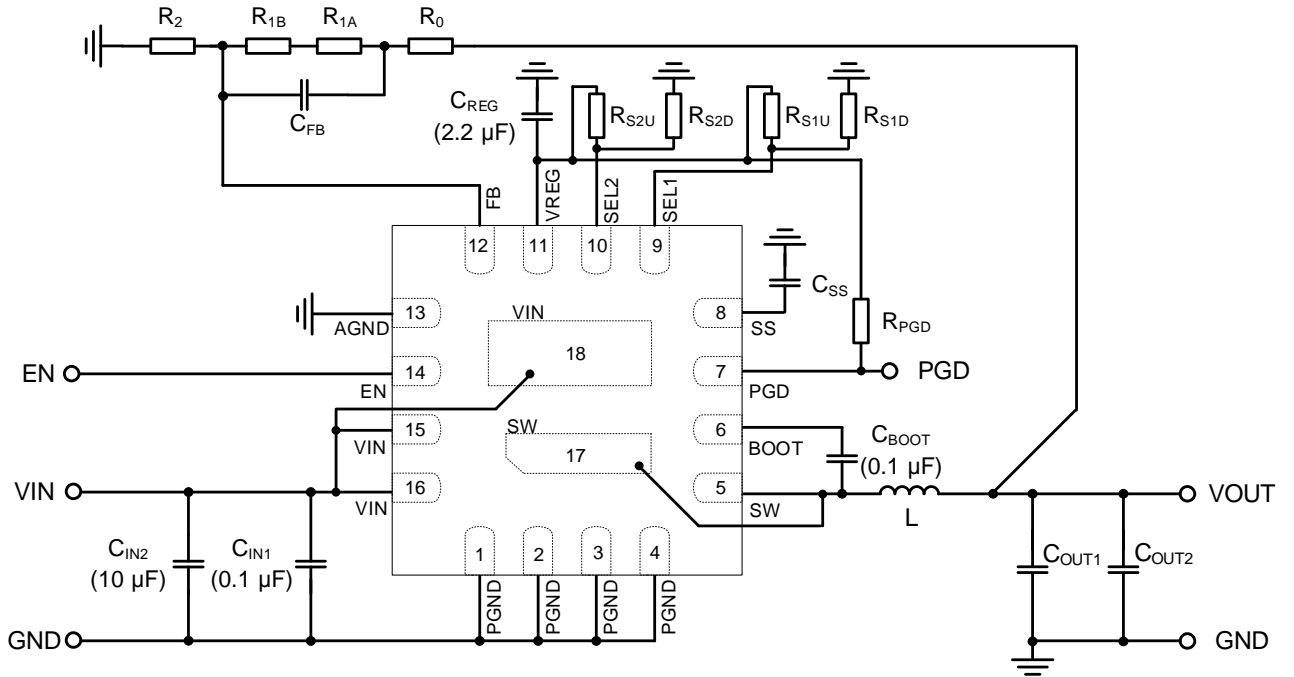


Figure 106. Application Circuit

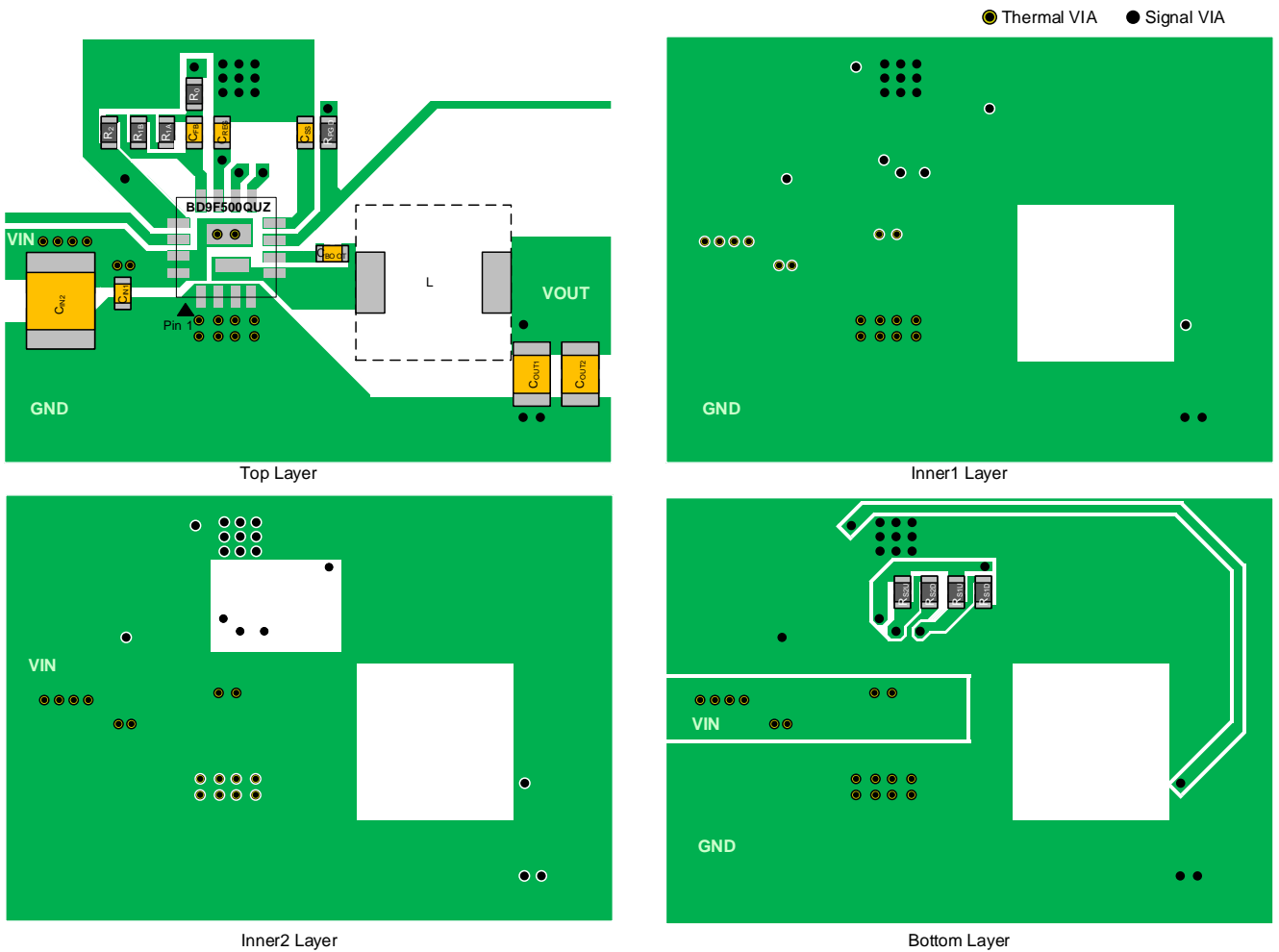
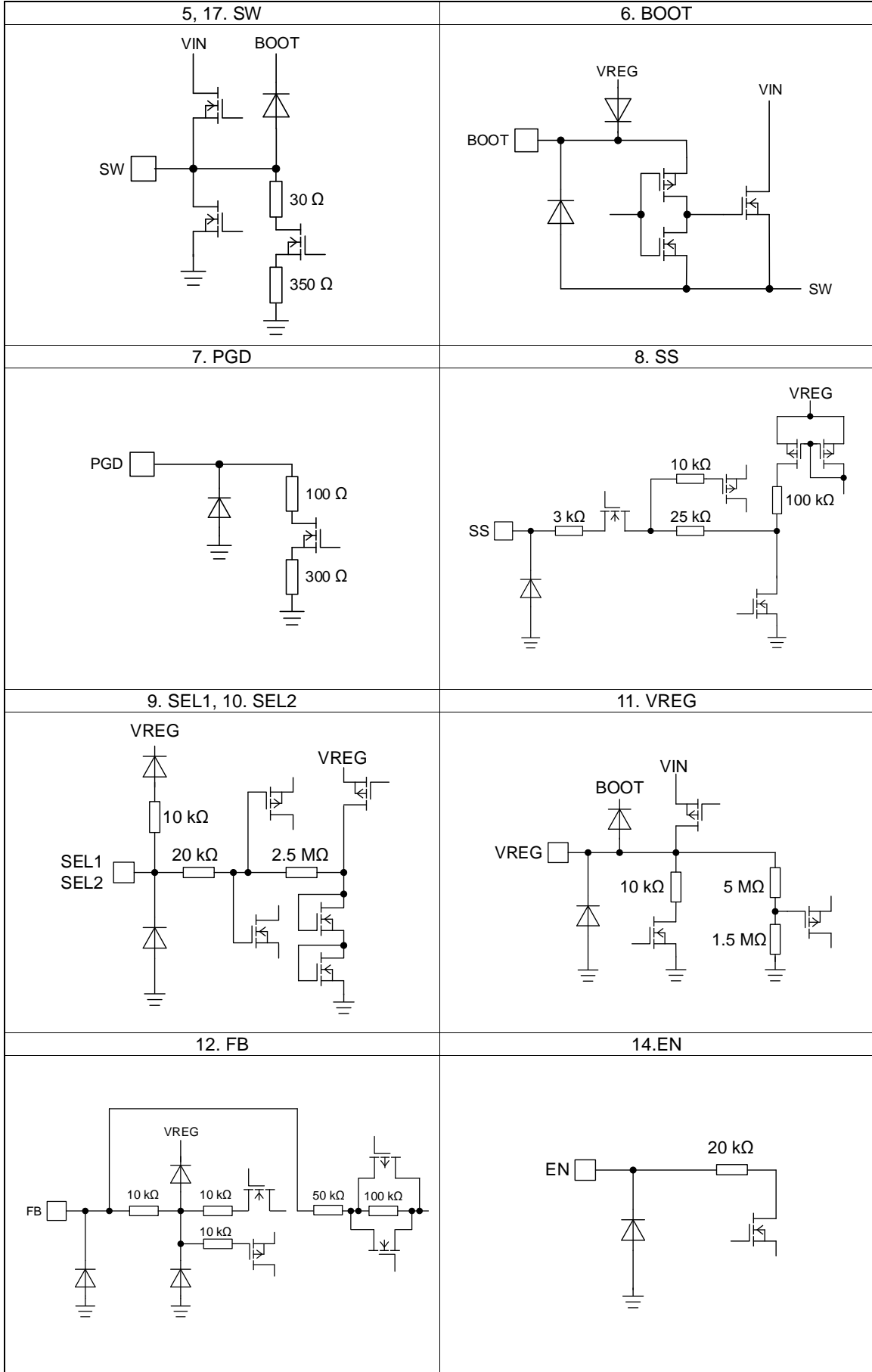


Figure 107. Example of PCB Layout

I/O Equivalence Circuits



(Note) Resistor values are typical.

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**10. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

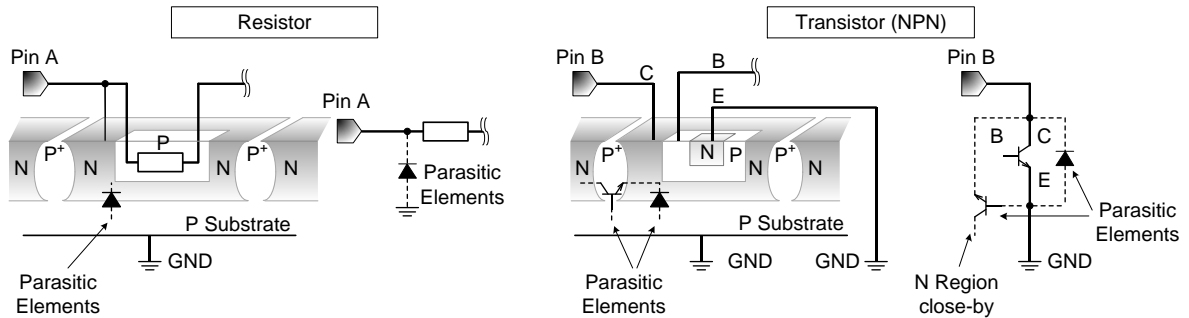


Figure 108. Example of Monolithic IC Structure

**11. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**12. Thermal Shutdown Circuit (TSD)**

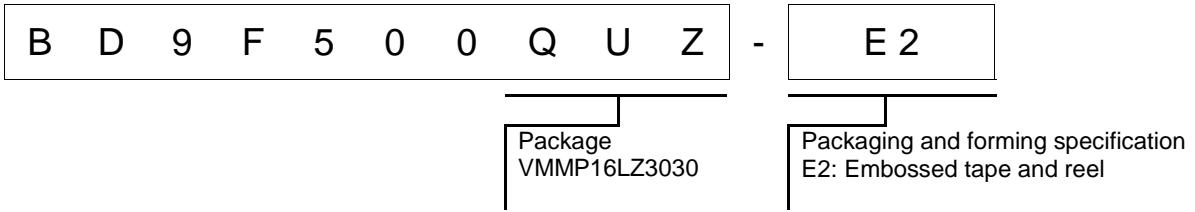
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

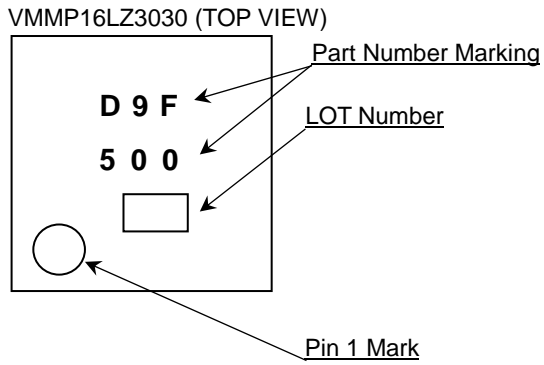
**13. Over Current Protection Circuit (OCP)**

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

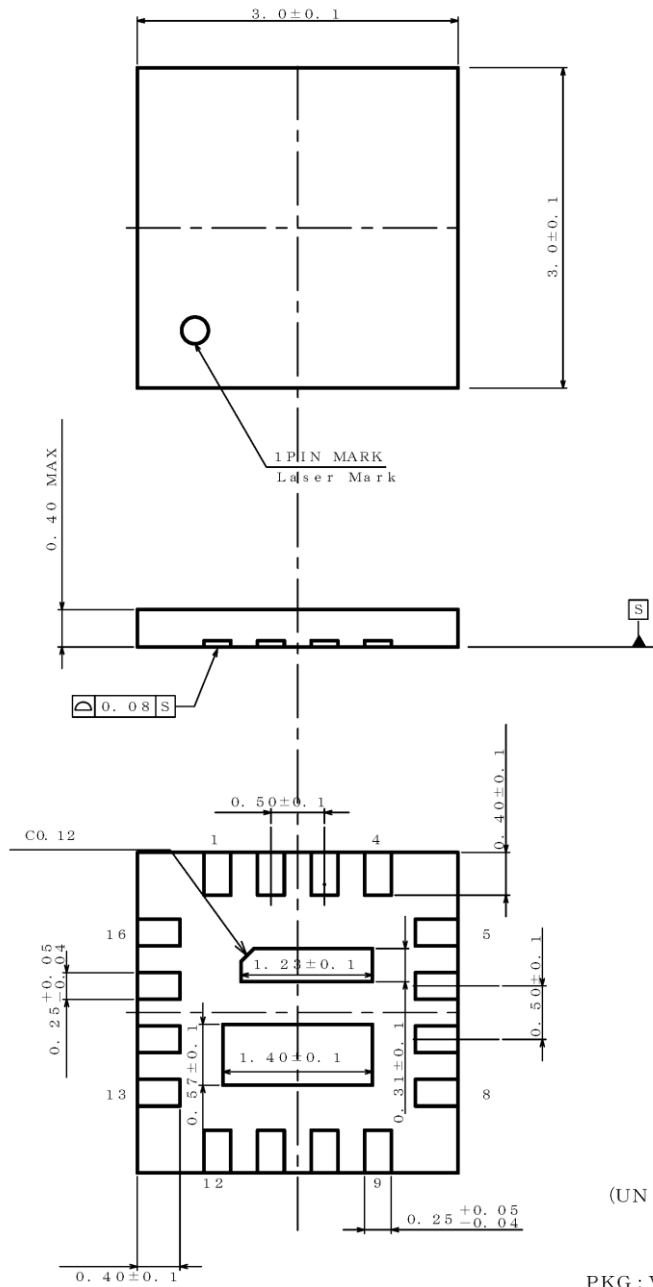


Marking Diagram



Physical Dimension and Packing Information

Package Name	VMMP16LZ3030
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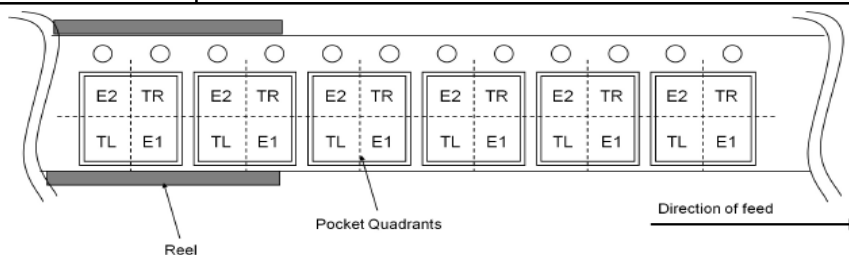
(UNIT : mm)

PKG : VMMP16LZ3030

Drawing No. EX768-5002-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



**Revision History**

Date	Revision	Changes
02.Apr.2020	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- Confirm that operation temperature is within the specified range described in the product specification.
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  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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