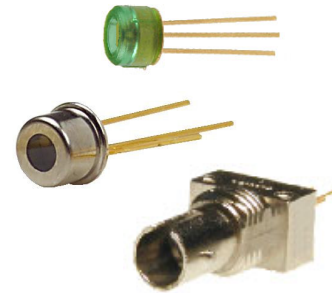


Fiber Optic Receiver

OPF500 Series



Features:

- Interfaces with all logic circuits
- Two output options
- Optimized for fiber optic applications using 50 to 200 micron fibers
- Data rate to 200kbps NRZ
- Available with multiple packaging options

Description:

The OPF500 series receiver contains a monolithic integrated circuit which incorporates a photodiode, linear amplifier, a voltage regulator, and a Schmitt trigger on a single silicon chip. These receivers are designed for short haul fiber optic systems using 850 nm LEDs such as Optek’s OPF300 series.

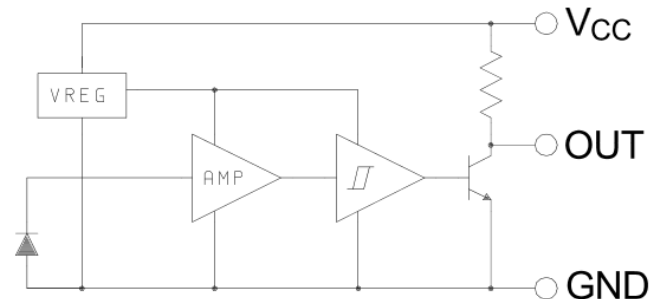
These devices feature TTL/LSTTL compatible logic level output. An internal voltage regulator allows operation with supply voltages ranging from 4.5V to 16V.

Applications:

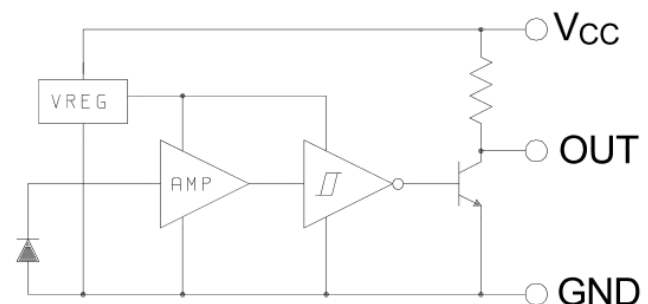
- Industrial Ethernet equipment
- Copper-to-fiber media conversion
- Intra-system fiber optic links
- Video surveillance systems

Part Ordering Information	
Part Number	Description
OPF500	Buffer, 10kW Pull-Up Plastic Cap Component
OPF505	Buffer, 10kW Pull-Up Metal Can Component
OPF507	Buffer, 10kW Pull-Up Metal ST Receptacle

Buffer/10K PU



Inverter/10K PU



RoHS



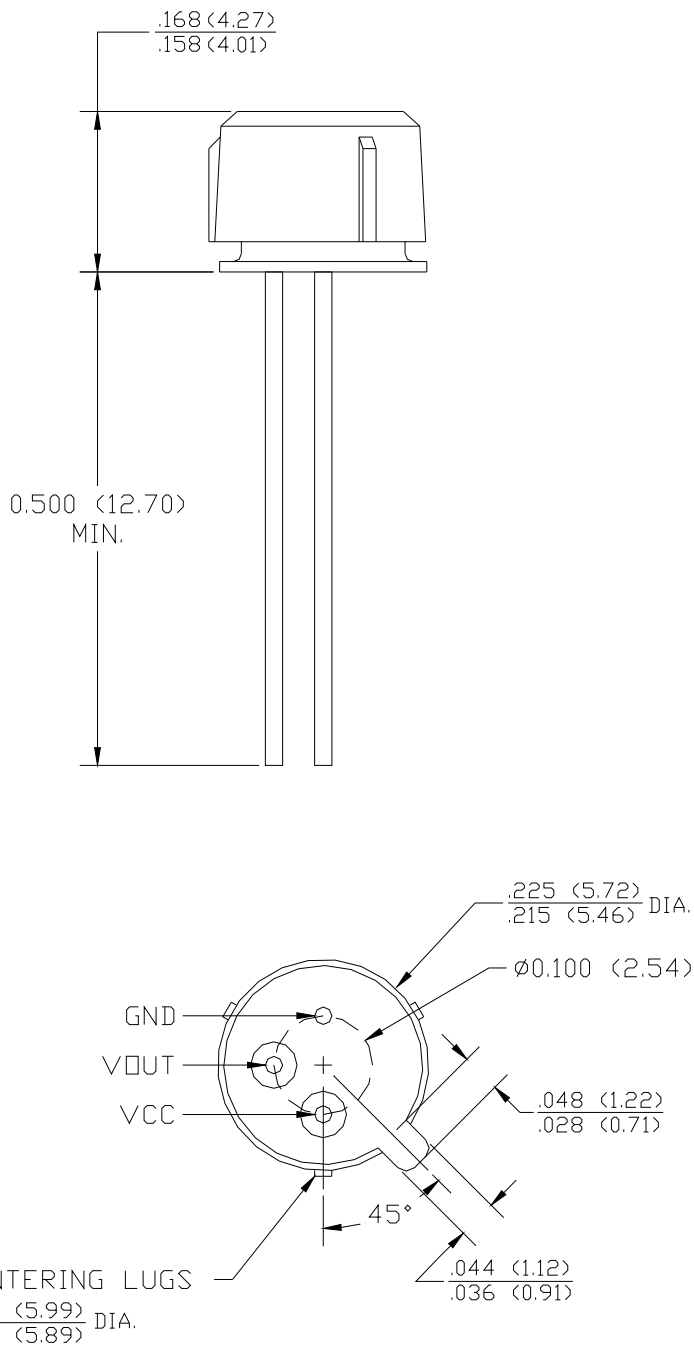
This component is susceptible to damage from electrostatic discharge (ESD). Normal static precautions should be taken in handling and assembly of this component to prevent ESD damage or degradation.

General Note

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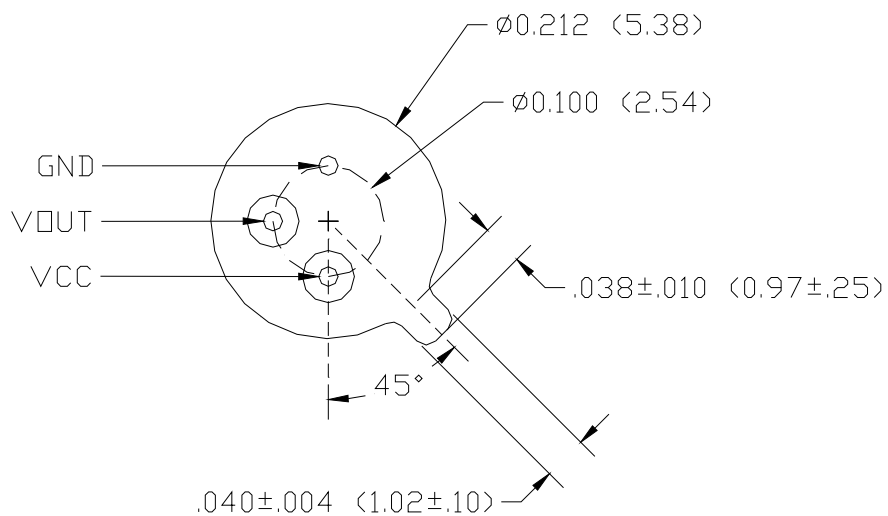
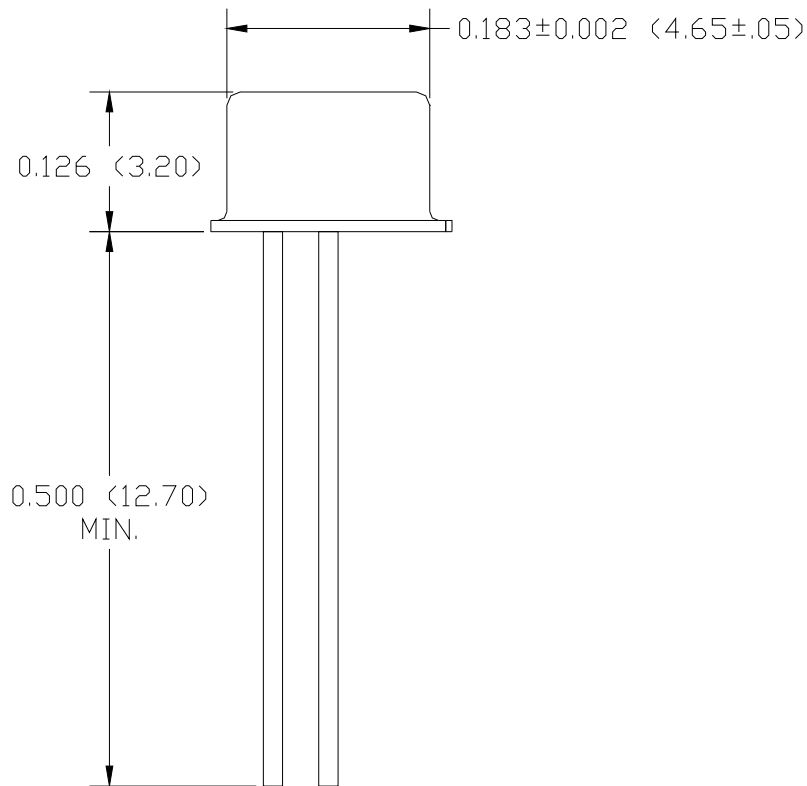
Mechanical Outline—OPF500



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Mechanical Outline—OPF505

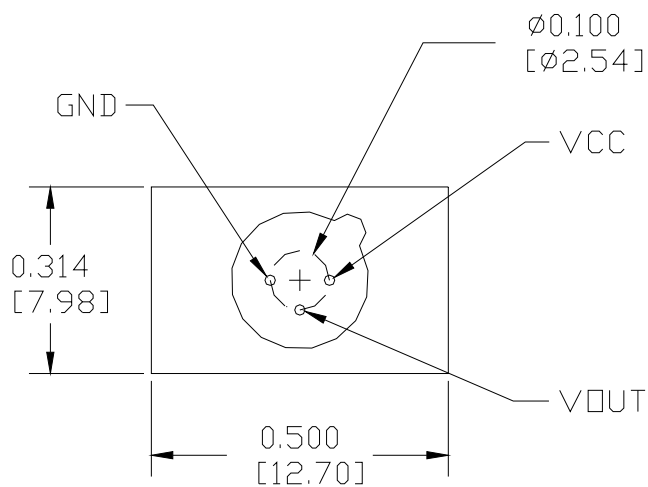
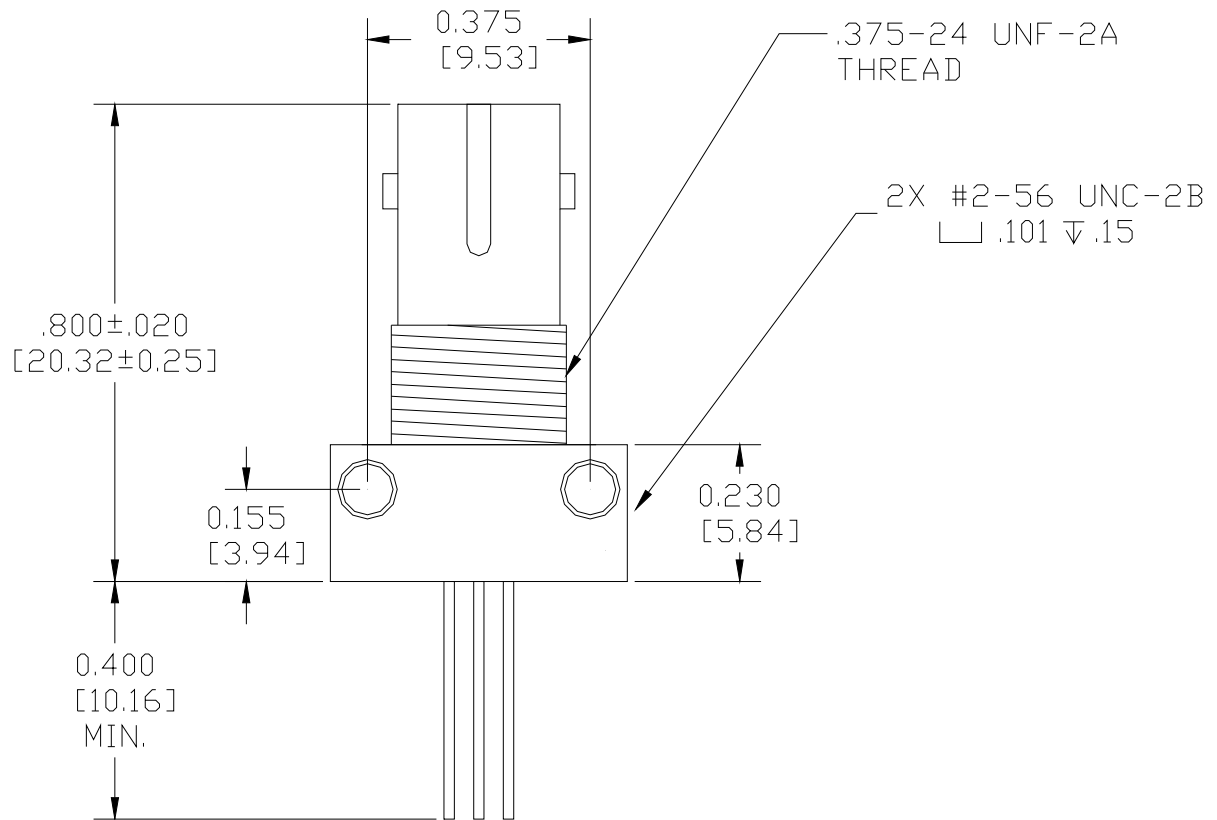


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Mechanical Outline—OPF507



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Electrical Specifications

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Storage Temperature	65° C to +100° C
Operating Temperature	-40° C to +85° C
Lead Soldering Temperature (for 10 seconds)	260° C
Supply Voltage	18 V
Sinking Current	16 mA
Power Dissipation	200 mW
Open Collector Power Distribution	40mW
Voltage at Output	30 V

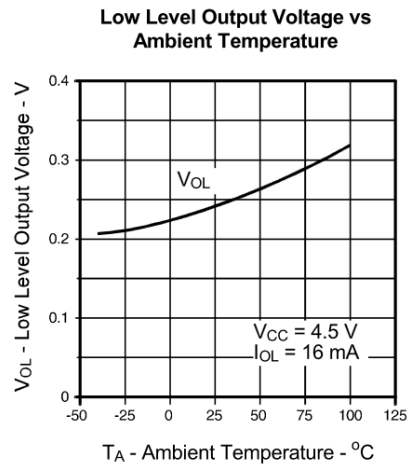
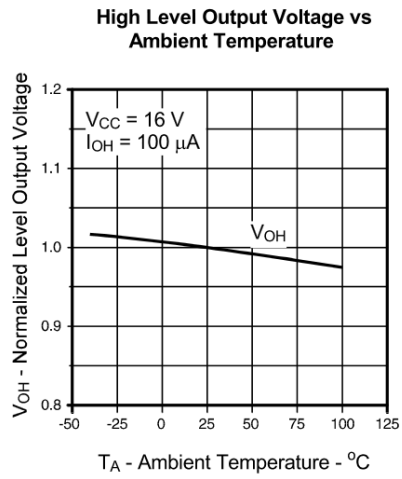
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{CC}	Supply Voltage	4.5		16.0	V	
V_{OH}	High Level Output Voltage	$V_{CC} - 1.5$			V	Buffer: $P_{IN} > 2.0 \mu\text{W}$ Inverter: $P_{IN} < 0.1 \mu\text{W}$
V_{OL}	Low Level Output Voltage			0.4	V	Buffer: $P_{IN} < 0.1 \mu\text{W}$ Inverter: $P_{IN} > 2.0 \mu\text{W}$
I_{CC}	Supply Current		5.0	12.0	mA	No output load
P_{IN}	Input Sensitivity			2.0	μW	$\lambda_p = 850 \text{ nm}$
t_r	Rise Time			300 100	ns	Buffer Inverter $P_{IN} = 1.5 \mu\text{W}$ (peak) $V_{CC} = 5.0 \text{ V}$
t_f	Fall Time			300 100	ns	Buffer Buffer
BW	Bandwidth	100			kHz	$P_{IN} > 2.0 \mu\text{W}$, 50% duty cycle
PWD	Pulse Width Distortion		± 10		%	$1 \mu\text{W} < P_{IN} < 100 \mu\text{W}$, $f = 20 \text{ kHz}$ 50% duty cycle

General Note

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Performance



General Note

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