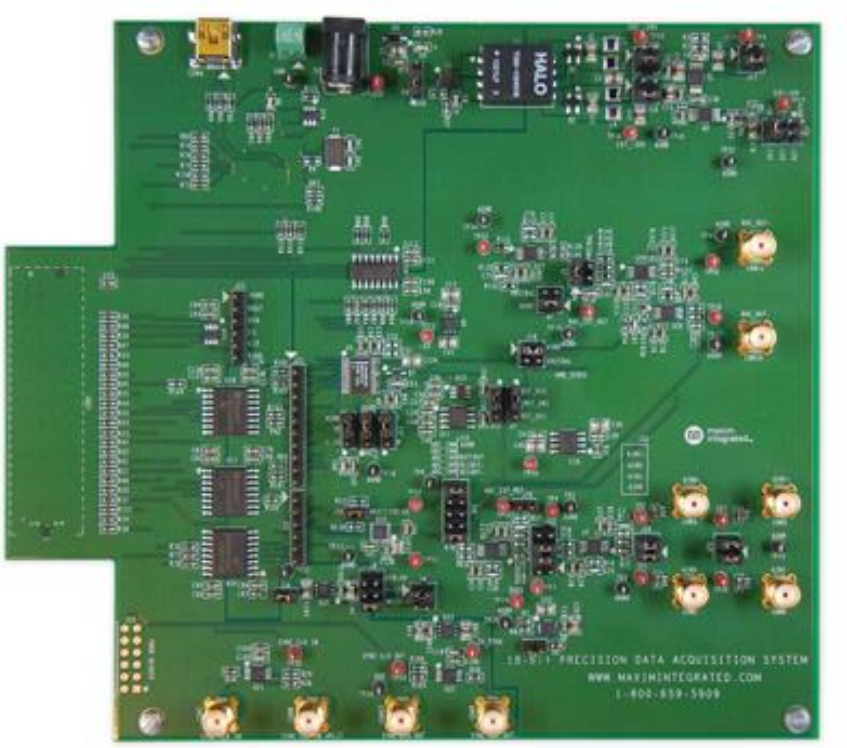
maxim integrated™

System Board 5944

MAXREFDES74#: 18-BIT PRECISION DATA ACQUISITION SYSTEM

MAXREFDES74# System Board



Introduction

The MAXREFDES74# reference design performs high-speed, 18-bit, precision data acquisition based on Maxim's leading-edge, high-accuracy, low-power data converters. The MAXREFDES74# design works as a building block for a high-speed, low-power, high-accuracy data acquisition and control system for industrial process control and automation, and high-speed protection systems for power distribution and automation. By changing the ADC and DAC to pin-compatible 16-bit devices such as the MAX11166 and the MAX5316, a 16-bit data acquisition system can also be tested.

The MAXREFDES74# reference design features:

- Power and data isolation
- Flexible, configurable inverting or noninverting input scheme
- Unipolar or bipolar input (ADC) and output (DAC)

MAX11156

- 18-bit resolution with no missing codes
- SNR: 94.4dB
- THD: -107dB at 1kHz
- Buffered internal or external voltage reference input
- Internal reference with -6ppm/°C (typ) temperature coefficient
- Single 5V supply
- True bipolar ±5V input range

MAX5318

- 18-bit resolution with no missing codes
- High accuracy: ±2 LSB INL (max)
- 3µs settling time
- User-programmable offset and gain calibration
- ±0.5ppm/°C (typ) offset and gain drift over temperature
- Force/sense output
- 50MHz SPI-compatible interface with 1.8V to 5.5V logic

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Detailed Description

The block diagram of the MAXREFDES74# board is shown in **Figure 1**.

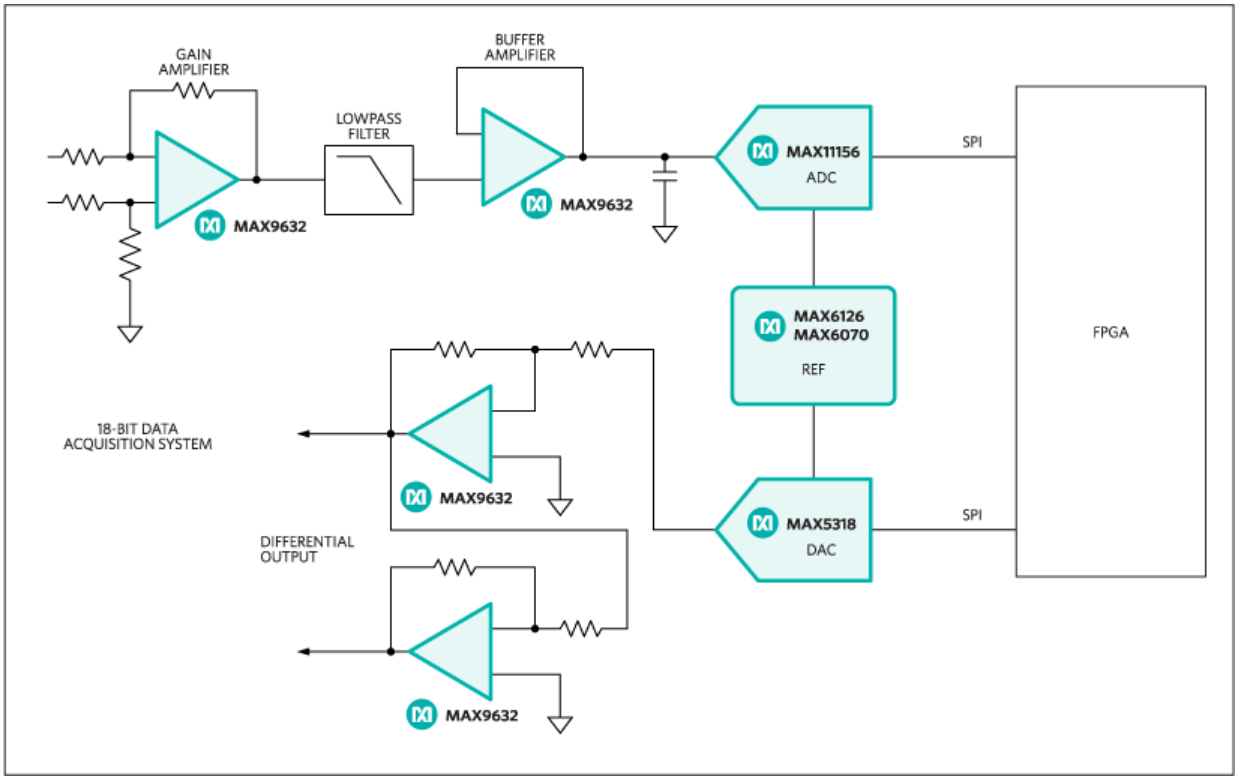

Figure 1. MAXREFDES74# block diagram.

The analog front-end consists of two user-selectable MAX9632 op amps, followed by the MAX11156. The op amps can be configured as inverting or noninverting amplifiers by jumper selectors. Both op amps work as anti-aliasing lowpass filters (LPF) and can be daisy-chained to create a second-order LPF.

The output of the MAX5318 DAC can also be configured as a positive or negative single-ended output, or as a true differential output through three MAX9632 op amps. The DAC output can also be shifted up to double the output level to 2 x V_{REF}.

The voltage reference (V_{REF}) for both the ADC and DAC comes from the selectable reference sources, which include the MAX6126, with 3ppm/°C, 0.02% initial accuracy V_{REF} in an 8-pin SO package, and the MAX6070, with 6ppm/°C, 0.04% initial accuracy V_{REF} in a 6-pin SOT23 package. The MAX11156 can use an internal V_{REF} (default operation) or one of the external references.

The shunt positions for major ADC configurations are shown in **Table 1** and **Figure 2**, and for the DAC output in **Table 2**, and a V_{REF} connection in **Table 3**.

Table 1. ADC Input Configuration

CONFIG #	ADC INPUT CONFIGURATION	INPUT CONNECTORS	SHUNT POSITIONS
1	Noninverting, single-ended, second-order LPF (default)	CON3: AIN0+ or (TP2 and TP8): AIN0+ and AGND	J28: 1-2 J29: 1-2 and 3-4 J32: 5-6 and 3-4 J10: 1-2 and 9-10
2	Noninverting, differential, second-order LPF	CON3 (TP2): AIN0+ CON2 (TP1): AIN0-	J28: Open J29: 1-2 J32: 5-6 and 3-4 J10: 1-2 and 9-10
3	Inverting, single-ended, second-order LPF	CON2: AIN0 or (TP1 and TP8): AIN0 and AGND	J28: 3-4 J29: 3-4 J32: 1-2 and 7-8 J10: 1-2 and 9-10
4	Inverting, differential, second-order LPF	CON2 (TP1): AIN0- CON3 (TP2): AIN0+	J28: Open J29: 3-4 J32: 1-2 and 7-8

			J10: 1-2 and 9-10
5	Noninverting, single-ended, first-order LPF	CON5: AIN1 or (TP7 and TP15): AIN1 and AGND	J29: 1-2 J32: 3-4 and 7-8 J10: 1-2 and 9-10
6	Differential, first-order LPF	CON5 (TP7): AIN1+ CON4 (TP10): AIN1-	J29: Open J32: 3-4 and 7-8 J10: 1-2 and 9-10
7	Inverting, single-ended, first-order LPF	CON4: AIN1 or (TP10 and TP15): AIN1 and AGND	J29: 3-4 J32: 1-2 and 7-8 J10: 1-2 and 9-10
8	DAC noninverting, single-ended	Use the on-board MAX5318 as input source*	J10: 3-4 and 9-10 J9: 1-2 J5: 1-2 J18: 1-2
9	DAC inverting, single-ended	Use the on-board MAX5318 as input source*	J10: 5-6 and 9-10 J9: 1-2 J5: 1-2 J18: 1-2
	DAC differential	Use the on-board MAX5318 as input source*	J10: 3-4 Jump wire J10: 5-10

*DAC output configuration must be compliant with the ADC input range.

Table 2. DAC Output Configuration

CONFIG #	DAC OUTPUT	SHUNT POSITIONS	OUTPUT CONNECTORS
10	Single ended, 0 to 3 x V_{REF}	J9: 1-2 J5: 1-2 J18: 1-2	CON11: DAC_OUT+ or (TP46 and TP41): DAC_OUT+ and AGND
11	Single ended, 0 to -3 x V_{REF}	J9: 1-2 J5: 1-2 J18: 1-2	CON10: DAC_OUT- or (TP18 and TP17): DAC_OUT- and AGND
12	Differential, - 3 x V_{REF} to 3 x V_{REF}	J9: 1-2 J5: 1-2 J18: 1-2	CON11 (TP46): DAC_OUT+ CON10 (TP18): DAC_OUT-
13	Single ended, -1.5 x V_{REF} to 1.5 x V_{REF} (default)	J9: 3-4 J5: 1-2 J18: 1-2	CON11: DAC_OUT+ or (TP46 and TP41): DAC_OUT+ and AGND

Note: Alternate connections are shown in parentheses.

Table 3. V_{REF} Connection

CONFIG #	V_{REF}	SHUNT POSITIONS FOR ADC	SHUNT POSITIONS FOR DAC
14	Internal	J13: open (default)	—
15	External U11 (MAX6126)	J13: 2-3	J7: 2-3 (default)
16	External U12 (MAX6070)	J13: 1-2	J7: 1-2

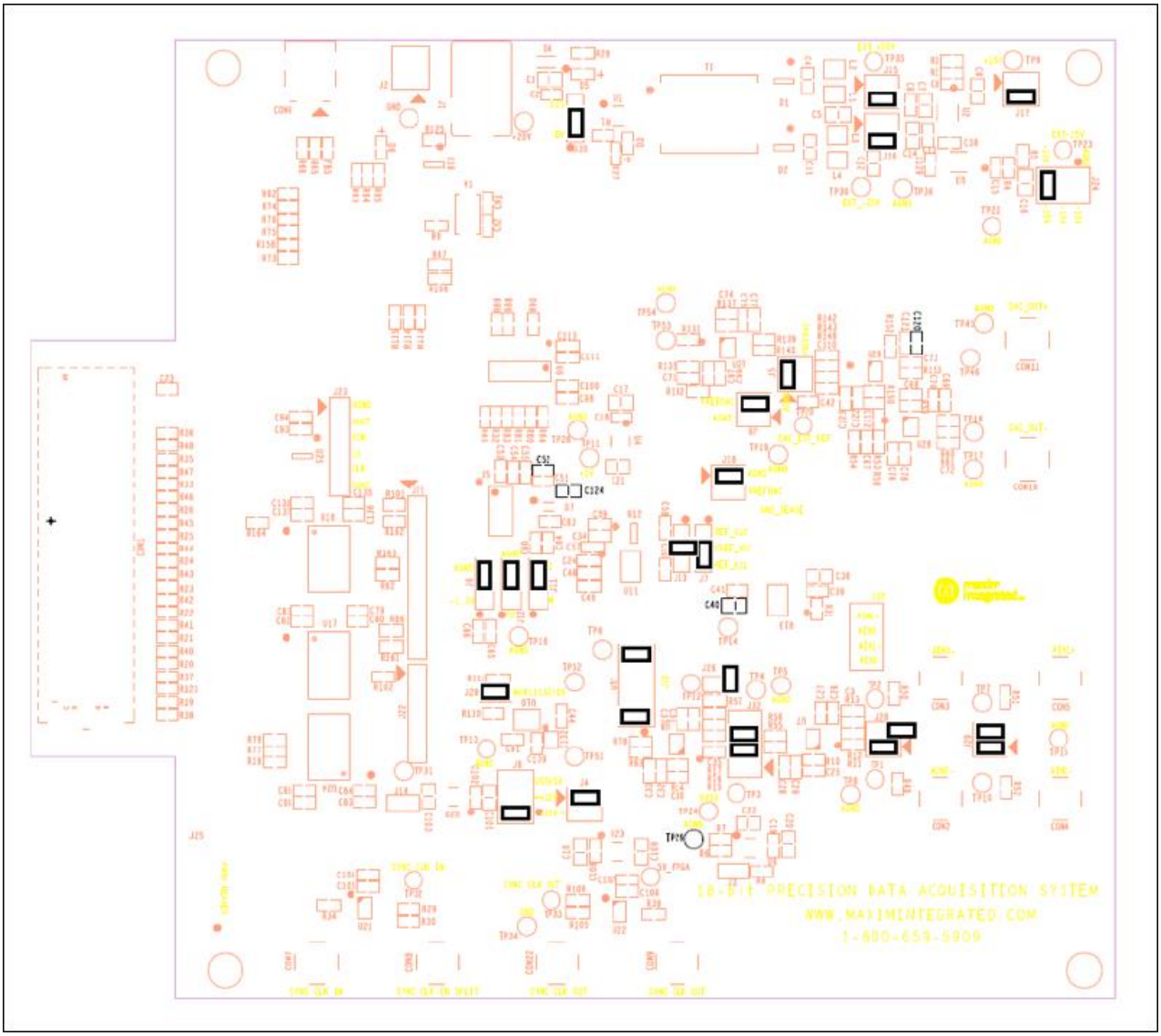

Figure 2. Default shunt positions.

Power Supply

The MAXREFDES74# board receives power from a single DC source of 15V to 20V, 300mA through a J1 power jack. The MAX13256, H-bridge driver and transformer create an additional negative rail for +20V and -20V. The power is then rectified and regulated down to a +15V and -15V supplies for the op amps, as well as into +5V $V_{DD}$and 3.3V V_{DDIO} for V_{REF}, ADC, and DAC. See the MAXREFDES74# schematic for details. Specific voltages may be connected to the board for each rail, see **Table 4** for corresponding shunt positions.

Table 4. Power Supply to the Board

POWER	INPUT CONNECTORS	SHUNT POSITIONS
Single +15V to +20V input from a wall adapter (default)	J1	J30: 1-2 Enable U1 J15: 3-4 J16: 3-4 J17: 3-4 J24: 5-6
An external ±20V	TP35 (+20V) TP30 (-20V) TP36 (Common 0V)	J30: 2-3 Disable U1 J15: 1-2 J16: 1-2 J17: 3-4 J24: 5-6
An external ±15V	TP9 (+15V) TP23 (-15V) TP22 (Common 0V)	J30: 2-3 Disable U1 J15: 1-2 J16: 1-2 J17: 1-2 J24: 3-4

Mezzanine Card Operation with ZedBoard

The MAXREFDES74# board is connected to the ZedBoard through a low-pin-count FMC CON1 connector. The ZedBoard should be connected to a PC through an Ethernet port, which allows the GUI to perform different operations with full control over mezzanine card functions.

Quick Start Guide

Required Equipment

- MAXREFDES74#, 18-bit precision data acquisition board, with +15V, 1A AC-DC wall adapter or +15V DC power supply
- ZedBoard (Part Number: AES-Z7EV-7Z020-G) with +12V AC-DC wall adapter and SD card
- PC with Windows® 7 or later operating system
- Ethernet cable
- High-performance signal generator (e.g., Audio Precision 2700 series)

Procedure

The MAXREFDES74# board is fully assembled and tested. Follow the steps below to verify board operation:

1. Download the latest version of the MAXREFDES74# Software GUI and MAXREFDES74# Zedboard firmware. Save the firmware and software to a temporary folder and uncompress the zip files. Store the firmware file to an SD card.
2. Solder the 2-pin header on J18-3V3 of the ZedBoard. Place a shunt on the J18-3V3 header to select 3.3V I/O operation to be compatible with the MAXREFDES74# board.
3. Connect the Ethernet cable from the PC to the ZedBoard and configure the Internet Protocol Version 4 (TCP/IPv4) properties in the local area connection to IP address 192.168.1.2 and subnet mask to 255.255.255.0.
4. Insert the SD card with the boot file into the card slot (J12) of ZedBoard, located underneath the PCB.
5. Verify the ZedBoard boot mode MIO2-6 jumpers are set to SD card mode as described in the Hardware User Guide for ZedBoard.

MIO6	GND
MIO5	3V3
MIO4	3V3
MIO3	GND
MIO2	GND

6. Turn on the power switch (SW8) of the ZedBoard to the ON position. The green power-good LED (LD13) should light and the current revision of the MAXREFDES74 firmware is displayed on the OLED (DISP1).
7. Turn off the power to the ZedBoard.
8. Connect the MAXREFDES74# board to the ZedBoard through the FMC connector.
9. Apply power to the MAXREFDES74# board from a +15V wall adapter.
10. Turn on the power to ZedBoard.
11. Open the MAXREFDES74# GUI. The GUI automatically detects the network connection to the ZedBoard and displays a confirmation message. If no network connection is found, the GUI will go to demo mode.
12. After the connection is established, the GUI indicates the board condition in the status bar on the bottom side of the GUI.

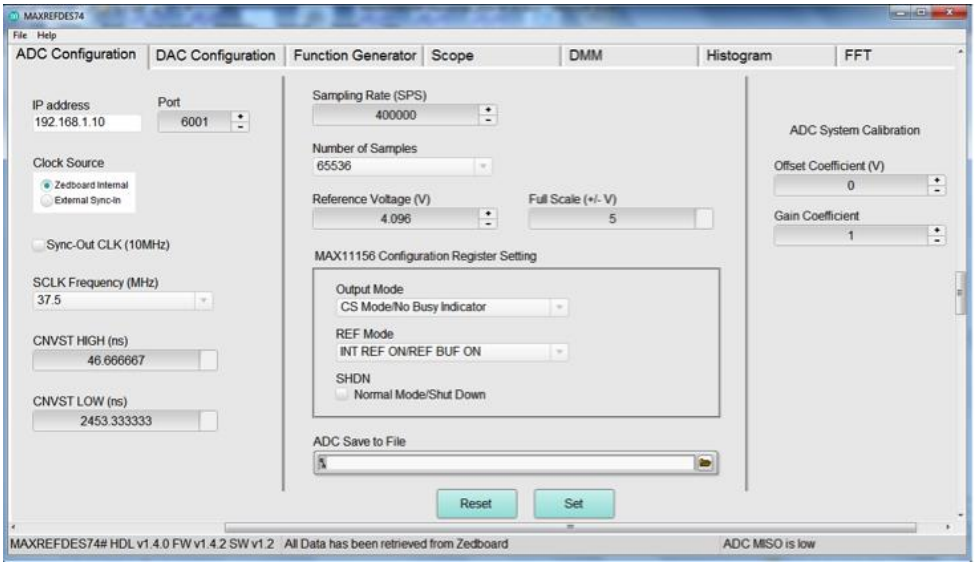

Figure 3. MAXREFDES74# GUI.

13. Verify the Clock Source, Sampling Rate, Number of Samples, and Configuration of the MAX11156 ADC, and click the Set button.
14. Go to the DMM tab, select mV from the Display Units pulldown menu and click the Capture button. The reading of the MAX11156 ADC should display a small number in mV. That is the reading of the 0V (AGND) input. Make sure that all inputs are grounded by shunts on J28 and J29; see the ADC Input Configuration table, Table 1, and the MAXREFDES74# schematic.
15. Go to the Scope, Histogram, and FFT tabs to verify functionality and performance of the 0V reading. Set the Sampling rate and select the Number of Samples, the Display Units, and the Average from the corresponding pulldown menu and perform a read operation by clicking the Capture button. The corresponding print screens are shown in **Figure 4**, **Figure 5**, **Figure 6**, and **Figure 7**.

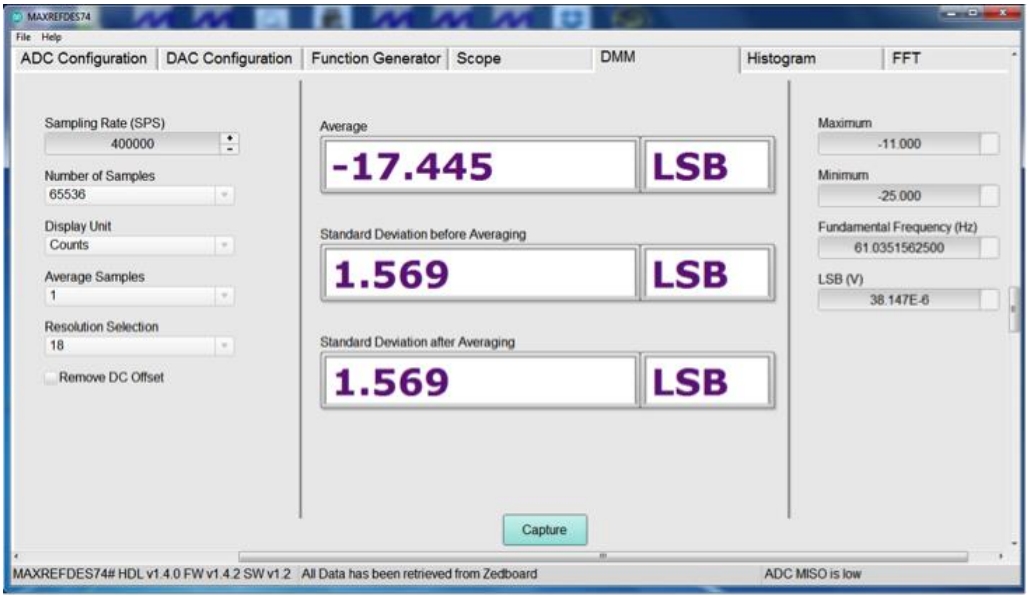

Figure 4. DMM tab.

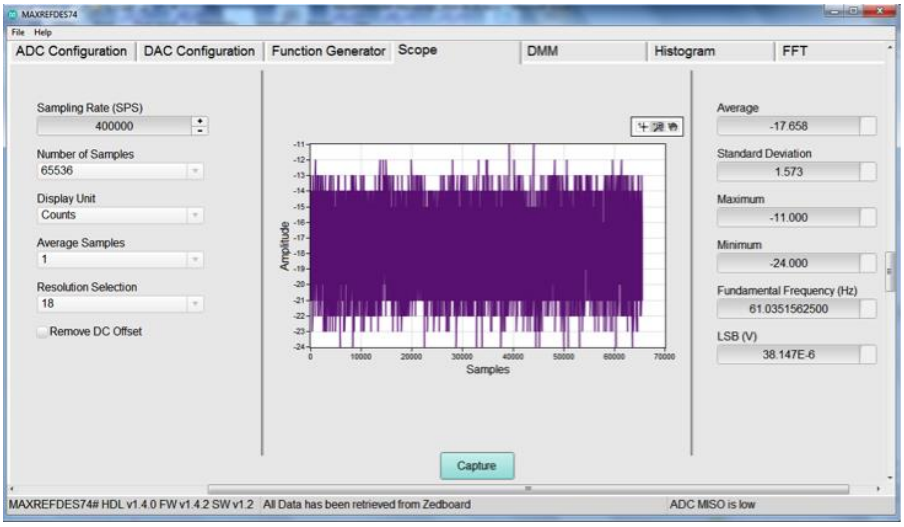

Figure 5. Scope tab.

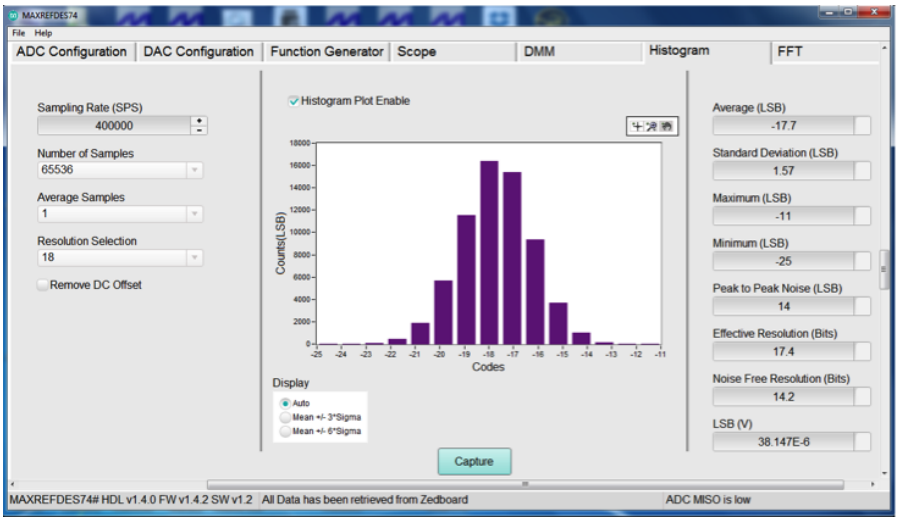

Figure 6. Histogram tab.

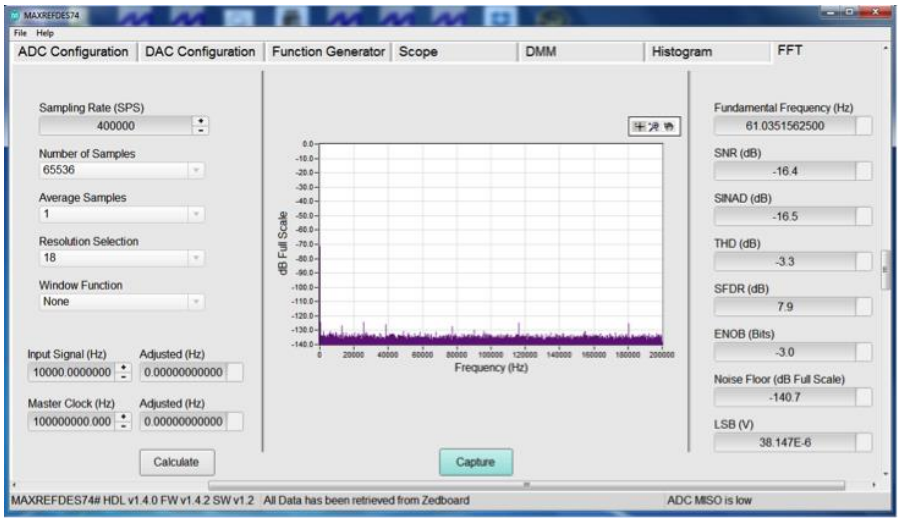

Figure 7. FFT tab.

16. Place a J26 shunt and repeat the performance of the $V_{REF}/2$ reading.
17. Apply a 10kHz sine wave from an external source, e.g. Audio Precision 2700, to CON3 (AIN0+). Synchronize the external source with the MAXREFDES74# ADC by connecting CON9 (SYNC_CLK_OUT) to the REF IN input for coherent sampling. In the ADC Configuration tab, check the Sync-Out CLK (10MHz) selection box to enable the 10MHz clock output from the ZedBoard and click the Set button. Then go to the FFT tab, select Sampling Rate, Number of Samples, put desired signal frequency in the Input Signal (Hz) pulldown menu and then click the Calculate button. The GUI will calculate the coherent input signal frequency based on the coherent sampling equation. The user will then enter the adjusted signal frequency, shown in the Adjusted (Hz) box, into the external function generator. Then click the Capture button in the FFT tab.

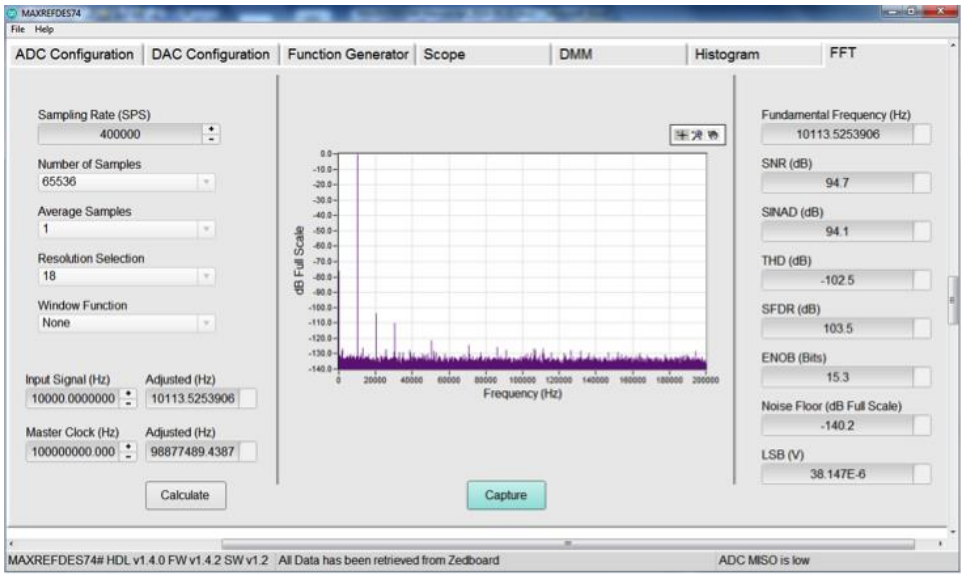

Figure 8. Coherent sampling of a 10kHz sine wave.

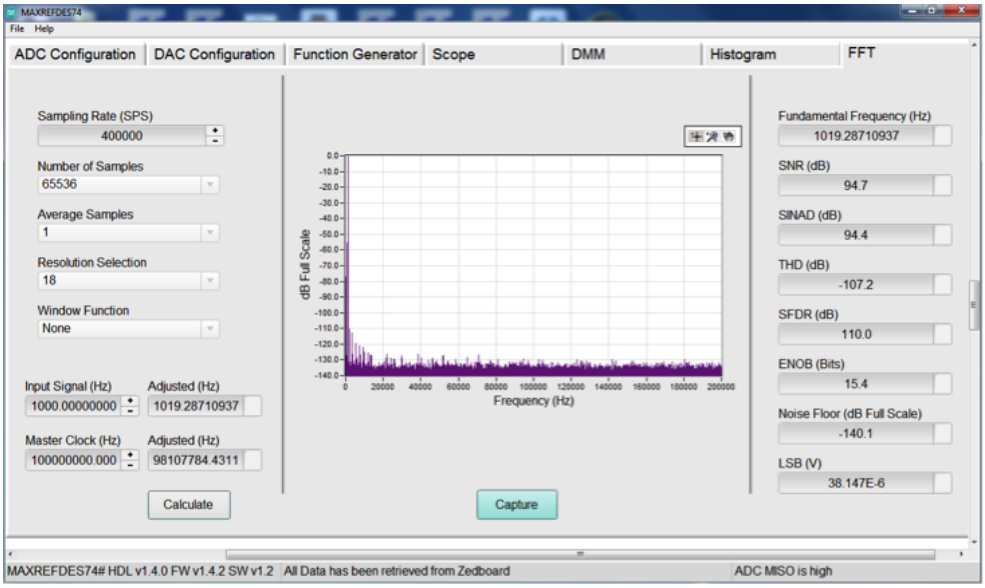

Figure 9. Coherent sampling of a 1kHz sine wave.

Also see:
Bipolar Work Around for the MAXREFDES74 ›

All Design Files

Download All Design Files

Hardware Files:
Schematic
Bill of Materials (BOM)
PCB Layout
PCB Gerber

Software Files:
Software GUI

Firmware Files:
ZedBoard Firmware

Part Number
MAXREFDES74# Status Active Carrier Type Box