FLINK3V8BT-85 Evaluation Kit

User's Guide

Literature Number: SNLU032A
February 2011–Revised August 2016

FLINK3V8BT-85 Evaluation Kit

1 Introduction

The FLINK3V8BT-85 evaluation kit contains a transmitter (Tx) board, a receiver (Rx) board, and an interfacing cable. This kit will demonstrate the DS90C385A/DS90CF386 chipsets interfacing from test equipment or a graphics controller using low voltage differential signaling (LVDS) to a receiver board. The transmitter board accepts LVTTL/LVCMOS RGB signals from the graphics controller along with the clock signal. The LVDS transmitter converts the LVTTL/LVCMOS parallel lines into four serialized LVDS data pairs plus a LVDS clock. The serial data streams toggle at 3.5 times the clock rate. The receiver board accepts the LVDS serialized data streams plus clock and converts the data back into parallel LVTTL/LVCMOS RGB signals and clock for the panel timing controller. The user must provide the proper RGB inputs and clock to the transmitter and also provide a proper interface from the receiver output to the panel timing controller or test equipment. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used. A power-down feature is also provided that reduces current draw when the link is not required.

1.1 Contents of the Evaluation Kit

- One transmitter board with the DS90C385A - 28 bit transmitter
- One receiver board with the DS90CF386 - 28-bit receiver
- One 20-pin IDC flat ribbon cable

1.2 FPD-Link I Typical Applications

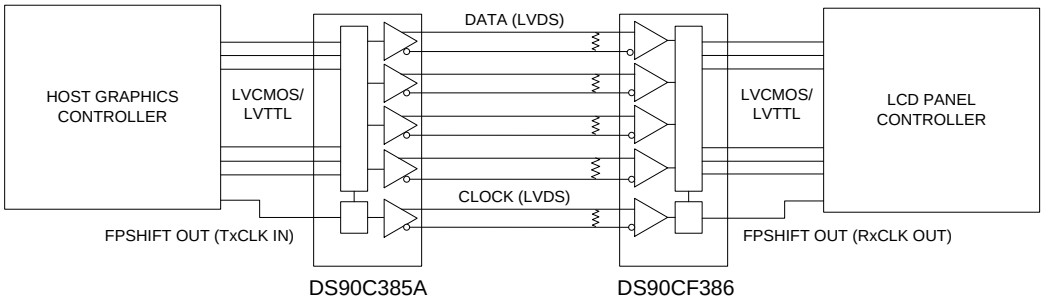


Figure 1. Typical FPD-Link I GPU and LCD Application

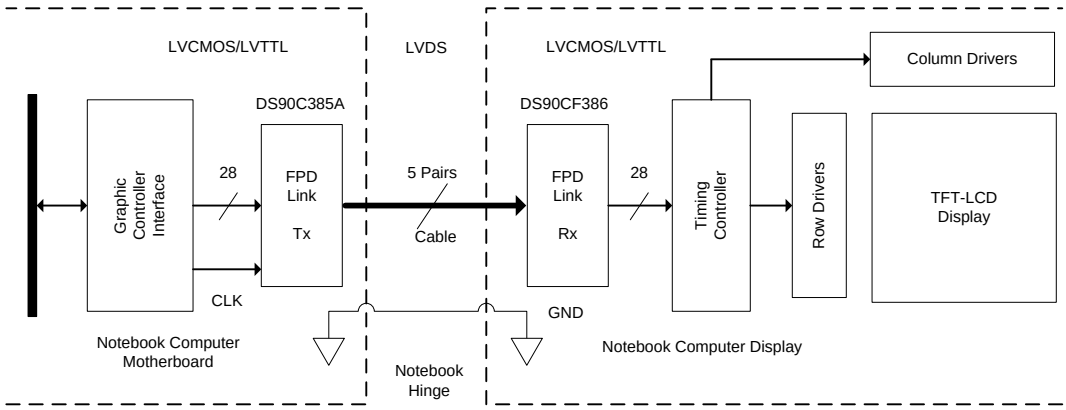


Figure 2. Typical FPD-Link I Display Application (24-Bit Color)

Figure 1 and Figure 2 show the use of the chipset (Tx/Rx) in a host-to-LCD panel interface.

Chipsets support up to 18-bit or 24-bit AM-TFT LCD panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), and single/dual pixel SXGA (1280X1024) resolutions.

Because of the non-periodic nature of STN-DD SHFCLK, the chipset may not work with all D-STN panels. The PLL CLK input of the transmitter requires a free running periodic SHFCLK. Most graphics controller can provide a separate pin with a free running clock. In this case the STN-DD SHFCLK can be sent as data while the free running clock can be used as SHFCLK for the PLL ref CLK. For example, C&T's 65550's WEC (pin 102) can be programmed to provide a free running clock using the BMP (Bios Modification Program). Refer to STN Application using AN-1056 for more information on STN support.

Refer to the proper datasheet information on chipsets (Tx/Rx) provided on each board for more detailed information.

2 How to Set Up the Evaluation Kit (Overview)

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from a 60-pin IDC connector. The TxOUT/RxIN interface uses a 20-pin IDC connector through a IDC ribbon cable. Follow these steps to set up the evaluation kit for bench testing and performance measurements:

1. Connect one end of the 20-pin IDC cable to the transmitter board and the other end to the receiver board. Longer lengths can be used. **Note:** Previous HSL Tx/Rx 8-bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.
2. Jumpers have been configured at the factory, they should not require any changes for operation of the chipset. See text on Jumper settings for more details.
3. From the Graphics card, connect a flat (ribbon) cable to the transmitter board and connect another flat cable from the receiver board to the panel (Note: Refer to AN-1127 for suggested mapping schemes). Note that pin 1 on the connector should be connected to pin 1 of the cable. A scramble cable may be required.
4. Power for the Tx and Rx boards must be supplied externally through TP1 (V_{CC}). Grounds for both boards are connected through TP2 (GND) (see Section 2.1).

2.1 Power Connection

The transmitter and receiver boards must be powered by supplying power externally through TP1 (V_{CC}) and TP2 (GND) on EACH board. The maximum voltage that should ever be applied to the FPD-link transmitter (385A) or receiver (386) V_{CC} terminal is +4 V maximum.

3 FLINK3V8BT-85 Transmitter Board

J1 (60 position) accepts 28-bit LVTTL/LVCMOS data along with the clock.

The FPD-Link Transmitter board is powered externally. For the transmitter to be operational, the $\overline{\text{PWR DWN}}$ pin must be set HIGH with a jumper. Rising or falling edge reference clock is selected by JP1 tied to V_{CC} (rising) or GND (falling).

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the Receiver board.

Note: Previous HSL Tx/Rx 8-bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

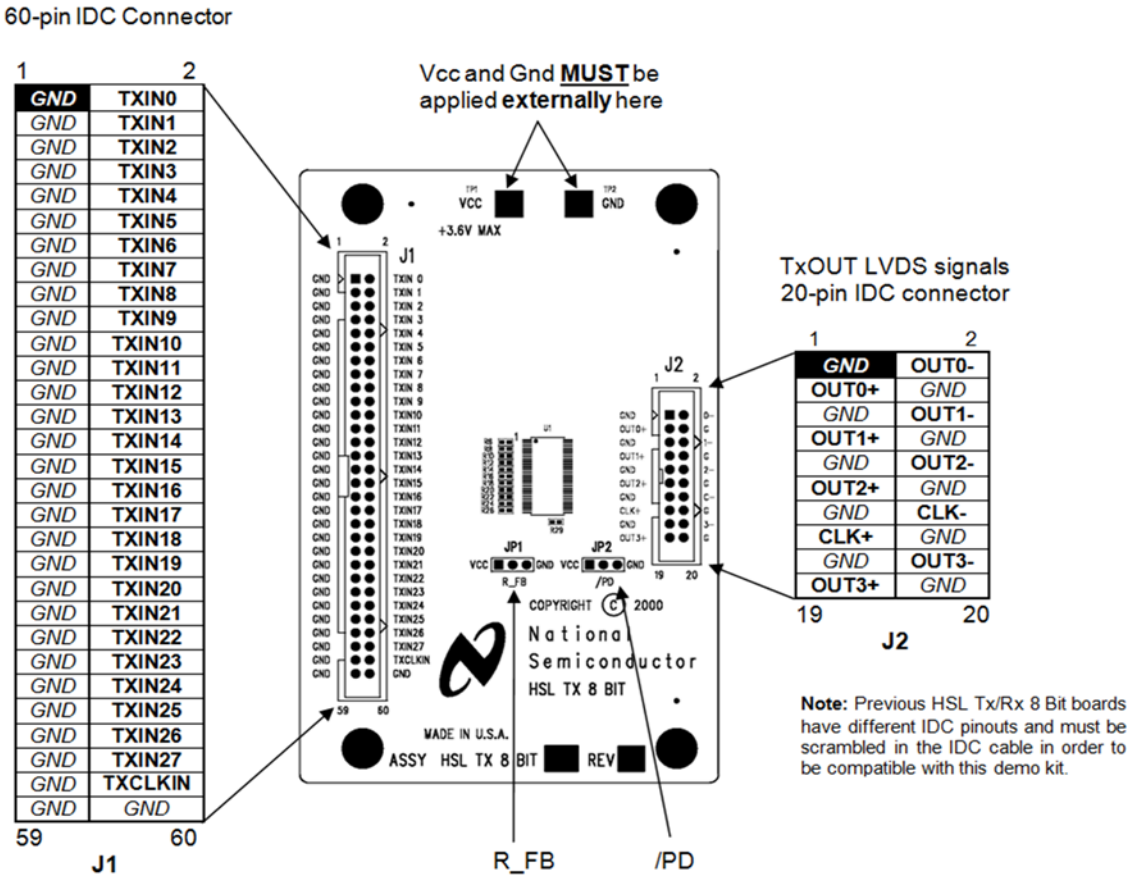
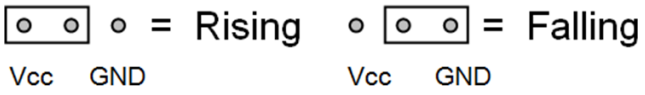
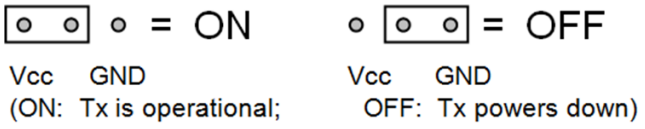


Figure 3. FLINK3V8BT-85 Transmitter Board

3.1 Selectable Jumper Settings for the Tx Board

JUMPER	PURPOSE	SETTINGS
R_FB (JP1)[1]	**R**ising or **F**alling data Strobe	
/PD (JP2)[2]	**P**ower **D**own	

(1) Default setting is JP1 set LOW (to GND), falling edge strobe.
(2) Default setting is JP2 set HIGH (to V_{CC}), operational mode.

3.2 Tx LVDS Mapping by IDC Connector

Figure 4 through Figure 6 show how the Tx inputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC (J2) connector pinout is also shown.

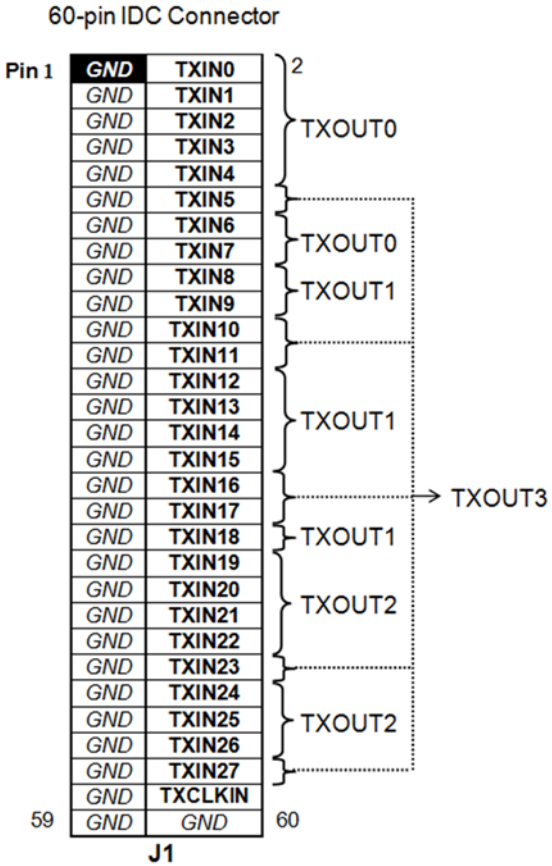


Figure 4. 60-Pin IDC Connector (Transmitter Board)

TxOUT LVDS signals
20-pin IDC connector

Pin 1	**GND**	**OUT0-**	2
	OUT0+	*GND*	
	GND	**OUT1-**	
	OUT1+	*GND*	
	GND	**OUT2-**	
	OUT2+	*GND*	
	GND	**CLK-**	
	CLK+	*GND*	
	GND	**OUT3-**	
19	**OUT3+**	*GND*	20

J2

Figure 5. TxOUT LVDS Signals 20-pin IDC connector

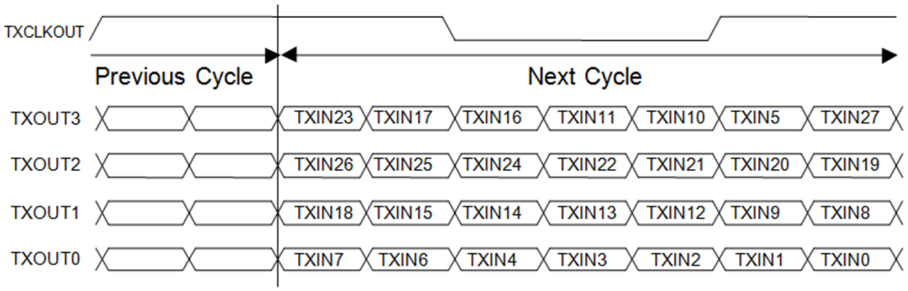


Figure 6. Parallel LVTTL/LVCMOS Data Inputs Mapped to LVDS Outputs

3.3 Tx Board Optional: 50-Ω Termination for TxIN

On the Tx demo board, the 29 inputs have an option for 50-Ω terminations. There are 0402 pads for this purpose. One side is connected to the signal line, and the other side is tied to ground. These pads are unpopulated from the factory but are provided if the user needs to install a 50-Ω termination. R1 to R28 are associated with the Tx data input lines. R29 is associated with CLKIN. Some test equipment may require a 50-Ω load. Mapping of transmitter inputs for the optional termination resistors is shown in Table 1 and Figure 7:

Table 1. Tx Pin and Optional Termination Resistor Mapping

Tx PIN NAMES	Tx PIN NUMBER	TERMINATION RESISTOR
TxIN0	51	R1
TxIN1	52	R2
TxIN2	54	R3
TxIN3	55	R4
TxIN4	56	R5
TxIN5	2	R6
TxIN6	3	R7
TxIN7	4	R8
TxIN8	6	R9
TxIN9	7	R10
TxIN10	8	R11
TxIN11	10	R12
TxIN12	11	R13
TxIN13	12	R14
TxIN14	14	R15
TxIN15	15	R16
TxIN16	16	R17
TxIN17	18	R18
TxIN18	19	R19
TxIN19	20	R20
TxIN20	22	R21
TxIN21	23	R22
TxIN22	24	R23
TxIN23	25	R24
TxIN24	27	R25
TxIN25	28	R26
TxIN26	30	R27
TxIN27	50	R28
TxCLKIN	31	R29

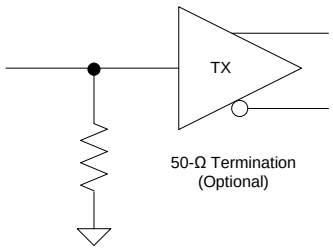


Figure 7. Schematic of Optional Parallel Input 50-Ω Termination to GND

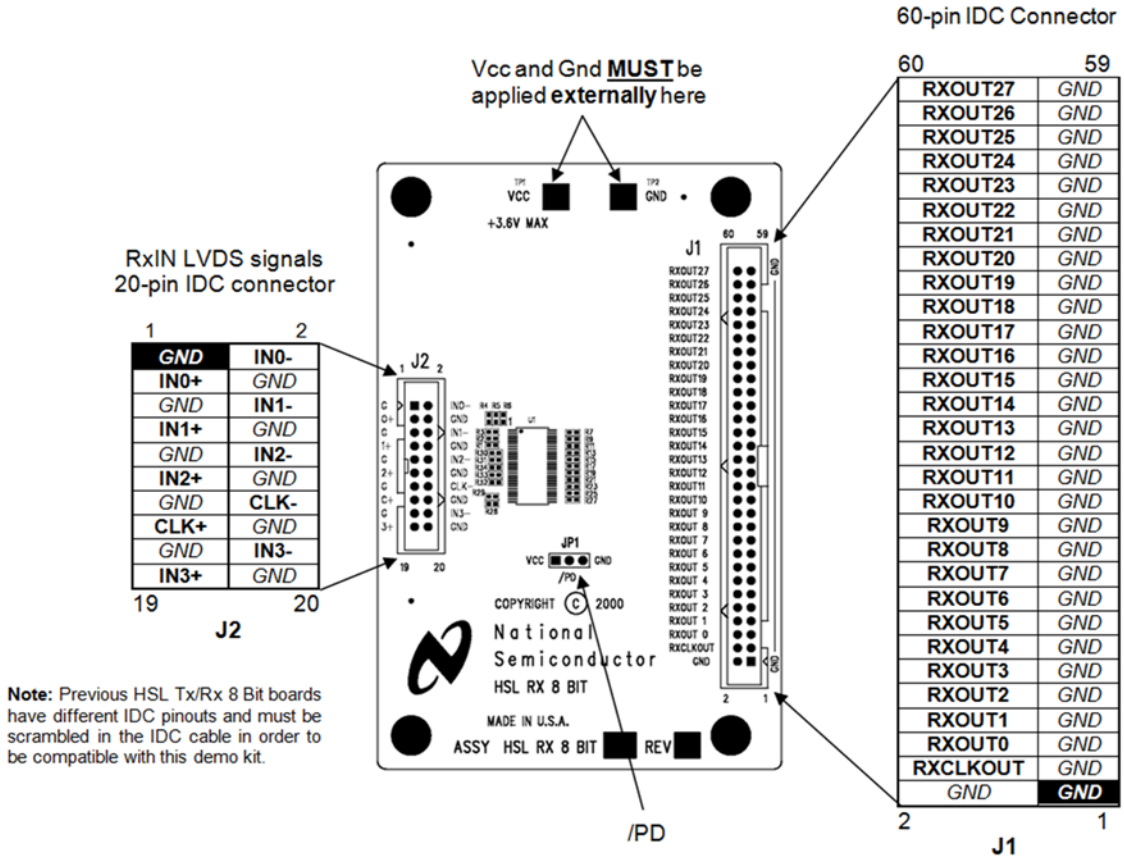
4 FLINK3V8BT-85 Receiver Board

J1 (60 position) provides access to the 28 bit LVTTL/LVCMOS and clock outputs.

The FPD-Link receiver board is powered from the pads shown below. For the receiver to be operational, the $\overline{\text{PWR DOWN}}$ pin must be set HIGH with the jumper.

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the receiver board.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.



1	2
GND	IN0-
IN0+	GND
GND	IN1-
IN1+	GND
GND	IN2-
IN2+	GND
GND	CLK-
CLK+	GND
GND	IN3-
IN3+	GND

19 20

60	59
RXOUT27	GND
RXOUT26	GND
RXOUT25	GND
RXOUT24	GND
RXOUT23	GND
RXOUT22	GND
RXOUT21	GND
RXOUT20	GND
RXOUT19	GND
RXOUT18	GND
RXOUT17	GND
RXOUT16	GND
RXOUT15	GND
RXOUT14	GND
RXOUT13	GND
RXOUT12	GND
RXOUT11	GND
RXOUT10	GND
RXOUT9	GND
RXOUT8	GND
RXOUT7	GND
RXOUT6	GND
RXOUT5	GND
RXOUT4	GND
RXOUT3	GND
RXOUT2	GND
RXOUT1	GND
RXOUT0	GND
RXCLKOUT	GND
GND	GND

2 1

Figure 8. FLINK3V8BT-85 Rx Board

4.1 Selectable Jumper Settings for the Rx Board

JUMPER	PURPOSE	SETTINGS
/PD (JP2)[1]	**P**ower **D**own	▭ ○ = ON (Vcc GND; (ON: Rx is operational;) ○ ▭ = OFF (Vcc GND; OFF: Rx powers down)

(1) Default setting is JP2 set HIGH (to V_{CC}), operational mode.

4.2 LVDS Mapping by IDC Connection

Figure 9 through Figure 11 show how the Rx outputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC connector (J2) pinout is also shown.

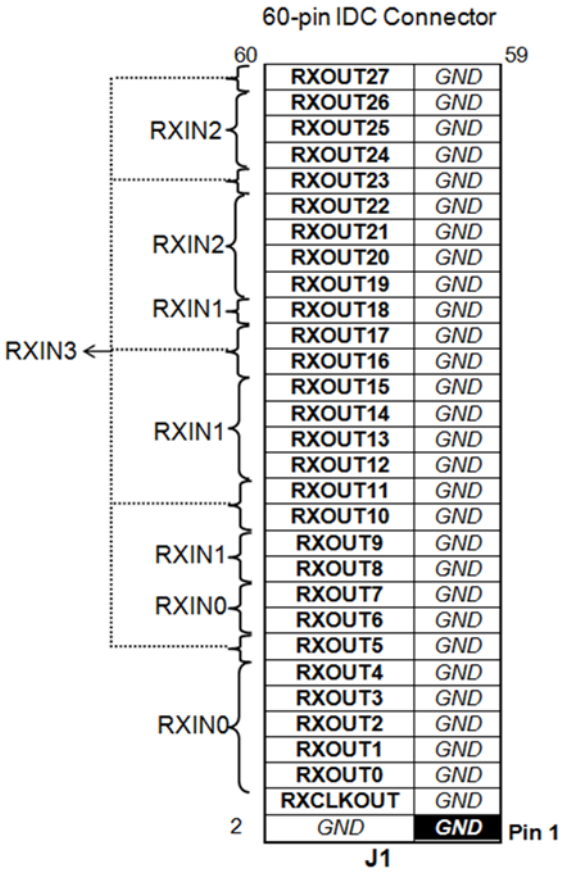


Figure 9. 60-Pin IDC Connector (Receiver Board)

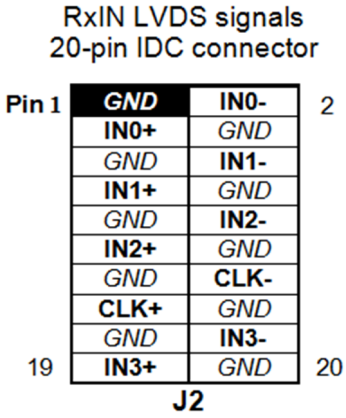


Figure 10. RxIN LVDS Signals 20-Pin IDC connector

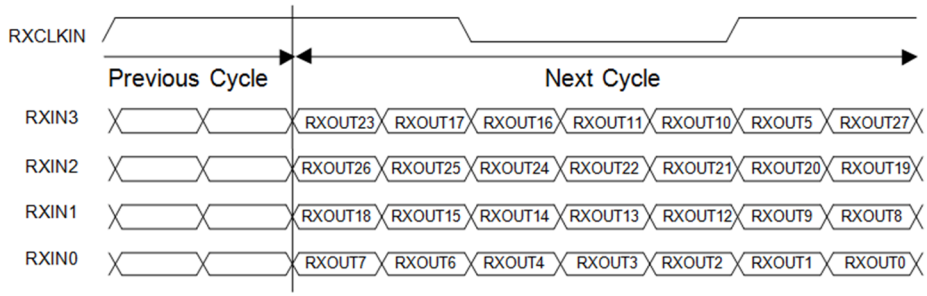


Figure 11. LVDS Data Inputs Mapped to LVTTL/LVCMOS Outputs

4.3 Rx Optional: Series Termination for RxOUT

On the Rx demo board, there are 29 outputs that have an 0402 pad in series (which are shorted out). These pads are unpopulated from the factory but are provided if the user needs to install a 450-Ω series resistors. This is required if directly connecting to 50-Ω inputs on a scope. To use this option, the user must cut the signal line between the pads before installing the 450-Ω series resistors. R1 to R28 are associated with the DATA output lines. R29 is associated with CLKOUT. The total load presented to the receiver output is 500 Ω (450 Ω + 50 Ω). The waveform on the scope is 1/10 of the signal due to the resulting voltage divider (50 / (450 + 50)). Mapping of receiver outputs for the optional series termination resistors is shown in Table 2 and Figure 12:

Table 2. Rx Pin and Optional Series Resistor Mapping

Rx PIN NAMES	Rx PIN NUMBER	SERIES TERMINATION RESISTOR
RxOUT0	27	R28
RxOUT1	29	R27
RxOUT2	30	R26
RxOUT3	32	R25
RxOUT4	33	R24
RxOUT5	34	R23
RxOUT6	35	R22
RxOUT7	37	R21
RxOUT8	38	R20
RxOUT9	39	R19
RxOUT10	41	R18
RxOUT11	42	R17
RxOUT12	43	R16
RxOUT13	45	R15
RxOUT14	46	R14
RxOUT15	47	R13
RxOUT16	49	R12
RxOUT17	50	R11
RxOUT18	51	R10
RxOUT19	53	R9
RxOUT20	54	R8
RxOUT21	55	R7
RxOUT22	1	R6
RxOUT23	2	R5
RxOUT24	3	R4
RxOUT25	5	R3
RxOUT26	6	R2
RxOUT27	7	R1
RxCLKOUT	26	R29

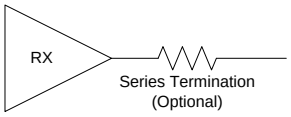


Figure 12. Schematic of Optional Parallel Output 450-Ω Series Termination

5 Typical Connection/Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Tx inputs:

1. Graphics card or GUI controller with digital RGB (LVTTL) output.
2. TEK HFS9009 - This pattern generator along with 9DG2 cards may be used to generate input signals and also the clock signal.
3. TEK DG2020 - This generator may also be used to generate data and clock signals.
4. TEK MB100 BERT - This bit error rate tester may be used for both signal source and receiver.
5. Any other signal / pattern generator that generates the correct input levels as specified in the data sheet.

The following is a list of typical test equipment that may be used to monitor the output signals from the Rx outputs:

1. LCD Display Panel which supports digital RGB (LVTTL) inputs.
2. TEK MB100 BERT - receiver.
3. Any SCOPE with 50-Ω inputs or high impedance probes.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes. Figure 13 shows a typical test setup using a graphics card and LCD panel:

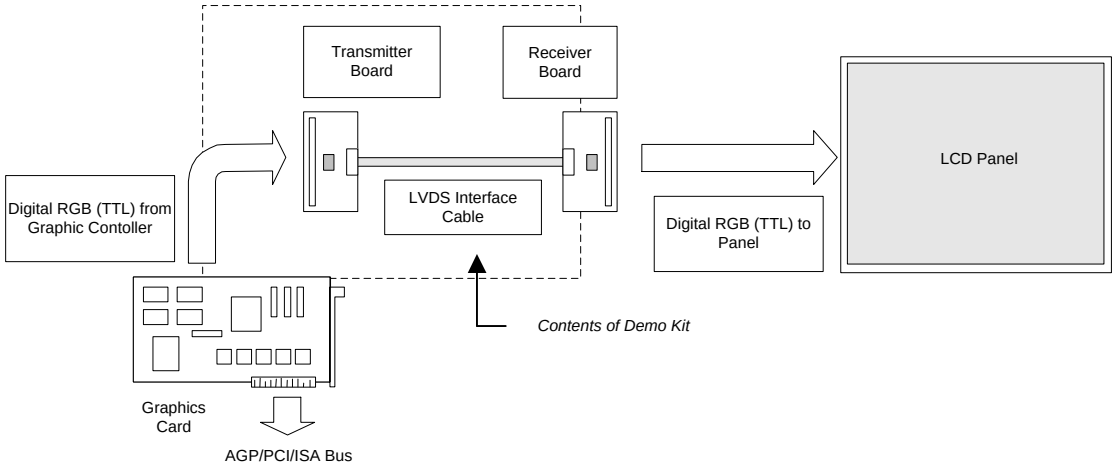


Figure 13. Typical FPD-Link I Setup/PC Panel Application

Figure 14 shows a typical test set up using a generator and scope:

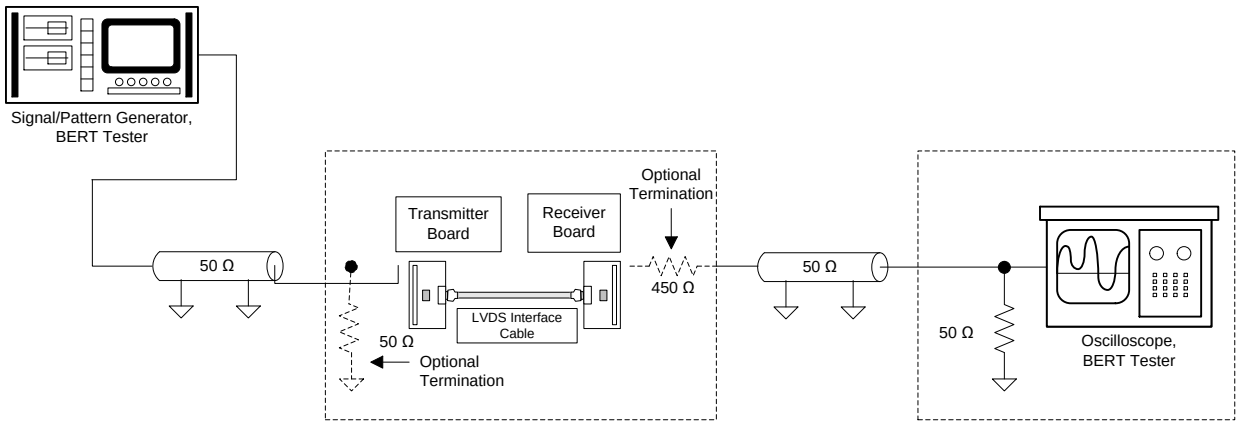


Figure 14. Typical Connection/Test Equipment Setup

6 Typical Waveforms

6.1 LVDS Serial Stream

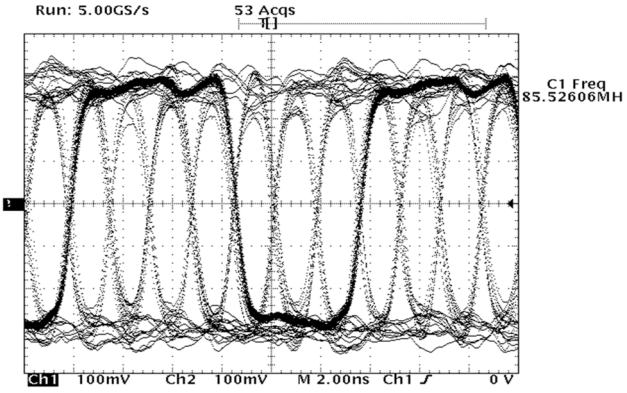


Figure 15. LVDS Serial Data and Clock

Figure 15 shows both the LVDS data channel with PRBS data and also the LVDS clock overlaid. Note that the clock pattern is four bit times HIGH and three bit times LOW. The differential signal should be typically ±300 mV. These waveforms were acquired using the TEK P6248 probes. Clock rate is 85 MHz.

6.2 RxOUT Parallel Stream

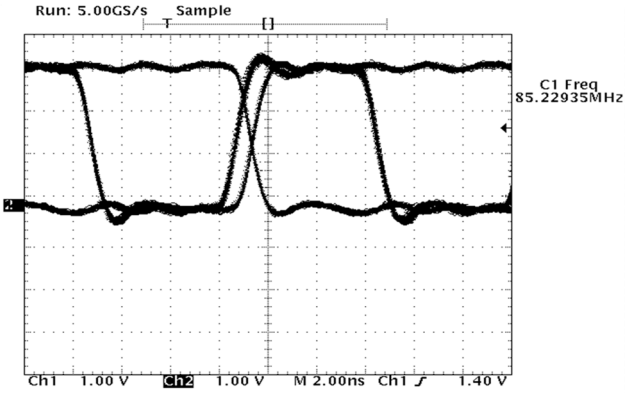


Figure 16. LVCMOS Parallel Data and Clock

Figure 16 shows both the recovered PRBS data and also the regenerated clock overlaid. Note that the clock transitions slightly before the data transition and strobes the data on the falling edge of the clock. The data and clock signals are low drive 3.3-V LVCMOS outputs. The plot above is at 85 MHz.

7 Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems.

Quick checks:

1. Check that power and ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3 V) and also current draw with both Tx and Rx boards (should be about 200 mA with clock and one data bit at 66 MHz).
3. Verify input clock and input data signals meet requirements (V_{IL}, V_{IH}, t_{set}, t_{hold}). Also verify that data is strobed on the selected rising/falling (R_FB pin) edge of the clock.
4. Check that the jumpers are set correctly.
5. Check that the cable is properly connected.

Table 3. FLINK3V8BT-85 Troubleshooting Checklist

PROBLEM	SOLUTION
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin.Make sure data is valid at the input.
No output data and clock.	Make sure power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the $\overline{\text{PWR DOWN}}$ pins of both boards and make sure that the devices are enabled ($\overline{PD} = V_{CC}$) for operation.
The devices are pulling more than 1 A of current.	Check for shorts in the cables connecting the Tx and Rx boards.
After powering up the demo boards, the power supply reads less than 3 V when it is set to 3.3 V.	Use a larger power supply that provides enough current for the demo boards — a 500-mA power supply is recommended.

8 Bill of Materials

Table 4. FLINK3V8BT-85 Tx Board

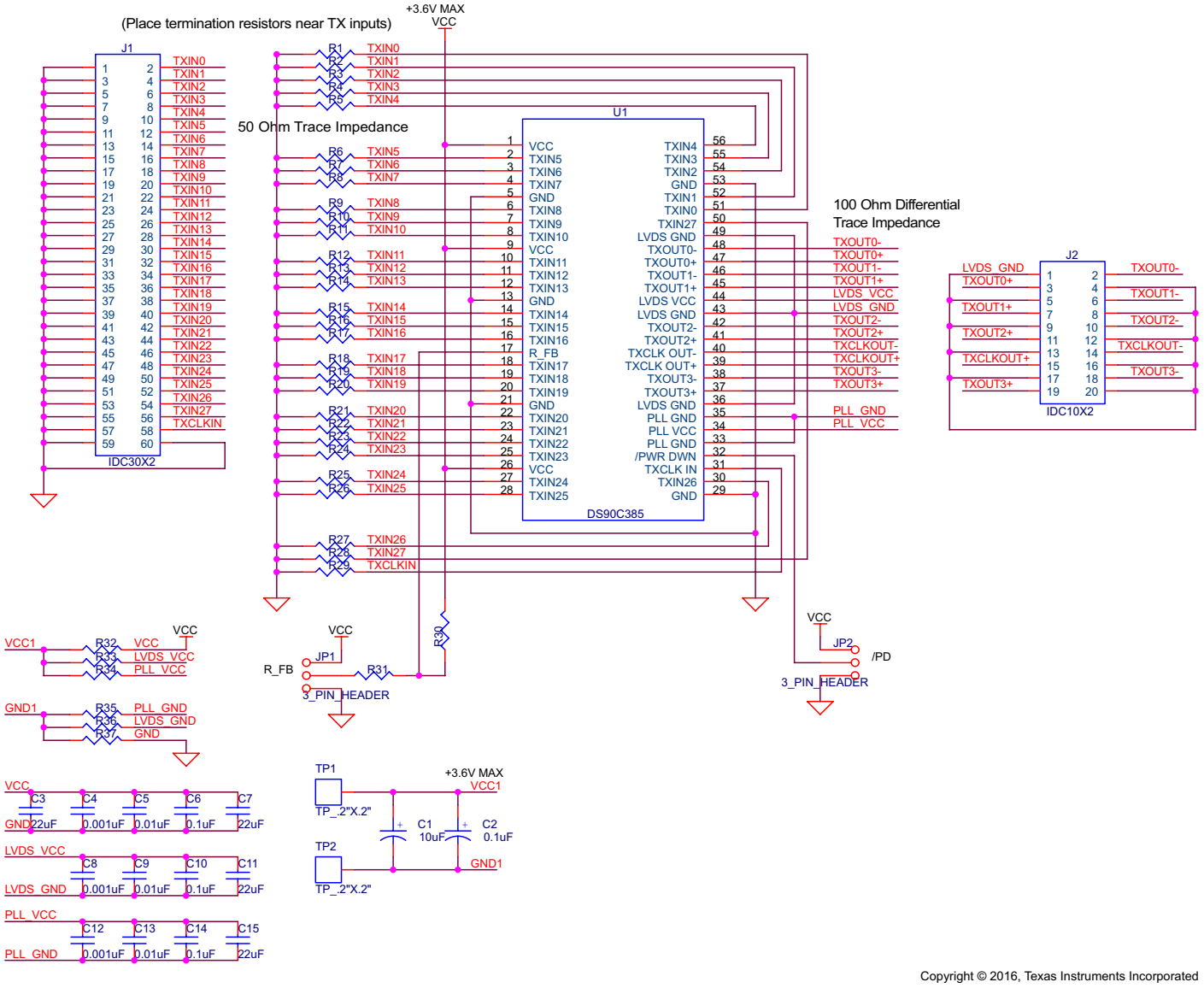
ITEM	QTY	REFERENCE	PART	PKG SIZE
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	2	JP2,JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12, R13,R14,R15,R16,R17,R18,R19,R20,R21, R22,R23,R24,R25,R26,R27,R28,R29	Optional (see Section 3.3)	402
10	8	R30,R31,R32,R33,R34,R35,R36,R37	0 Ω	402
11	2	TP1,TP2	N/A	TP_0.2 inches × 0.2 inches
12	1	U1	DS90C385AMT/NOPB	56-pin TSSOP

Table 5. FLINK3V8BT-85 Rx Board

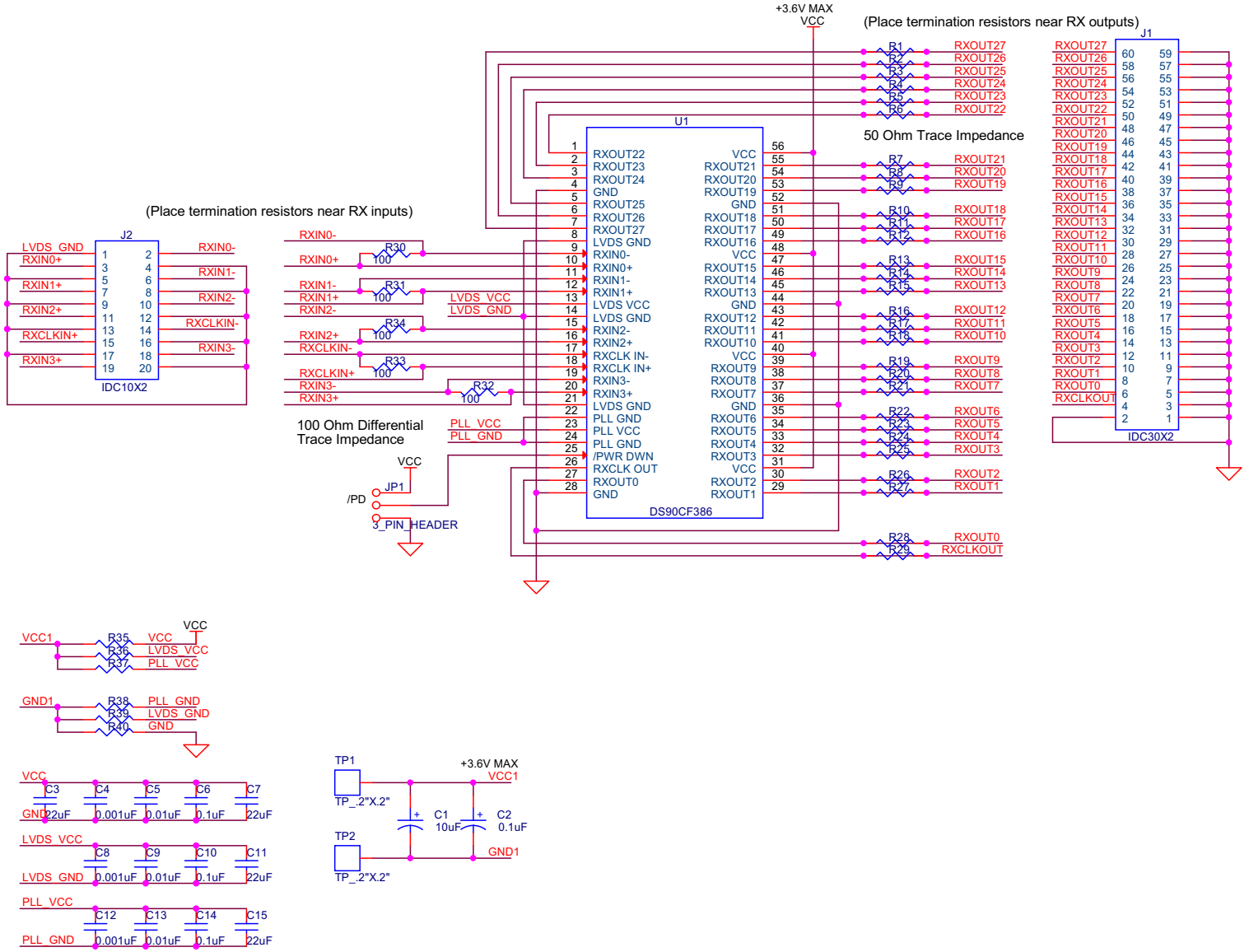
ITEM	QTY	REFERENCE	PART	PKG SIZE
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	1	JP1	3_PIN_HEADER	0.1-inch spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12, R13,R14,R15,R16,R17,R18,R19,R20,R21, R22,R23,R24,R25,R26,R27,R28,R29	Optional (see Section 4.3)	402
10	6	R35,R36,R37,R38,R39,R40	0 Ω	402
11	5	R30,R31,R32,R33,R34	100 Ω	402
12	2	TP1,TP2	N/A	TP_0.2 inch × 0.2 inch
13	1	U1	DS90CF386MTD/NOPB	56-pin TSSOP

9 Schematics

9.1 FLINK3V8BT-85 Tx Board



9.2 FLINK3V8BT-85 Rx Board



10 References

For the latest data sheets, see:

- *+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display Link-87.5 MHz*
- *DS90CF3x6 3.3-V LVDS Receiver 24-Bit Or 18-Bit Flat Panel Display (FPD) Link, 85 MHz*

11 Application Notes

- *AN-1032 An Introduction to FPD-Link*
- *AN-1056 STN Application Using FPD-Link*
- *AN-1059 High Speed Transmission with LVDS Link Devices*
- *AN-1084 Parallel Application of High Speed Link*
- *AN-1085 FPD-Link PCB and Interconnect Design-In Guidelines*
- *AN-1127 LVDS Display Interface (LDI) TFT Data Mapping for Interoperability*
- *AN-1163 TFT Data Mapping for Dual Pixel LDI Application*

12 Additional Information

For more information on FPD-Link Transmitters/Receivers, refer to TI's Signal Conditioning website.

For an overview of high-speed interface technologies, refer to the LVDS Owners Manual.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2011) to A Revision	Page
• Changed User's Guide format from National Semiconductor to TI format	2
• Deleted 60-pin IDC flat ribbon cable, User's Guide, datasheet, and LVDS Owner's Manual from kit list	2

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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