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LC898217XC

Auto Focus (AF) Controller & Driver



ON Semiconductor[®]

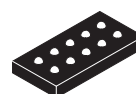
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1. Overview

LC898217XC is an AF control LSI. It consists of 1 system of feedback circuit for AF control.

2. Features

- Built-in equalizer circuit using digital operation
 - AF control equalize circuit
 - Any coefficient can be specified by 2-wire serial I/F (TWIF)
- 2-wire serial interface
(The communication protocol is compatible with I²C.)
- Built-in A/D converter
 - Input 1 channel
- Built-in D/A converter
 - Output 2 channel (Hall offset, Constant current bias)
- Built-in VGA
 - Hall Amp
 - 1 channel
- Built-in EEPROM
 - 128 byte (16 byte/page)
- Built-in OSC
- Built-in Constant Current Driver
 - 110 mA
 - 1 channel
- Package
 - WL-CSP 10-pin
 - Pb-Free, Halogen Free
- Supply voltage
 - V_{DD} (2.6 V to 3.3 V)



WLCSP10, 1.04x2.04

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

3. Pin Description

| TYPE | | | | | |
|------|-------------|---|-------------------|----|-------------|
| I | INPUT | P | Power supply, GND | NC | NOT CONNECT |
| O | OUTPUT | | | | |
| B | BIDIRECTION | | | | |

■ 2-wire serial interface

| | | |
|-----|---|-----------------------------------|
| SCL | I | 2-wire serial interface clock pin |
| SDA | B | 2-wire serial interface data pin |

■ Hall interface

| | | |
|-------|---|-------------------------------|
| BIASO | O | D/A output (to Hall element) |
| OPINP | I | VGA input (from Hall element) |
| OPINM | I | VGA input (from Hall element) |

■ Driver interface

| | | |
|------|---|-----------------------------|
| OUT1 | O | Driver output (to Actuator) |
| OUT2 | O | Driver output (to Actuator) |

■ Power supply pin

| | | |
|-----|---|--------------|
| VDD | P | Power supply |
| VSS | P | GND |

■ Test pin

| | | |
|------|---|--|
| PORT | B | Analog test signal input/output Convergence detection monitor output VSYNC input |
|------|---|--|

* Process when pins are not used

PIN TYPE "O" – Ensure that it is set to OPEN.

PIN TYPE "I" – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.

(Please contact ON Semiconductor for more information about selection of VDD or VSS.)

PIN TYPE "B" – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

* In case of connecting PORT pin with HOST CPU

When LC898217XC is power off and HOST CPU is power on, a HOST CPU pin connected with PORT pin have to be fixed "L" level.

LC898217XC

4. Pin Layout

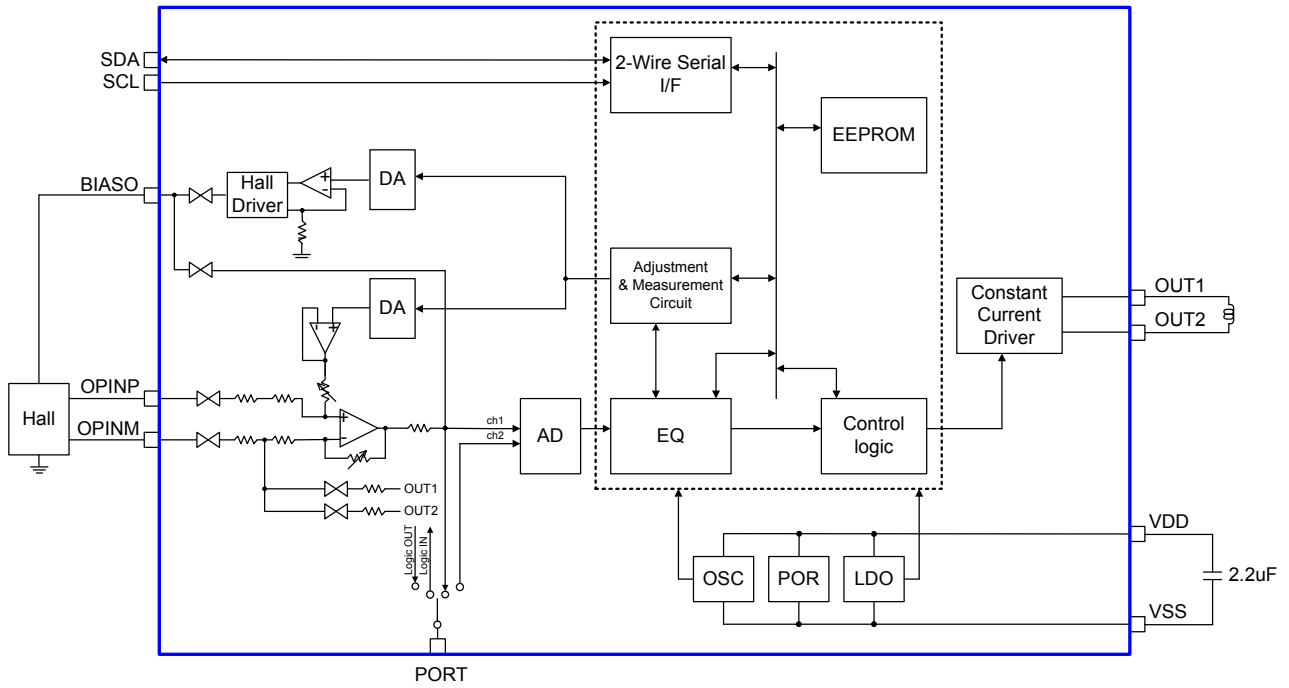
| Circuit Name | Number of PINs | Circuit Name | Number of PINs |
|--------------|----------------|--------------|----------------|
| Analog | 4 | Driver | 2 |
| Logic | 2 | Power | 2 |

“PORT” pin has analog function and digital function.

BOTTOM VIEW

| | A | B |
|---|-------|-------|
| 1 | OUT2 | OUT1 |
| 2 | VSS | VDD |
| 3 | PORT | SCL |
| 4 | BIASO | SDA |
| 5 | OPINM | OPINP |

5. Block Diagram

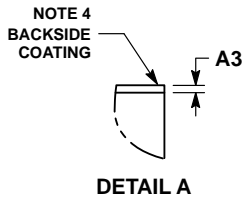
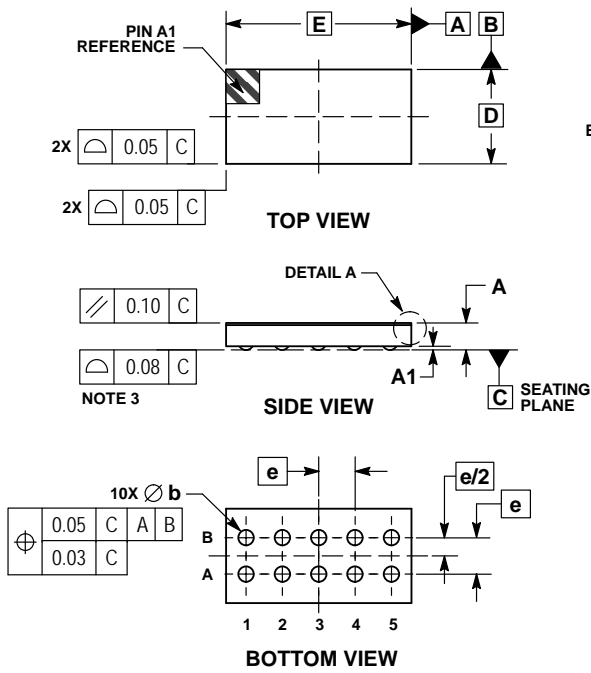


6. Package Dimensions

unit : mm

WLCSP10, 1.04x2.04

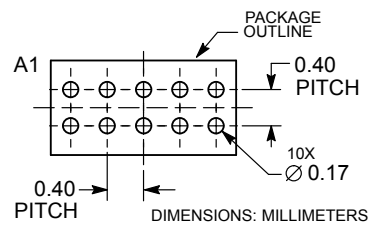
CASE 567LF
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 4. BACKSIDE COATING IS OPTIONAL.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.27 | 0.33 |
| A1 | 0.04 REF | |
| A3 | 0.025 REF | |
| b | 0.12 | 0.22 |
| D | 1.04 BSC | |
| E | 2.04 BSC | |
| e | 0.40 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

7. Electrical Characteristics

1) Absolute Maximum Rating at $V_{SS} = 0\text{ V}$

| Item | Symbol | Condition | Rating | Unit |
|-------------------------------|-----------------------|-----------------------------|------------------------|------------------|
| Supply voltage | $V_{DD33\text{ max}}$ | $T_a \leq 25^\circ\text{C}$ | -0.3 to 4.6 | V |
| Input/output voltage | V_{I33}, V_{O33} | $T_a \leq 25^\circ\text{C}$ | -0.3 to $V_{DD33}+0.3$ | V |
| Storage ambient temperature | Tstg | | -55 to 125 | $^\circ\text{C}$ |
| Operating ambient temperature | Topr | | -30 to 70 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Allowable Operating Ratings at $T_a = -30$ to 70°C , $V_{SS} = 0\text{ V}$

3 V power supply (V_{DD})

| Item | Symbol | Min | Typ | Max | Unit |
|---------------------|------------|-----|-----|------------|------|
| Supply voltage | V_{DD33} | 2.6 | 2.8 | 3.3 | V |
| Input voltage range | V_{IN} | 0 | | V_{DD33} | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3) DC Characteristics : Input/Output level at $V_{SS} = 0\text{ V}$, $V_{DD} = 2.6$ to 3.6 V , $T_a = -30$ to 70°C

| Item | Symbol | Condition | Min | Typ | Max | Unit | Applicable pins |
|---------------------------|----------|------------------------|--------------|-----|-----|------------|-----------------|
| High-level input voltage | V_{IH} | CMOS compliant Schmidt | 1.4 | | | V | SCL, SDA, PORT |
| Low-level input voltage | V_{IL} | | | | 0.4 | V | |
| High-level output voltage | V_{OH} | IOL = -2 mA | $V_{DD}-0.4$ | | | V | PORT |
| Low-level output voltage | V_{OL} | IOL = 2 mA | | | 0.4 | V | SDA, PORT |
| Pulldown resistor | Rdn | | 50 | | 220 | k Ω | PORT |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4) Driver output (OUT1, OUT2) at $V_{SS} = 0\text{ V}$, $V_{DD} = 2.8\text{ V}$, $T_a = 25^\circ\text{C}$

| Item | Symbol | Condition | Min | Typ | Max | Unit | Applicable pins |
|---------------------|-------------------|-----------|-----|-----|-----|---------------|-----------------|
| Maximum current | I _{full} | | 105 | | 115 | mA | OUT1, OUT2 |
| Output leak current | I _{leak} | | | 1 | | μA | |

5) Non-volatile Memory Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit | Applicable circuit |
|----------------|-----------------|-----------|-----|-----|------|--------|--------------------|
| Endurance | EN | | | | 1000 | Cycles | EEPROM |
| Data retention | RT | | 10 | | | Years | |
| Write time | t _{WT} | | | | 20 | ms | |

8. AC Characteristics

8.1 V_{DD} supply timing

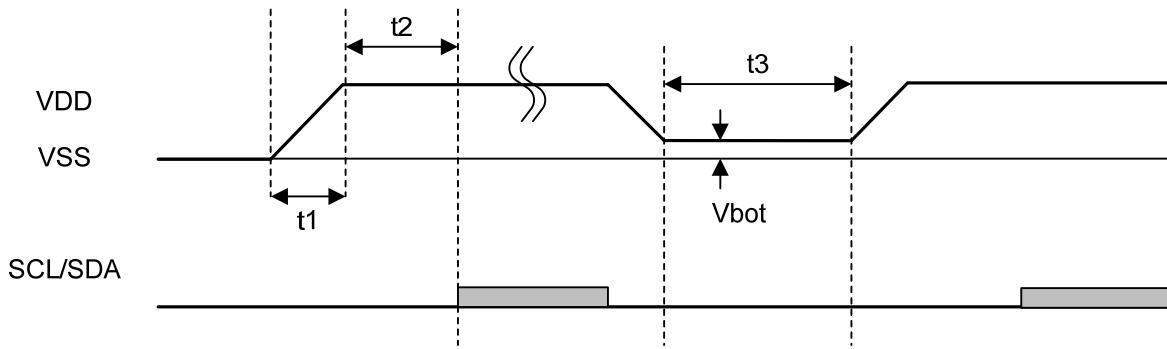


Figure 8.1 V_{DD} supply timing

It is available to use 2-wire serial interface 5 ms later for Power On Reset of V_{DD}.

| Item | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----|-----|------|
| V _{DD} turn on time | t1 | | | 3 | ms |
| 2-wire serial interface start time from V _{DD} on | t2 | 5 | | | ms |
| V _{DD} off time | t3 | 100 | | | ms |
| Bottom Voltage | Vbot | | | 0.1 | V |

8.2 AC specification

Figure 8.2 shows interface timing definition and Table 8.1 shows electric characteristics.

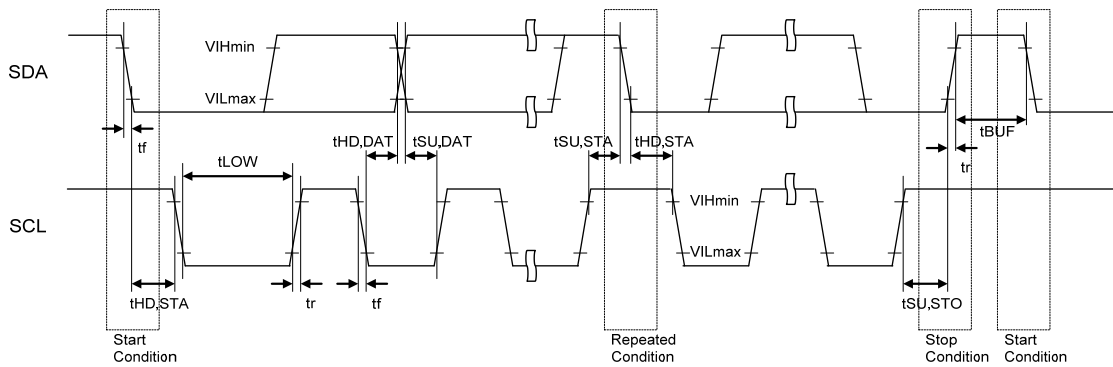


Figure 8.2 2-wire serial interface timing definition

Table 8.1 Electric characteristics for 2-wire serial interface (AC characteristics)

| Item | Symbol | Pin name | Fast-mode | | | Fast-mode Plus | | | Unit |
|---|----------------------|------------|-----------|-----|-----|----------------|-----|------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| SCL clock frequency | FSCL | SCL | | | 400 | | | 1000 | kHz |
| START condition hold time | t _{HD, STA} | SCL SDA | 0.6 | | | 0.26 | | | μs |
| SCL clock Low period | t _{LOW} | SCL | 1.3 | | | 0.5 | | | μs |
| SCL clock High period | t _{HIGH} | SCL | 0.6 | | | 0.26 | | | μs |
| Setup time for repetition START condition | t _{SU, STA} | SCL SDA | 0.6 | | | 0.26 | | | μs |
| Data hold time | t _{HD, DAT} | SCL SDA | 0 (*3) | | 0.9 | 0 (*3) | | | μs |
| Data setup time | t _{SU, DAT} | SCL SDA | 100 | | | 50 | | | ns |
| SDA, SCL rising time | t _r | SCL SDA | | | 300 | | | 120 | ns |
| SDA, SCL falling time | t _f | SCL SDA | | | 300 | | | 120 | ns |
| STOP condition setup time | t _{SU, STO} | SCL SDA | 0.6 | | | 0.26 | | | μs |
| Bus free time between STOP and START | t _{BUF} | SCL SDA | 1.3 | | | 0.5 | | | μs |

*3: LC898217XC is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

LC898217XC

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|--|--------------------------|
| LC898217XC-MH | WLCSP10, 1.04x2.04 (Pb-Free / Halogen Free) | 4000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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