User's Guide
SNVA400B–August 2009–Revised May 2013

# AN-1976 LM5027 Evaluation Board

## 1 Introduction

The LM5027 evaluation board is designed to provide the design engineer with a fully functional power converter based on the Active Clamp Forward topology to evaluate the LM5027 controller. The evaluation board is provided in an industry standard quarter-brick footprint.

The performance of the evaluation board is as follows:

Input Operating Range: 36 to 78V (100V peak)

Output Voltage: 3.3V

Output Current: 0 to 30A

Measured Efficiency: 90.5% @ 30A, 92.5% @ 15A

Frequency of Operation: 250 kHz

Board Size: 2.3 X 1.45 x 0.5 inches

Load Regulation: 1%

Line Regulation: 0.1%

Line UVLO, Hiccup Current Limit

The printed circuit board consists of 6 layers of 2 ounce copper on FR4 material with a total thickness of 0.050 inches. The unit is designed for continuous operation at rated load at <40°C and a minimum airflow of 200 CFM.

## 2 Theory of Operation

Power converters based on the Forward topology offer high efficiency and good power handling capability in applications up to several hundred Watts. The operation of the transformer in a forward topology does not inherently self-reset each power switching cycle; a mechanism to reset the transformer is required. The active clamp reset mechanism is presently finding extensive use in medium level power converters in the 50 to 200W range.

The Forward converter is derived from the Buck topology family, employing a single modulating power switch. The main difference between the topologies are, the Forward topology employs a transformer to provide input / output ground isolation and a step down or step up function.

Each cycle, the main primary switch turns on and applies the input voltage across the primary winding, which has 12 turns. The transformer secondary has 2 turns, leading to a 6:1 step-down of the input voltage. For an output voltage of 3.3V the required duty cycle (D) of the main switch must vary from approximately 60% (low line) to 25% (high line). The clamp capacitor along with the reset switch reverse biases the transformer primary each cycle when the main switch turns off. This reverse voltage resets the transformer. The clamp capacitor voltage is Vin / (1-D).

Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an optocoupler. The LM5027 voltage mode controller pulse width modulates the error signal with a ramp signal derived from the input voltage. Deriving the ramp signal slope from the input voltage provides line feed-forward, which improves line transient rejection. The LM5027 also provides a controlled delay necessary for the reset switch. The evaluation board can be synchronized to an external clock with a recommended frequency range of 275 to 300 kHz.

# 3 Schematic

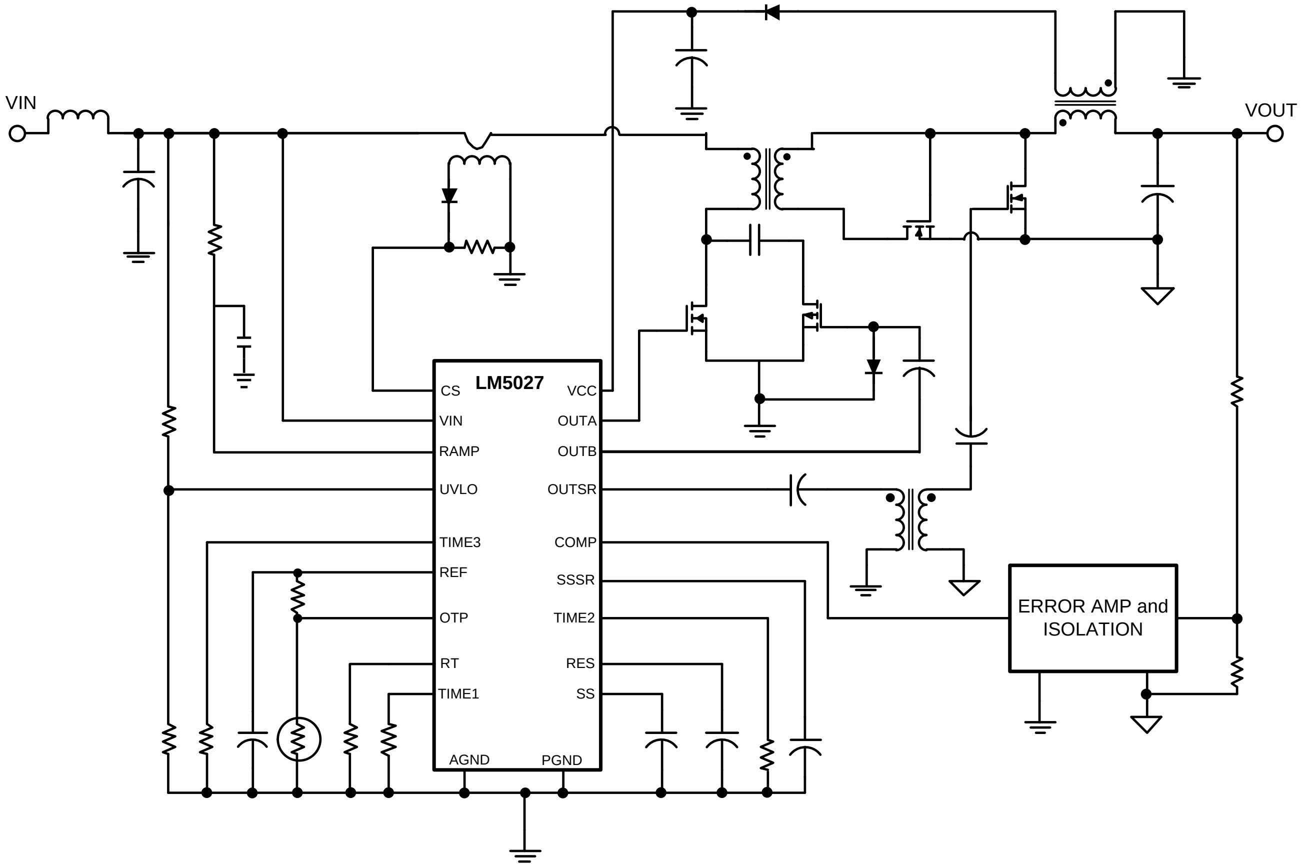


Figure 1. Board Schematic

# 4 Powering and Loading Considerations

When applying power to the LM5027 evaluation board certain precautions need to be followed. A failure or mis-connection can present itself in a very alarming manner.

## *4.1 Proper Connections*

When operated at low input voltages the evaluation board can draw up to 3.5A of current at full load. The maximum rated output current is 30A. Be sure to choose the correct connector and wire size when attaching the source supply and the load. Monitor the current into and out of the evaluation board. Monitor the voltage directly at the output terminals of the evaluation board. The voltage drop across the load connecting wires will give inaccurate measurements; this is especially true for accurate efficiency measurements.

## *4.2 Source Power*

The evaluation board can be viewed as a constant power load. At low input line voltage (36V) the input current can reach 3.5A, while at high input line voltage (78V) the input current will be approximately 1.5A. Therefore too fully test the LM5027 evaluation board a DC power supply capable of at least 80V and 4A is required. The power supply must have adjustments for both voltage and current. An accurate readout of output current is desirable since the current is not subject to loss in the cables as voltage is. The power supply and cabling must present a low impedance to the evaluation board. Insufficient cabling or a high impedance power supply will droop during power supply application with the evaluation board inrush current. If large enough, this droop will cause a chattering condition upon power up. This chattering condition is an interaction with the evaluation board undervoltage lockout, the cabling impedance and the inrush current.

### 4.3 Loading

An appropriate electronic load, with specified operation down to 3.0V minimum, is desirable. The resistance of a maximum load is 0.11Ω. You need thick cables! Consult a wire chart if needed. If resistor banks are used there are certain precautions to be taken. The wattage and current ratings must be adequate for a 30A, 100W supply. Monitor both current and voltage at all times. Ensure there is sufficient cooling provided for the load.

### 4.4 Air Flow

An appropriate electronic load, with specified operation down to 3.0V minimum, is desirable. The resistance of a maximum load is 0.11Ω. You need thick cables! Consult a wire chart if needed. If resistor banks are used there are certain precautions to be taken. The wattage and current ratings must be adequate for a 30A, 100W supply. Monitor both current and voltage at all times. Ensure there is sufficient cooling provided for the load.

### 4.5 Powering Up

Using the shutdown pin provided will allow powering up the source supply with the current level set low. It is suggested that the load be kept quite nominal during the first power up. Set the current limit of the source supply to provide about 1.5 times the wattage of the load. As you remove the connection from the shutdown pin to ground, immediately check for 3.3 volts at the output.

A most common occurrence, that will prove unnerving, is when the current limit set on the source supply is insufficient for the load. The result is similar to having the high source impedance referred to earlier. The interaction of the source supply folding back and the evaluation board going into undervoltage shutdown will start an oscillation, or chatter, that may have highly undesirable consequences.

A quick efficiency check is the best way to confirm that everything is operating properly. If something is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

### 4.6 Over Current Protection

The evaluation board is configured with hiccup over-current protection. In the event of an output overload (approximately 33A) the unit will discharge the softstart capacitor, which disables the power stage. After a delay the soft-start is released. The shutdown, delay and slow recharge time of the softstart capacitor protects the unit, especially during short circuit event where the stress is highest.

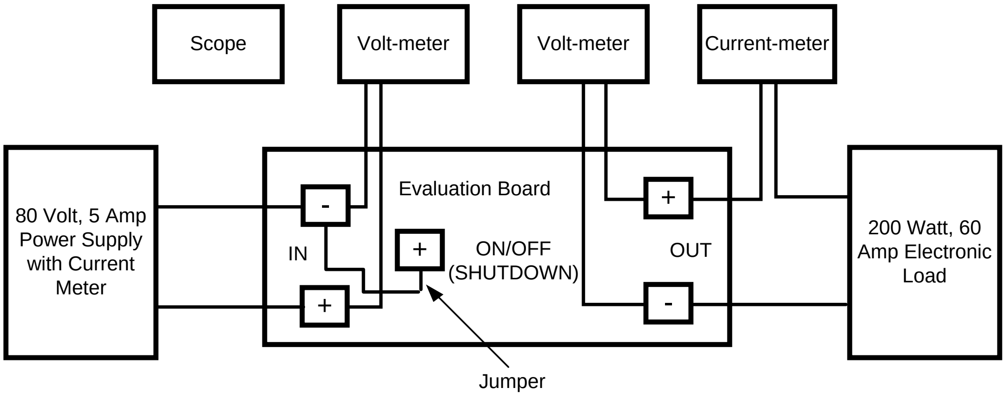


**Figure 2. Typical Evaluation Setup**

## 5 Start-Up

Power supplies have a soft-start circuit(s) to control their output voltage when input power is applied. The soft-start sequence limits the peak inrush current as the output capacitors are charged, and prevents the output voltage from over-shooting. In most power supplies there are primary side and secondary side soft-start circuits.

The primary side soft-start circuit is generally in a primary side controller and the soft-start time is set with an external capacitor. The function of the primary side soft-start circuit is to slowly increasing the duty cycle of the controller from zero to the maximum duty cycle. The maximum duty cycle varies based on the controller and the circuit topology.

The secondary side soft-start circuit connects a resistor/capacitor from the secondary side voltage reference to the positive input of the error amplifier. The soft-start time is set by the resistor/capacitor time constant and works by ramping up the voltage reference on the secondary side error amplifier. The output of the error amplifier is fed across the isolation boundary to the primary side controller compensation input which is connected to the controller PWM input. The voltage at the compensation input increases to a value required for regulation as determined by the voltage feedback loop. The secondary side soft-start along with the primary side soft-start work together to control the duty cycle on start-up to controlling the power supplies output start-up time, and limit the stress on the power components.

Figure 3 shows the primary and secondary side soft-start sequence using the LM5027 into an electronic load. After Vin is applied the primary side soft-start ramps up. When the voltage on the LM5027 SS pin reached 1.0 V the output drives start and power is delivered to the secondary of the transformer. The power supply output rises and the secondary side soft-start circuit begins to ramp-up. The output of the DC-DC converter monotonically increased with no overshoot to 3.3 V out.

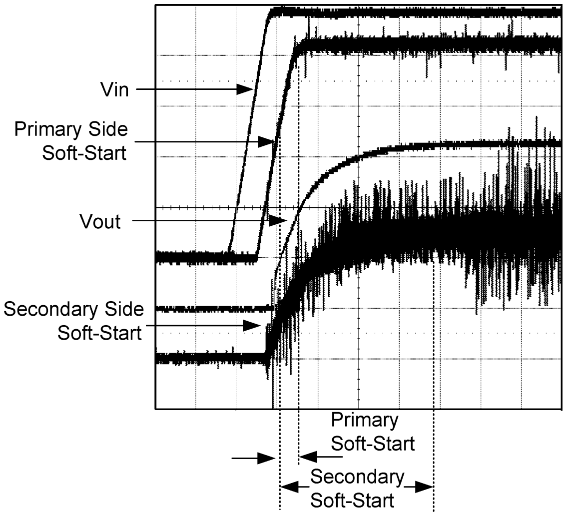


Figure 3. Soft-Start

## 6 Pre-Bias Load Start-Up

Figure 4 shows a typical Forward Converter topology with an active clamp using self-driven synchronous rectification. It’s simple and very efficient; however there are some disadvantages when starting this topology into a pre-biased load. The first occurs because the synchronous rectification is on the secondary side of the transformer and without adding intelligence the output current will flow into the converter via the output choke and the free wheeling MOSFET when the converter starts-up or shut down with pre-bias voltage.

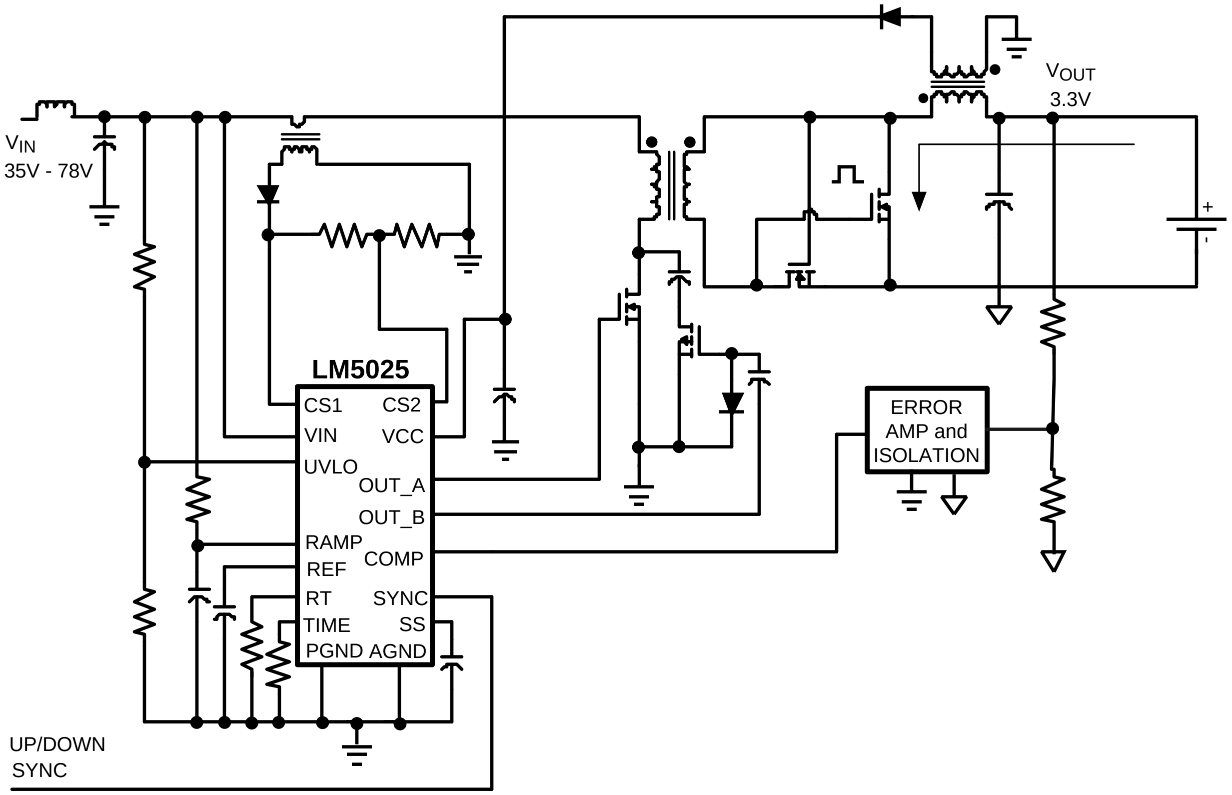


**Figure 4. Typical Forward Converter**

## 7 OUTSR Drive

The LM5027 has a dedicated pin (OUTSR) to drive the synchronous rectifier free wheeling MOSFET through a drive transformer as shown in Figure 5. When the converter starts-up, the OUTSR drive is held low and the freewheeling MOSFET is turned-off. As a result, no output current will sink into the converter. The OUTSR is enabled after the primary side soft-start reaches approximately 4.0V. The OUTSR delay was added to ensure that the power supply output voltage is up and in regulation prior to the freewheeling MOSFET being turned-on, refer to Figure 6 and Figure 7. The OUTSR drive is soft-started; a capacitor on the SSSR pin is released and is charged with a 25 µA current source, slowly increasing the duty cycle of the freewheeling FET's duty cycle.

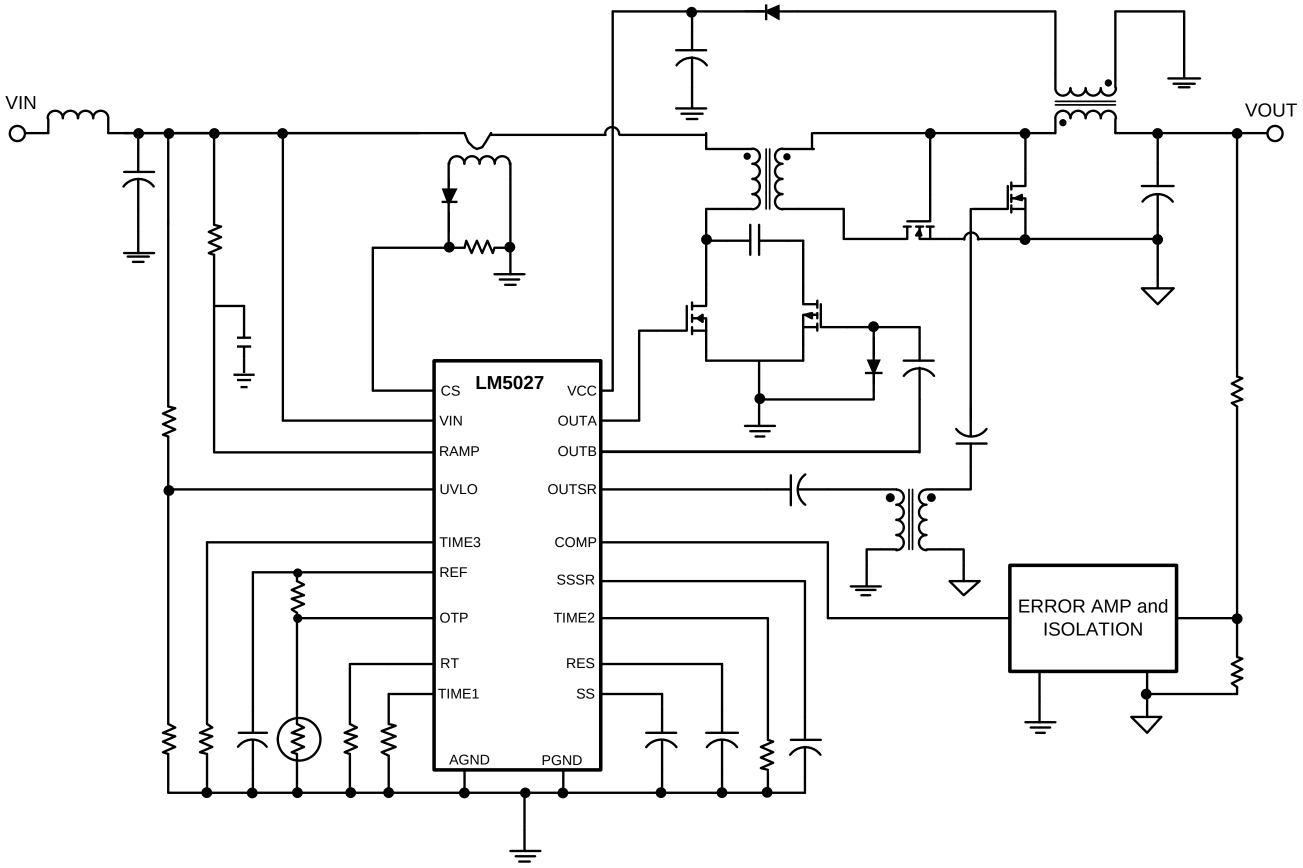


Figure 5. LM5027 Synchronous Rectifier Drive Output (OUTSR)

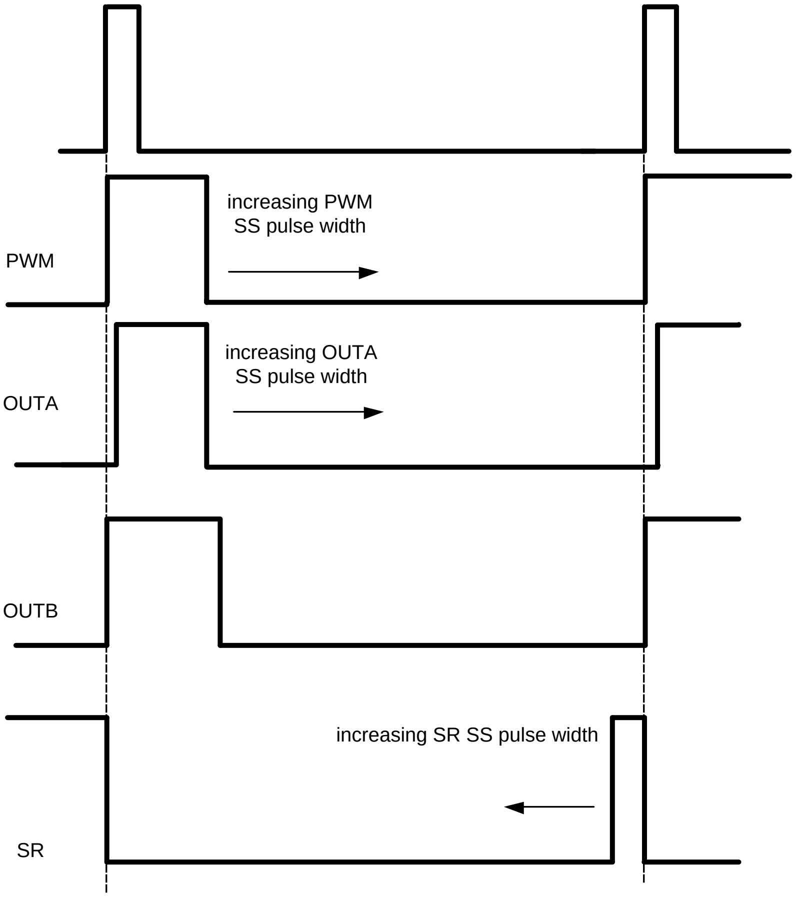


Figure 6. LM5027 Drive Timing

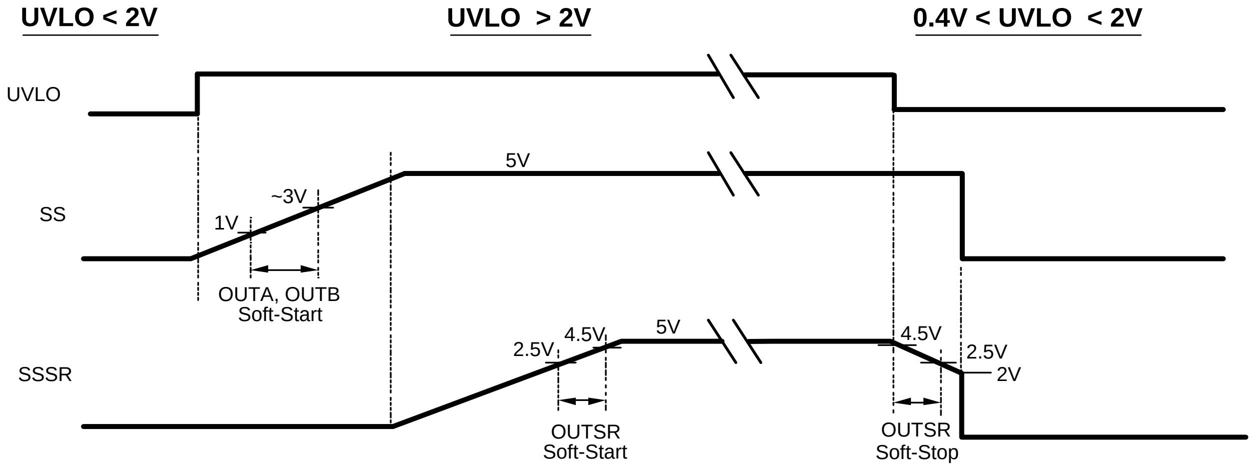


Figure 7. LM5027 Soft-Start Waveforms

## 8 Secondary Side Soft-Start

In a typical DC-DC converter with a 3.3 V output the voltage reference for the error amplifier is 1.2V. Prior to the power supply being turned-on and if there is a pre-bias load, the secondary side soft-start capacitor (CSS) will be pre-charged to the voltage reference level of 1.2 V (if the pre-bias load > 1.2V), refer to Figure 9. On start-up the primary side soft-start begins and the output voltage rises from the pre-bias voltage level to 3.3 V, refer to Figure 8. At the end of the primary side soft-start period the controller will be at maximum duty cycle and the output voltage will overshoot until the feedback error amplifier has a chance to respond and reduce the output voltage to the regulation set point.

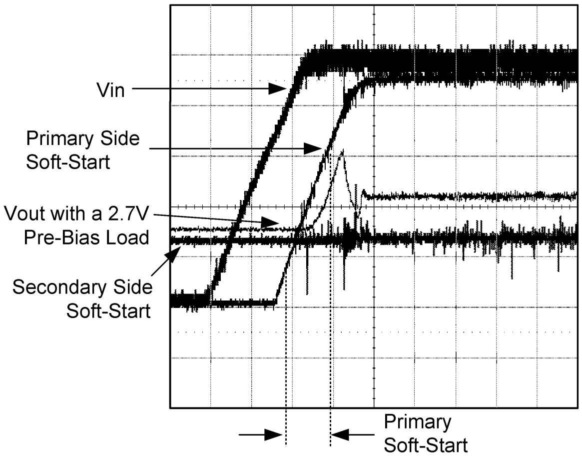


**Figure 8. Pre-bias Secondary Side Soft-Start**

## 9 Secondary Side Soft-Start Reset

When input power is supplied to the LM5027 Evaluation Board the LM5027's internal VCC Regulator turns-on providing power to the VCC pin, the primary side soft-start voltage increases, and the output drives are enabled. When the drive outputs are enables the voltage on the transformer secondary increases, the Secondary Bias rises supplying voltage to the reference and error amplifier, refer to Figure 10. During this time FET Q1 is turned-on holding the reference voltage at the positive input to the error amplifier low (zero volts). When the voltage on the secondary bias capacitor ($C_{BIAS}$) rises above the Zener diode> 3.6 V, the Secondary Bias Power Good (the collector of Q2) goes high. This turns-off FET Q1 allowing the secondary soft-start capacitor to charge up. This solution of reseting the soft-start capacitor to zero (0 V) on start-up works for pre-bias loads as well as loads that do not need to start into a pre-biased condition. This allows for a monotonic start-up under both operating modes.

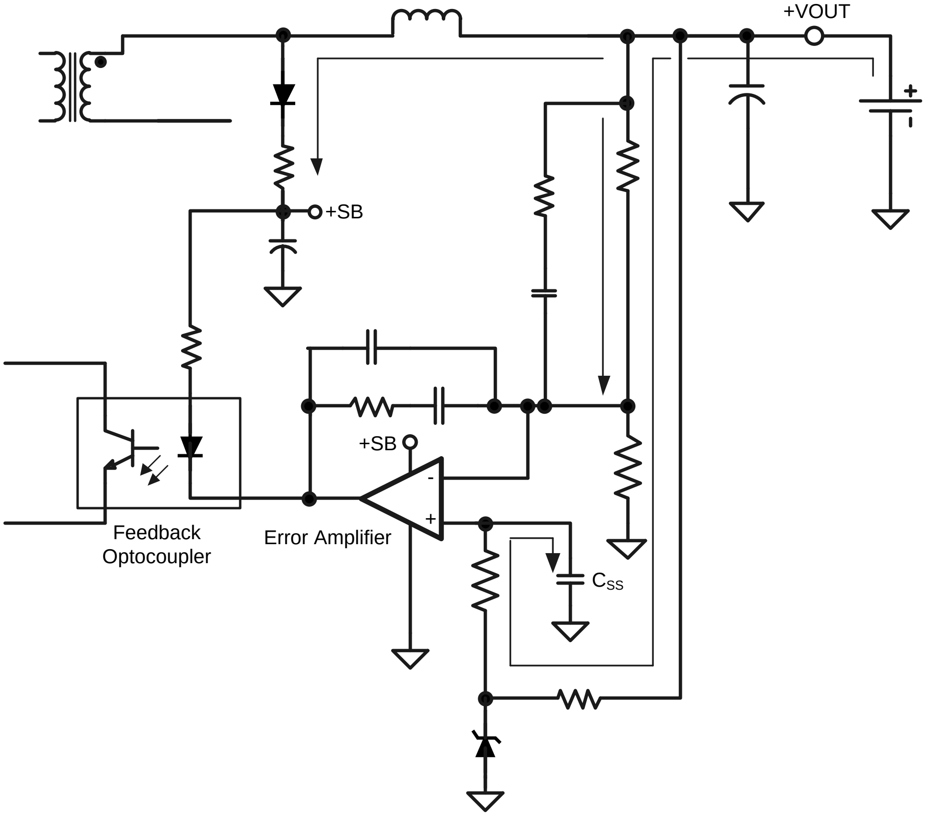


Figure 9. VREF with Pre-Bias Load

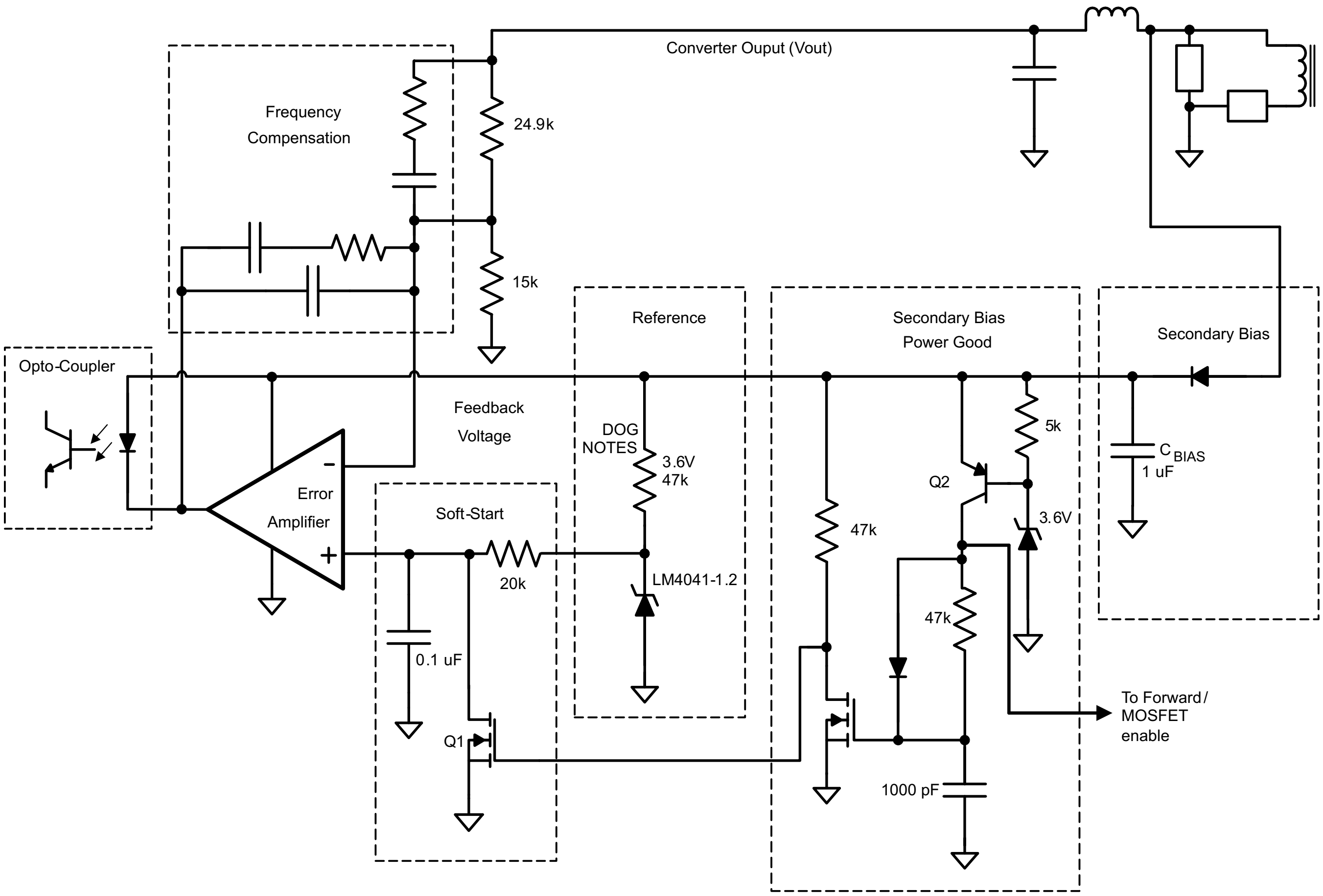


Figure 10. Pre-Bias Schematic

## 10 Pre-Bias Load-Synchronous Forward MOSFET Enabled

The self driven synchronous rectification topology has an issues starting into a pre-bias load. When a pre-bias load is connected across the power supply output, refer to Figure 11, the pre-bias source will conduct current through the output inductor and the self driven gate drive resistors R1 and R2. If the pre-bias voltage is greater than the Vgs of the synchronous MOSFET (M1), the MOSFET will be turned-on sinking current into the power supply.

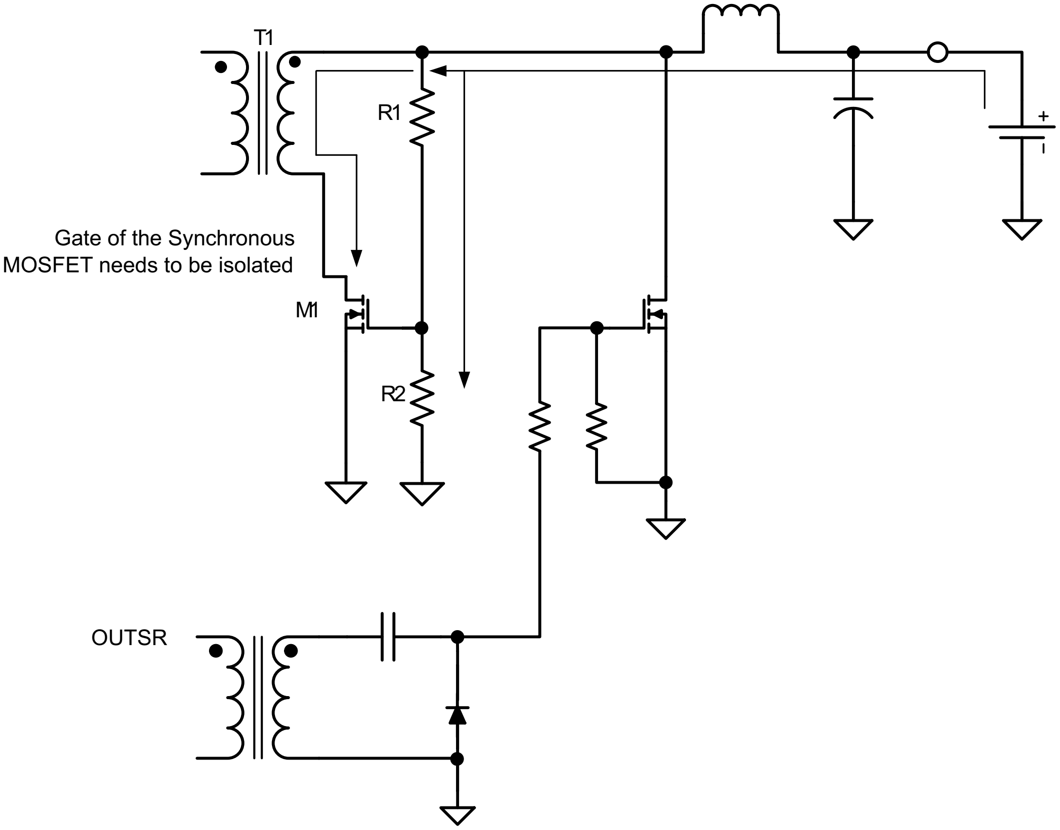


**Figure 11. Self Driven with Pre-Bias Load**

## 11 Synchronous Forward MOSFET Enabled

For the LM5027 Evaluation board we used the Secondary Bias Power Good signal as a flag to indicate that the primary sides MOSFETs are switching providing power to the secondary of the transformer T1. When the flag goes high this indicates that it is time to turn-on the forward conducting MOSFET M1. The Secondary Bias Power Good signal drives the base of an NPN transistor (Q3), refer to Figure 12. The NPN transistor is configured as a Cascod amplifier; when it is turned-on, the voltage on the secondary of the transformer T1 drives the gate of the synchronous MOSFET, M1. The MOSFET gate drive voltage is:

$$\text{V-GATE\_DRIVE\_M1} = \text{V\_Secondary\_Bias\_Power\_Good-VBE\_Q3} \quad (1)$$

An NPN transistor needs to be selected so that the transistors collector to emitter voltage under the worst case operating condition does not exceed it’s VCE ratings, and that the collector current (Icc) can handle the maximum peak current to drive the gate of MOSFET M1. For the LM5027 Evaluation board the transistor is a 30 V, 1.5 ampere transistor. The maximum VCE is:

$$\text{VCE} = \frac{\text{Vin\_max}}{\text{n}} = \frac{100}{6} = 16.67\ \text{Vpk}$$

where

- Vin = 100 V under transient conditions
- n is the transformer turns ratio = 6
- (2)

A diode D1 is connected from the collector to the emitter of Q3 to handle any voltage spikes as a result of circuit inductance. Without this diode inductive voltage spike may damage the Cascod amplifier Q3.

An NPN transistor was use instead of an N-Channel MOSFET because the Vgs drop, typically 4 to 5 volts; this would reduce the gates drive voltage to M1. Under minimum input line conditions M1 may not be fully turned-on and there would be an increase in the $I^2$ x $R_{DS(ON)}$ losses.

Figure 13 shows the start-up waveforms for the Evaluation board. After the input power is supplied to the Evaluation board the secondary bias voltage rises, when the secondary bias is greater than 3.6 V, the Secondary Power Good output goes high. This turns-on M1 and enables the secondary side soft-start circuit allowing the output voltage to increase after Vout > Vpre-bias.

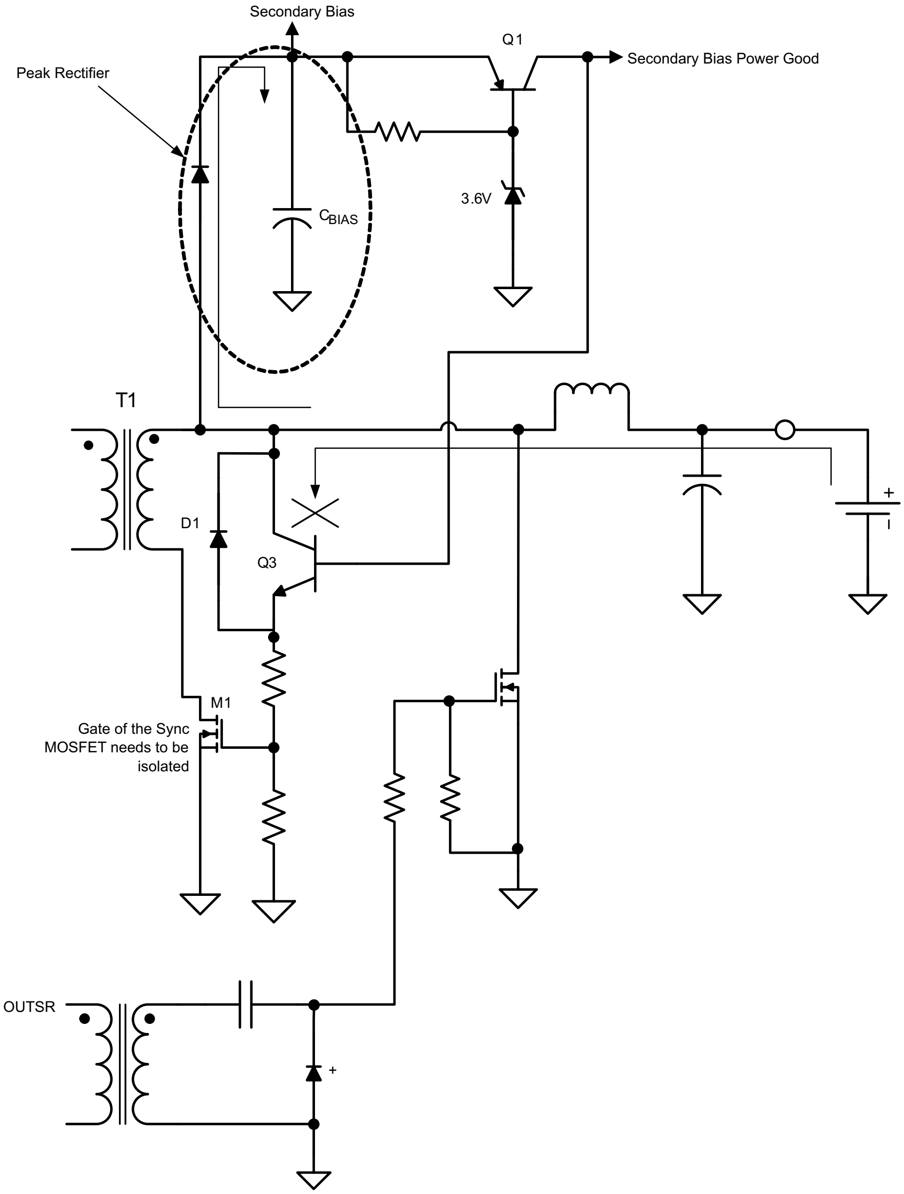


Figure 12. Isolated Synchronous MOSFET

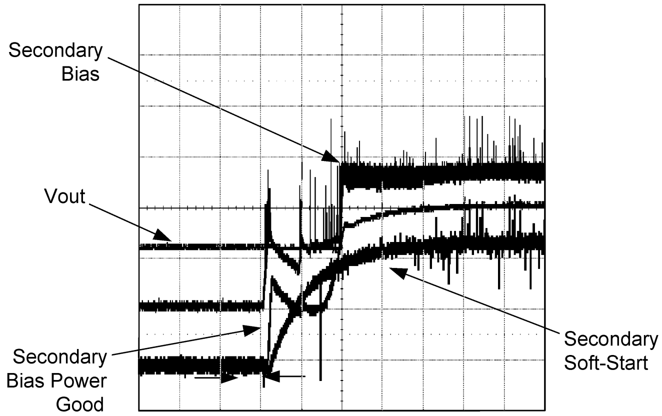


**Figure 13. Pre-Bias Load Waveforms**

An alternative to using the circuit in Figure 12 is shown in Figure 14; an additional winding can be added to the power transformer which can be used to drive the Forward Synchronous Rectifier MOSFET (M1). This is a simple solution and should not add a lot of complexity to the transformer design.

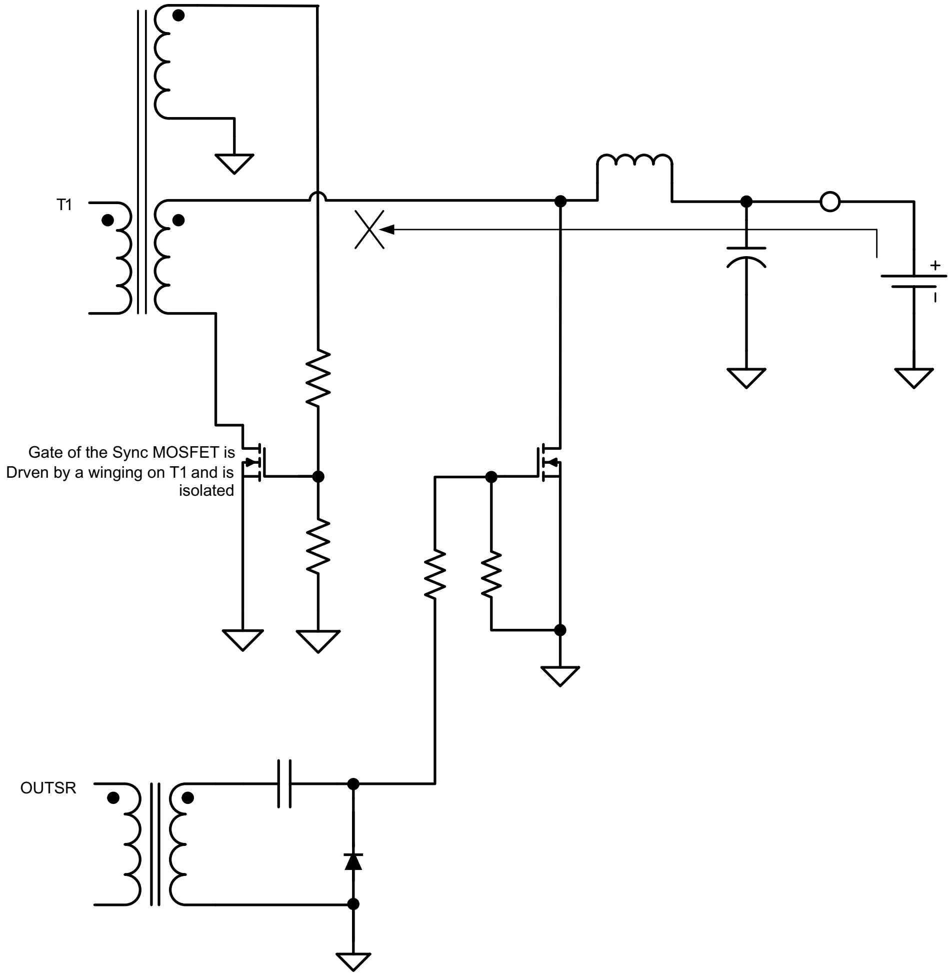


**Figure 14. Isolated Synchronous MOSFET Drive Using a Transformer**

## 12 Pre-Bias Load Test Set-Up

For the Pre-bias start-up test, the circuit in Figure 15 was used. An external bias supply, through a 1.0 ohm resistor, was connected across the output terminals of the Evaluation Board.

## 13 Pre-Bias Load Start-Up Requirements

The Evaluation board Pre-Bias start-up requirements are:

During converter start-up the output shall rise monotonically and not sink current (into the converter) of more than 50 mA.

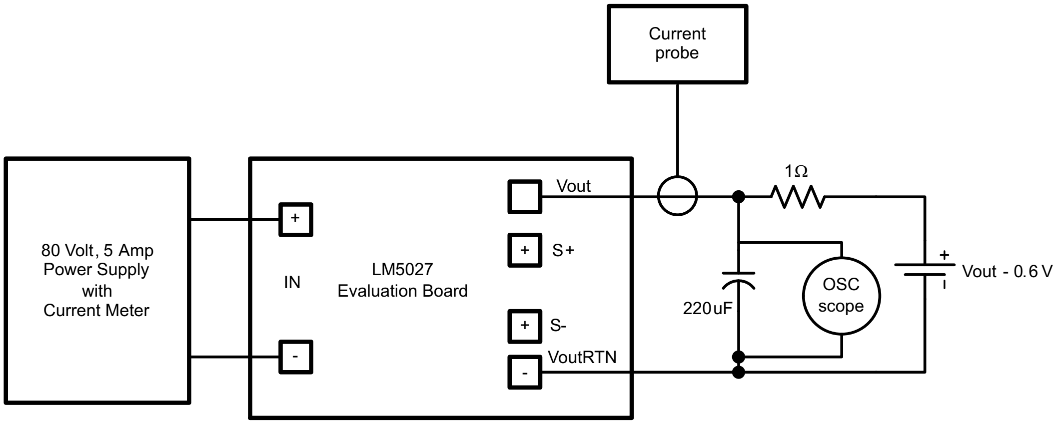


**Figure 15. Isolated Synchronous MOSFET Drive Using a Transformer**

## 14 Evaluation Board Results

Figure 16 shows the output of the Evaluation Board starting with a pre-bias voltage of 2.7 V. Under these conditions the output voltage starts at 2.7 V and then increases monotonically to 3.3 V. The current into the Evaluation board (sinking) is less than 50 mA. When the output voltage rise above the pre-bias voltage there is approximately 400 mA of current out of (sourced) the Evaluation Board to charge the external 220 µF capacitor. After the external capacitor is charge to 3.3 V the current out of the power supply drop to approximately 50 mA.

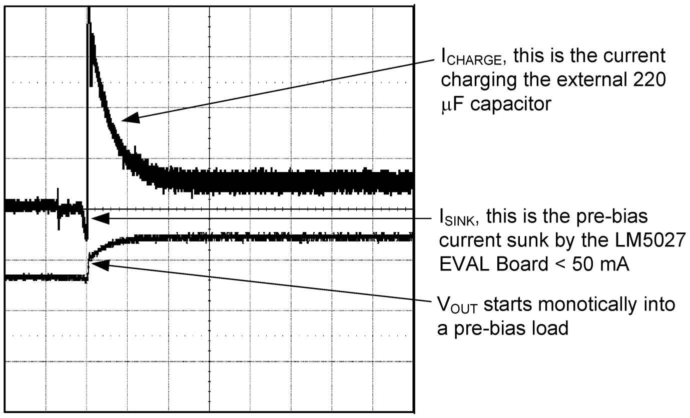


**Figure 16. Pre-Bias StartUp**

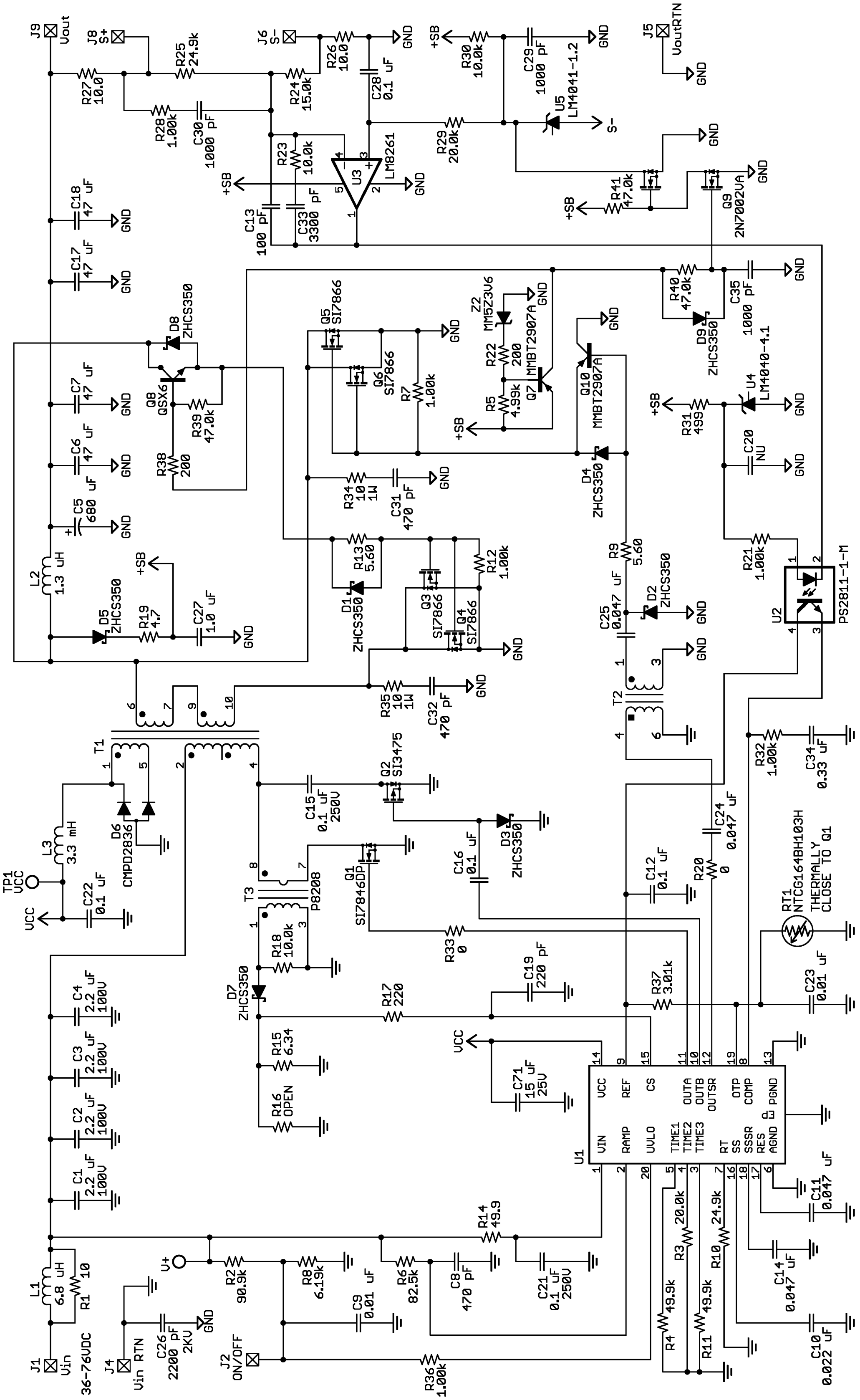


Figure 17. Application Schematic: Input 36-76, Vout 6.3A, 30A

## 15 Performance Characteristics

### Turn-on Waveforms

When applying power to the LM5027 evaluation board a certain sequence of events occurs. Soft-start capacitor values and other components allow for a minimal output voltage for a short time until the feedback loop can stabilize without overshoot. Figure 18 shows the output voltage during a typical start-up with a 48V input and a load of 5A. There is no overshoot during startup.

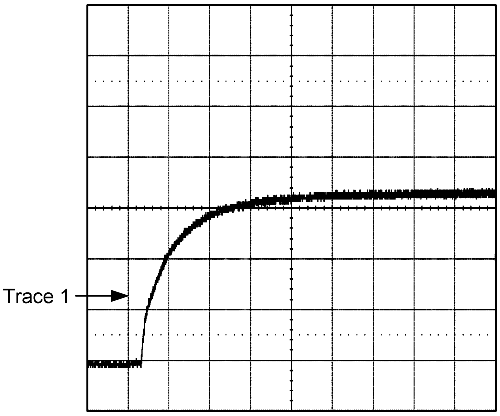
### Output Ripple Waveforms

Figure 19 shows the transient response for a load of change from 2A to 25A. The lower trace shows minimal output voltage droop and overshoot during the sudden change in output current shown by the upper trace.

Figure 20 shows typical output ripple seen directly across the output capacitor, for an input voltage of 48V and a load of 30A. This waveform is typical of most loads and input voltages.

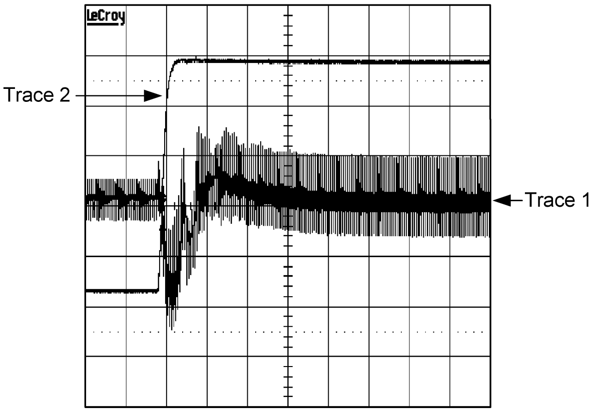
Figure 21 and Figure 22 show the drain voltage of Q1 with a 25A load. Figure 21 represents an input voltage of 38V and Figure 22 represents an input voltage of 78V.

Figure 23 shows the gate voltages of the synchronous rectifiers. The drive from the main power transformer is delayed slightly at turn-on by a resistor interacting with the gate capacitance. This provides improved switching transitions for optimum efficiency. The difference in drive voltage is inherent in the topology and varies with line voltage



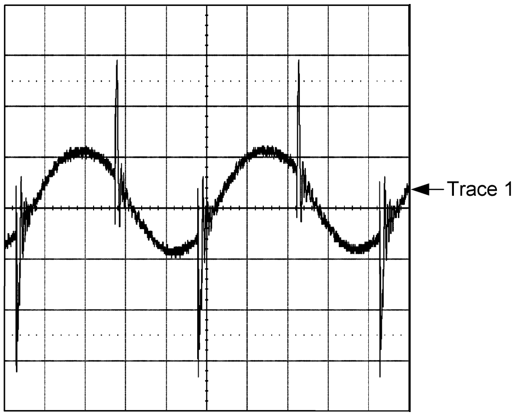
Conditions: Input Voltage = 48VDC Output Current = 5A Trace 1: Output Voltage Volts/div = 1.0V Horizontal Resolution =1 ms/div

**Figure 18. Turn-On Waveforms**



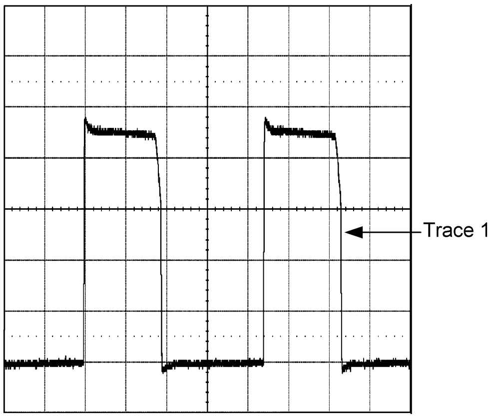
Conditions: Input Voltage = 48VDC Output Current = 2A to 25A Trace1: Output Voltage Volts/div = 0.2V Trace 2: Output Current Amps/Div = 5.0 A Horizontal Resolution = 1 ms/div

**Figure 19. Output Ripple Waveforms**



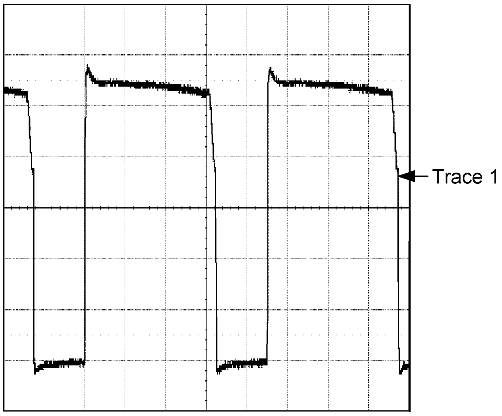
Conditions: Input Voltage = 48VDC Output Current = 30A Bandwidth Limit = 25 MHz Trace 1: Output Voltage Volts/div = 50 mV Horizontal Resolution = 2 µs/div

**Figure 20. Output Ripple**



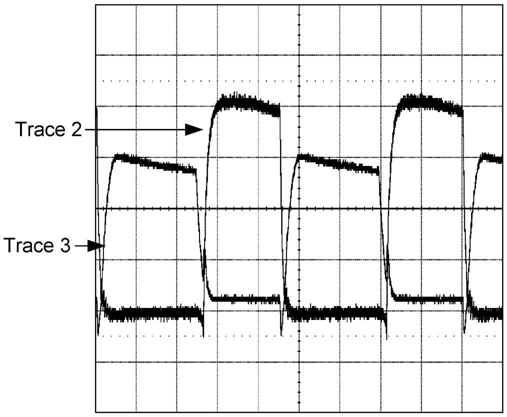
Conditions: Input Voltage = 38VDC Output Current = 25A Trace 1: Q1 Drain Voltage volts/Div = 20V Horizontal Resolution = 1 µs/div

**Figure 21. Drain Voltage**



Conditions: Input Voltage = 78VDC Trace 1: Q1 Drain Voltage Volts/Div = 20V Horizontal Resolution = 1 µs/div

**Figure 22. Drain Voltage**



Conditions: Input Voltage = 48VDC Output Current = 5A Trace 3: (gate) Synchronous Rectifier, Q3/Q4 Volts/Div = 2V Trace 2: (gate) Synchronous Rectifier, Q5/Q6 Volts/Div = 2V Horizontal Resolution = 1 µs/div

**Figure 23. Gate Voltages**

## 16 Bill of Materials

| Item | | Part Number | Description | Value |
|---|---|---|---|---|
| C | 1 | C4532X7R2A225M | CAPACITOR, CER, TDK | 2.2µ, 100V |
| C | 2 | C4532X7R2A225M | CAPACITOR, CER, TDK | 2.2µ, 100V |
| C | 3 | C4532X7R2A225M | CAPACITOR, CER, TDK | 2.2µ, 100V |
| C | 4 | C4532X7R2A225M | CAPACITOR, CER, TDK | 2.2v, 100V |
| C | 5 | APXE4R0ARA681MH80G | CAPACITOR, CER, United Chemi-Con | 680µ, 4V |
| C | 6 | C1210C476M8PACTU | CAPACITOR,CER,KEMET | 47µ, 10V |
| C | 7 | C1210C476M8PACTU | CAPACITOR,CER,KEMET | 47µ, 10V |
| C | 8 | C0603C471J5GAC | CAPACITOR, CER, KEMET | 470p, 50V |
| C | 9 | C0603C103K3RAC | CAPACITOR, CER, KEMET | 0.01µ, 25V |
| C | 10 | C0603C223K3RAC | CAPACITOR, CER, KEMET | 0.022µ, 25V |
| C | 11 | C0603C473K3RAC | CAPACITOR, CER, KEMET | 0.047µ, 25V |
| C | 12 | C1608X7R1H104K | CAPACITOR, CER, TDK | 0.1µ, 50V |
| C | 13 | C0603C101J5GAC | CAPACITOR, CER, KEMET | 100p, 50V |
| C | 14 | C0603C104K3RAC | CAPACITOR, CER, KEMET | 0.1µ, 25V |
| C | 15 | C3216X7R2E104K | CAPACITOR, CER, TDK | 0.1µ, 250V |
| C | 16 | C1608X7R1H104K | CAPACITOR, CER, TDK | 0.1µ, 50V |
| C | 17 | C1210C476M8PACTU | CAPACITOR, CER, TDK | 47µ, 10V |
| C | 18 | C1210C476M8PACTU | CAPACITOR, CER, TDK | 47µ, 10V |
| C | 19 | C0603C221J3GAC | CAPACITOR, CER, KEMET | 220p, 25V |
| C | 20 | OPEN | | |
| C | 21 | C3216X7R2E104K | CAPACITOR, CER, TDK | 0.1µ, 250V |
| C | 22 | C1608X7R1H104K | CAPACITOR, CER, KEMET | 0.1µ, 25V |
| C | 23 | C0603C103K3RAC | CAPACITOR, CER, KEMET | 0.01µ, 25V |
| C | 24 | C0603C473K3RAC | CAPACITOR, CER, KEMET | 0.047µ, 25V |
| C | 25 | C0603C473K3RAC | CAPACITOR, CER, KEMET | 0.047µ, 25V |
| C | 26 | C4532X7R3D222K | CAPACITOR, CER, TDK | 2200p, 2000V |
| C | 27 | GRM188R61E105KA12D | CAPACITOR, CER, MURATA | 1.0µ, 25V |
| C | 28 | C0603C224K3RAC | CAPACITOR, CER, TDK | 0.22µ, 25V |
| C | 29 | C0603C102K3RAC | CAPACITOR, CER, KEMET | 1000p, 25V |
| C | 30 | C0603C102K3RAC | CAPACITOR, CER, KEMET | 1000p, 25V |
| C | 31 | C0805C471J5GAC | CAPACITOR, CER, KEMET | 470p, 50V |
| C | 32 | C0805C471F5GAC | CAPACITOR, CER, KEMET | 470p, 50V |
| C | 33 | C2012X7R2A332K | CAPACITOR, CER, TDK | 3300p, 100V |
| C | 34 | OPEN | | |
| C | 71 | C4532X7R1E156M | CAPACITOR, CER, TDK | 15µ, 25V |
| C | 35 | C0603C102K3RAC | CAPACITOR, CER, KEMET | 1000p, 25V |
| C | 36 | GRM188R61E105KA12D | CAPACITOR, CER, MURATA | 1.0u, 25V |
| D | 1 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 2 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 3 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 4 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 5 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 6 | CMD2836 | DIODE, DUAL SIGNAL, CENTRAL | 120V, 200mA |
| D | 7 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 8 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |
| D | 9 | ZHCS350 | DIODE, SIGNAL, ZETEX | 40V, 500mA |

| Item | | Part Number | Description | Value |
|---|---|---|---|---|
| J | 1 | 3104-2-00-01-00-00-08-0 | PIN, BRICK, 0.040D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 2 | 3104-2-00-01-00-00-08-0 | PIN, BRICK, 0.040D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 4 | 3104-2-00-01-00-00-08-0 | PIN, BRICK, 0.040D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 5 | 3231-2-00-01-00-00-08-0 | PIN, BRICK, 0.080D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 6 | 3104-2-00-01-00-00-08-0 | PIN, BRICK, 0.040D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 8 | 3104-2-00-01-00-00-08-0 | PIN, BRICK, 0.040D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| J | 9 | 3231-2-00-01-00-00-08-0 | PIN, BRICK, 0.080D, MILL-MAX | MOUNT ON SOLDER SIDE OF PCB |
| L | 1 | SRU1048-6R8Y | INPUT CHOKE, Bourns | 6.8uH, 4.8Arms |
| L | 2 | 7443556130 | CHOKE, WURTH | 1.2µH, 37A |
| L | 3 | SDR0503-332JL | CHOKE, Bourns | 3.3mH, 0.045 A |
| Q | 1 | SI7846DP | N-FET, SILICONIX | 150V, 50m |
| Q | 2 | SI3475 | P-FET, IR | 200V, 1.6 |
| Q | 3 | SI7866DP | FET, SILICONIX | 20V, 3m |
| Q | 4 | SI7866DP | FET, SILICONIX | 20V, 3m |
| Q | 5 | SI7866DP | FET, SILICONIX | 20V, 3m |
| Q | 6 | SI7866DP | FET, SILICONIX | 20V, 3m |
| Q | 7 | MMBT2907A | Bipolar, PNP, 60V, 600mA | |
| Q | 8 | QSX6 | Bipolar, NPN, 30V, 1.5A | ROHM |
| Q | 9 | 2N7002VA | FET, N_Channel, Fairchild | 60V 280mA |
| Q | 10 | MMBT2907A | Bipolar, PNP, 60V, 600mA | |
| R | 1 | CRCW120610R0F | RESISTOR | 10 |
| R | 2 | CRCW08059093F | RESISTOR | 90.9k |
| R | 3 | CRCW06032002F | RESISTOR | 20k |
| R | 4 | CRCW06034992F | RESISTOR | 49.9k |
| R | 5 | CRCW06034991F | RESISTOR | 4.99k |
| R | 6 | CRCW08059093F | RESISTOR | 90.9K |
| R | 7 | CRCW06031001F | RESISTOR | 1K |
| R | 8 | CRCW06036191F | RESISTOR | 6.19K |
| R | 9 | CRCW06035R60F | RESISTOR | 5.6 |
| R | 10 | CRCW06032492F | RESISTOR | 24.9K |
| R | 11 | CRCW06034992F | RESISTOR | 49.9K |
| R | 12 | CRCW06031001F | RESISTOR | 1K |
| R | 13 | CRCW06035R60F | RESISTOR | 5.6 |
| R | 14 | CRCW120649R9F | RESISTOR | 49.9 |
| R | 15 | CRCW06036R34F | RESISTOR | 6.34 |
| R | 16 | OPEN | | |
| R | 17 | CRCW06032200F | RESISTOR | 220 |
| R | 18 | CRCW06031002F | RESISTOR | 10k |
| R | 19 | CRCW06034R70F | RESISTOR | 4.7 |
| R | 20 | SHORT (0 Ohms) | RESISTOR, 0 OHMS | 0 ohms |
| R | 21 | CRCW06031001F | RESISTOR | 1K |
| R | 22 | CRCW06032000F | RESISTOR | 200 |
| R | 23 | CRCW06031002F | RESISTOR | 10k |
| R | 24 | CRCW06031502F | RESISTOR | 15k |

| Item | | Part Number | Description | Value |
|---|---|---|---|---|
| R | 25 | CRCW06032492F | RESISTOR | 24.9k |
| R | 26 | CRCW060310R0F | RESISTOR | 10 |
| R | 27 | CRCW060310R0F | RESISTOR | 10 |
| R | 28 | CRCW06031001F | RESISTOR | 1k |
| R | 29 | CRCW06032002F | RESISTOR | 20.0k |
| R | 30 | CRCW06031002F | RESISTOR | 10.0k |
| R | 31 | CRCW06034990F | RESISTOR | 499 |
| R | 32 | OPEN | | |
| R | 33 | SHORT (0 Ohms) | RESISTOR, 0 OHMS | 0 ohms |
| R | 34 | CRCW1218100JT | RESISTOR | 10, 1W |
| R | 35 | CRCW1218100JT | RESISTOR | 10, 1W |
| R | 36 | CRCW06031001F | RESISTOR | 1k |
| R | 37 | CRCW06033011F | RESISTOR | 3.01k |
| R | 38 | CRCW06034990F | RESISTOR | 499 |
| R | 39 | CRCW06034702F | RESISTOR | 47k |
| R | 40 | CRCW06034702F | RESISTOR | 47k |
| R | 41 | CRCW06034702F | RESISTOR | 47k |
| R | 42 | CRCW06031002F | RESISTOR | 10k |
| R | T1 | NTCG164BH103H | NTC, 10k @25°C, 1k@100°C, TDK | 10k |
| | | | | |
| T | 1 | HA4000-Al | POWER XFMR W/AUX, COILCRAFT | 12:2 |
| T | 2 | DA2319-ALB | Gate Drive, Coilcraft | |
| T | 3 | P8208T, Pulse | CURRENT XFR, PULSE ENG | 100:1 |
| | | | | |
| U | 1 | LM5027 | CONTROLLER, Texas Instruments | |
| U | 2 | PS2811-1M | OPTO-COUPLER, NEC | |
| U | 3 | LM8261 | OPAMP,Texas Instruments | |
| U | 4 | LM4040 | REFERENCE, Texas Instruments | |
| U | 5 | LM4041 | REFERENCE, Texas Instruments | |
| Z | 2 | MM5Z3V6 | DIODE, ZENER 3.6V | Fairchild |

## 17 Printed Circuit Layout

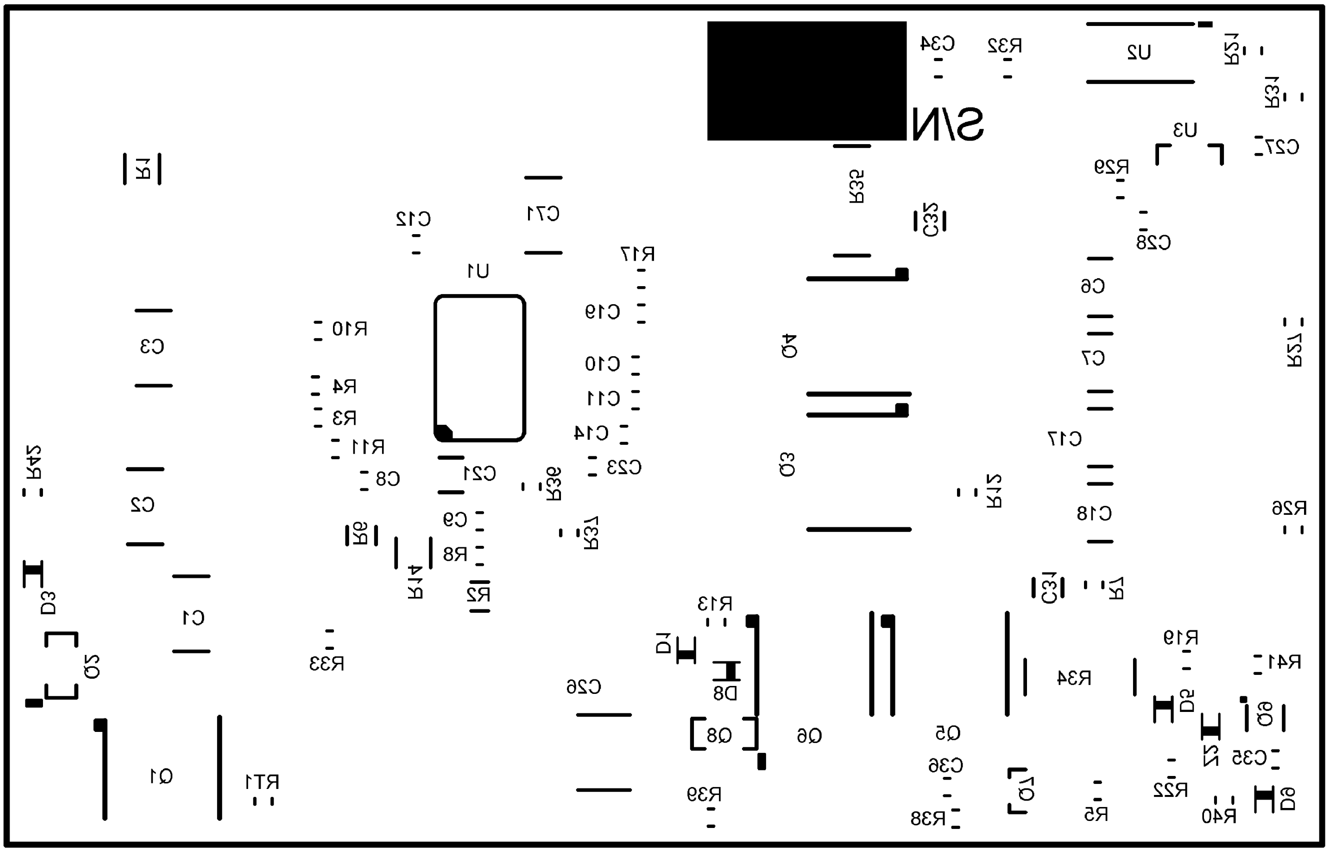


Figure 24. Bottom Assembly

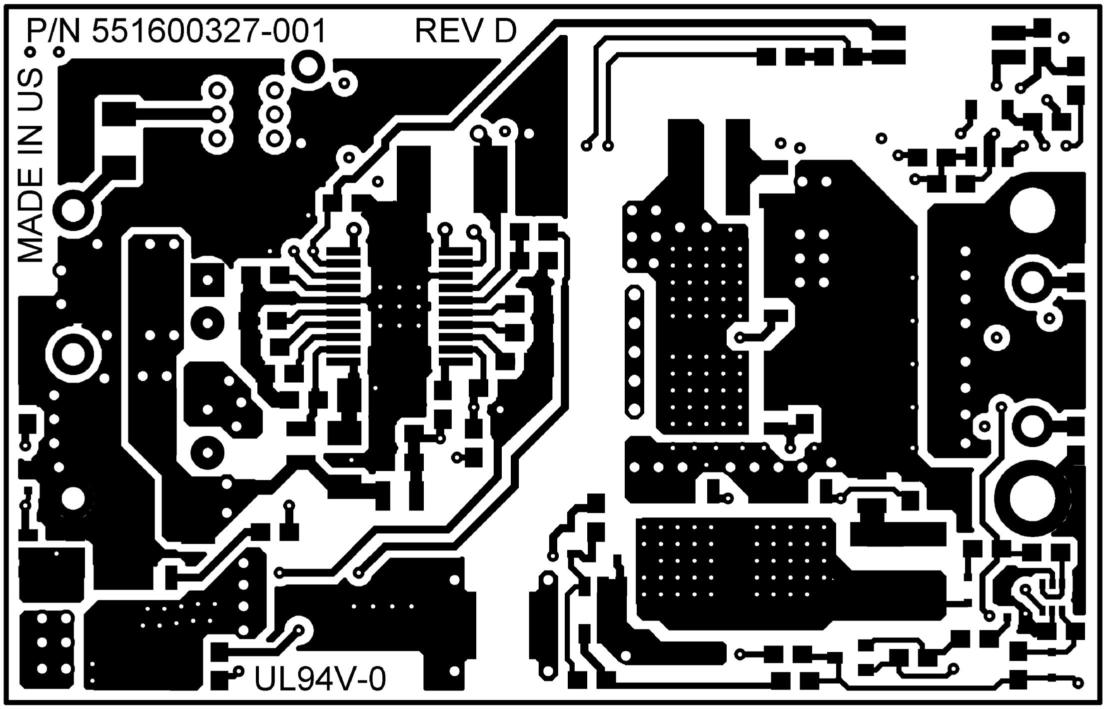


Figure 25. Bottom Layer

Figure 26. Bottom Silk Layer

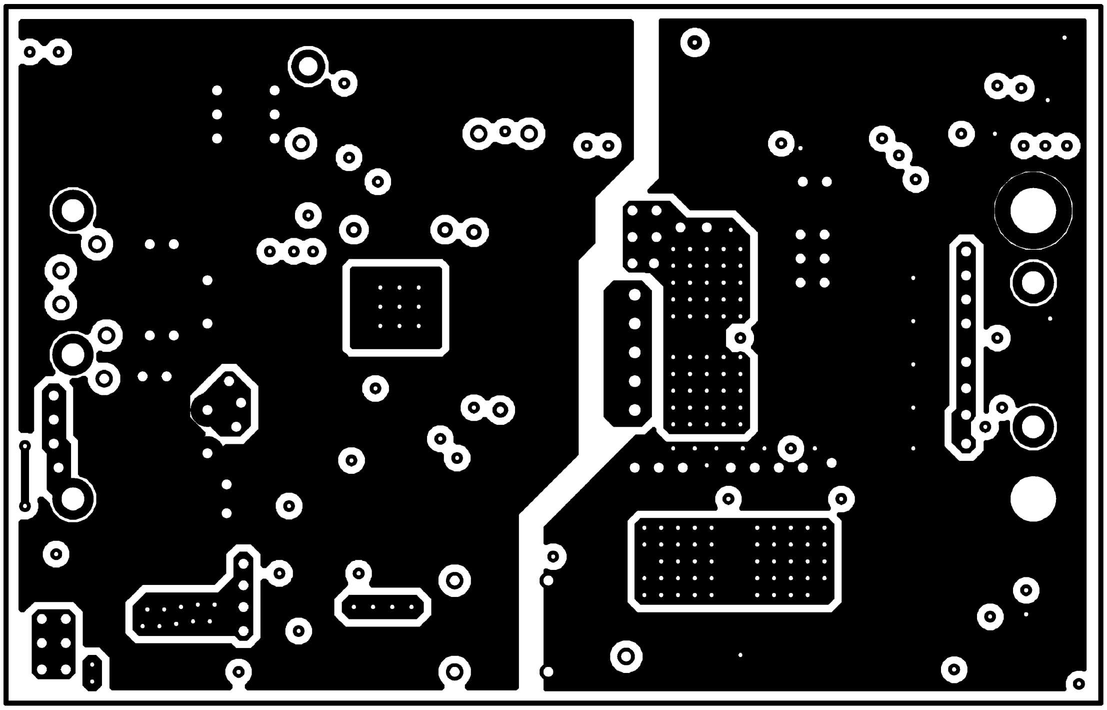


Figure 27. Mid 1 Layer

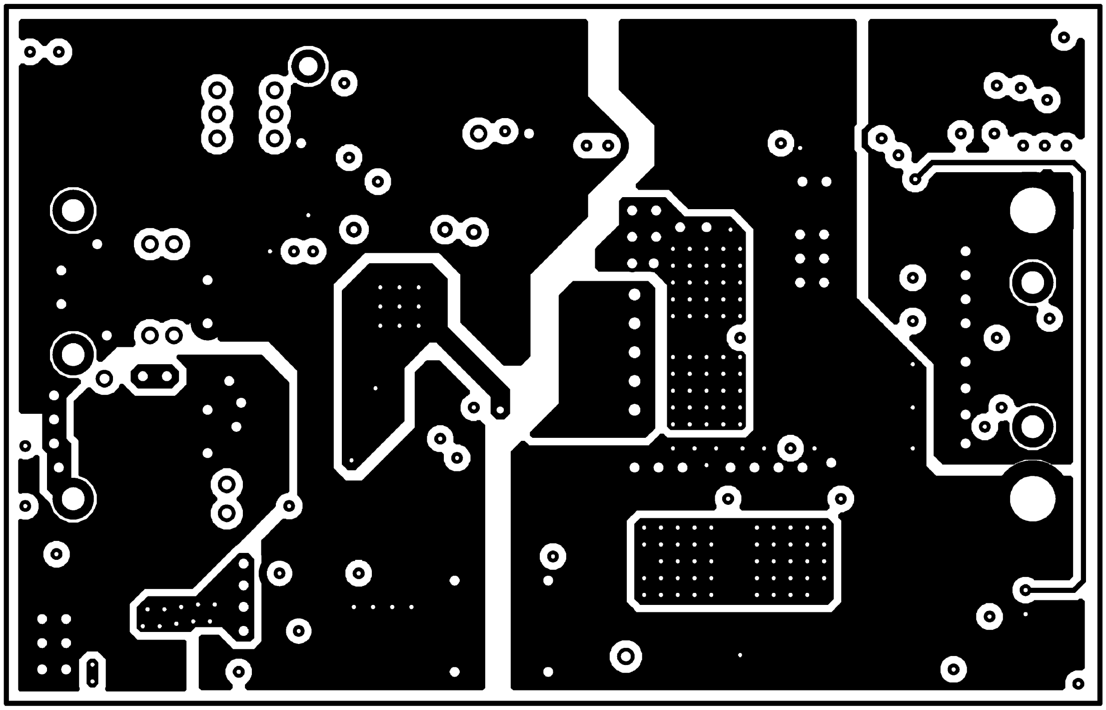


Figure 28. Mid 2 Layer

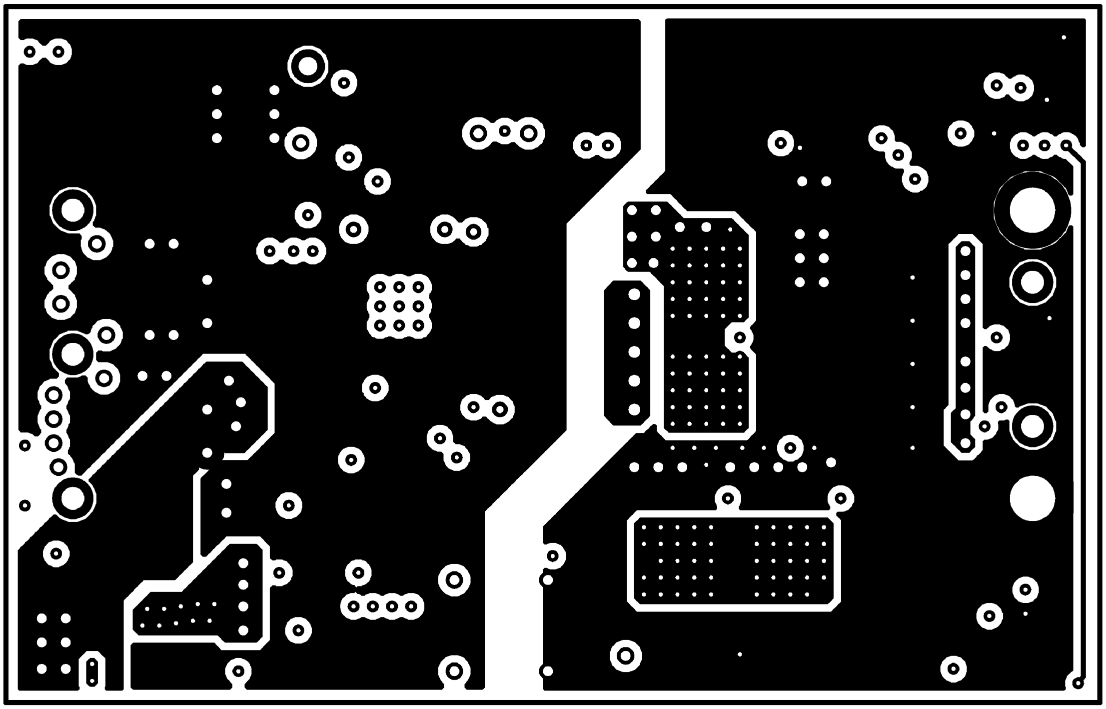


**Figure 29. Mid 3 Layer**

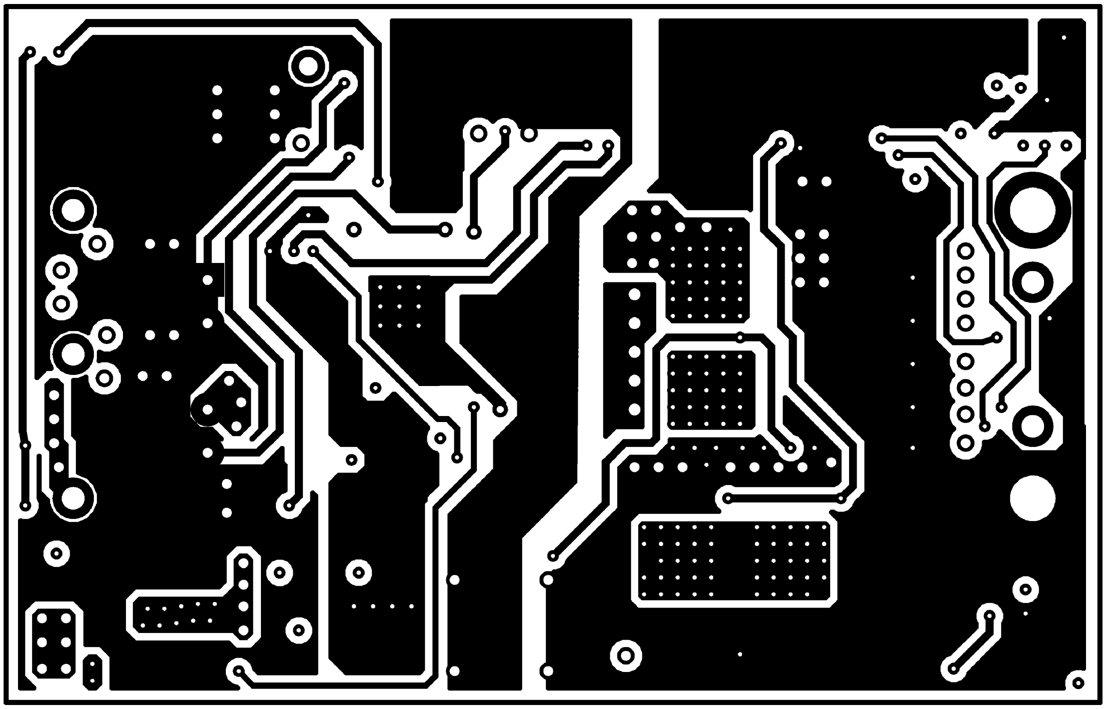


**Figure 30. Mid 4 Layer**

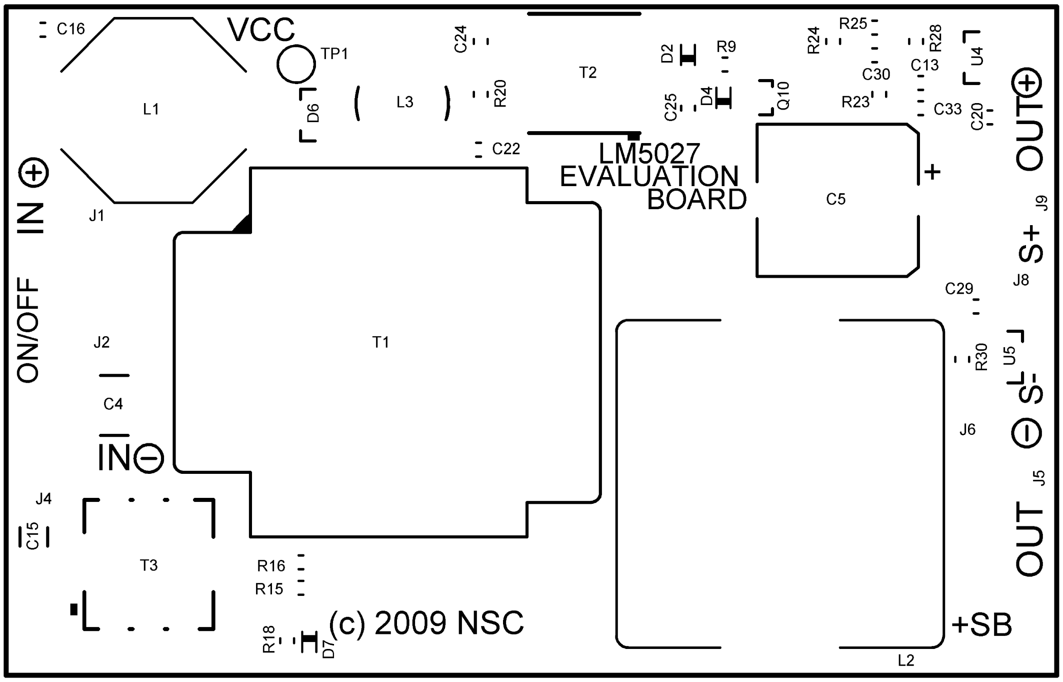


Figure 31. Top Assembly

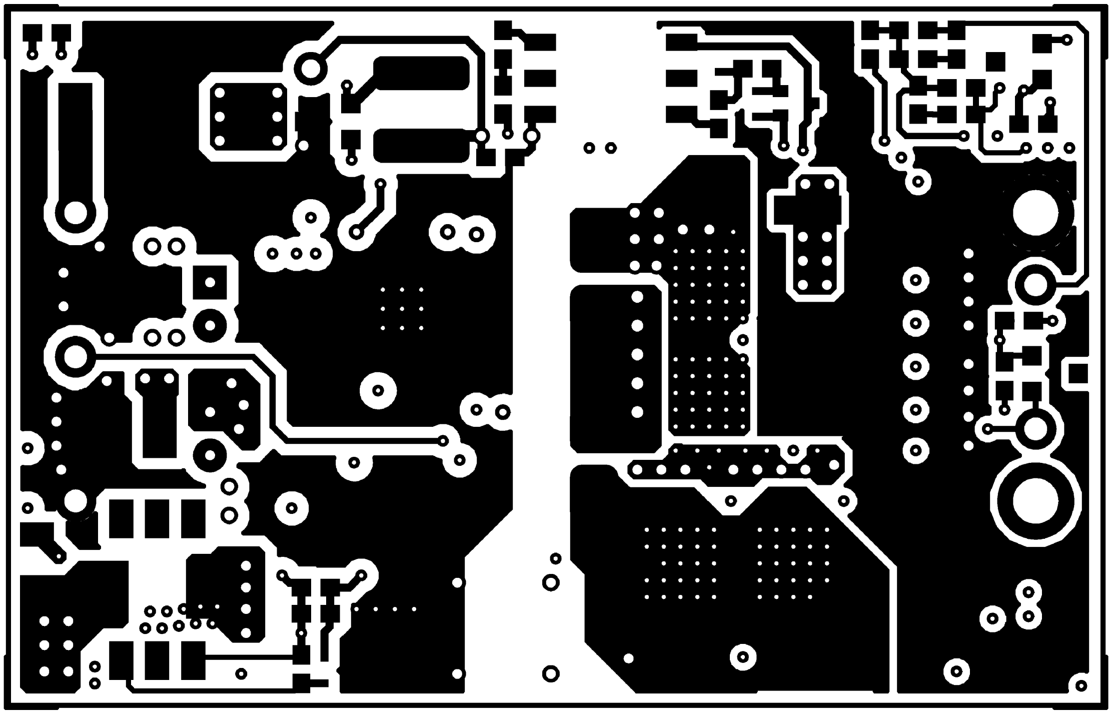


Figure 32. Top Layer

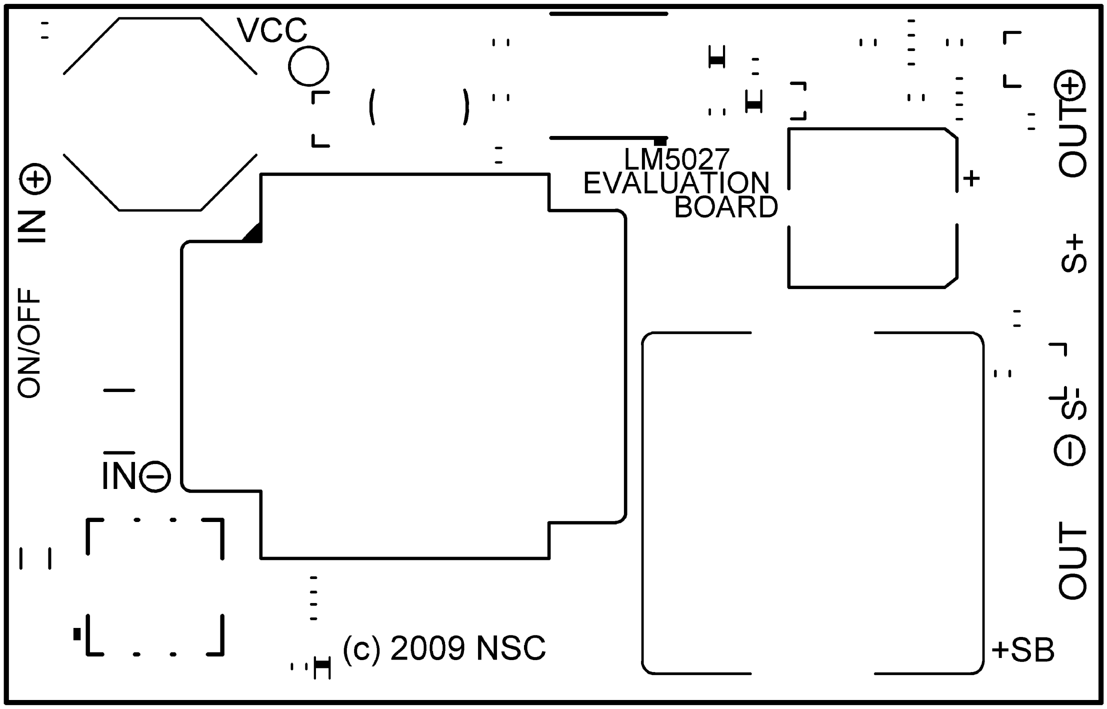


Figure 33. Top Silk Layer

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated