User's Guide

TPS54350 Step-Down Converter Evaluation Module User's Guide

TEXAS INSTRUMENTS

ABSTRACT

This user's guide describes the characteristics, operation, and the use of the TPS54350EVM−235 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and bill of materials are included.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments can cause interference with radio communications, in which case, the user at their own expense will be required to take whatever measures may be required to correct this interference.

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Table of Contents

1 Introduction

This chapter contains background information for the TPS54350 with support documentation for the TPS54350EVM-235 evaluation module (SLVP235). This user's guide contains the TPS54350EVM-235 performance specifications, schematic, and bill of material for the TPS54350EVM-235.

1.1 Background

The TPS54350 DC/DC converter is designed to provide up to 3-A output from a nominal 12-V (6-V to 18-V) input voltage source. Table 1-1 provides the rated input voltage and output current range. This evaluation module is designed to demonstrate the small PCB areas that can be achieved when designing with the TPS54350 regulator and does not reflect the high efficiencies that can be achieved when designing with this part. The switching frequency is set at a nominal 500 kHz, allowing the use of a relatively small footprint 10-mH output inductor. The high-side MOSFET is incorporated inside the TPS54350 package along with gate drive circuitry for an external synchronous FET. The low drain-to-source on resistance of the MOSFET allows the TPS54350 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. The TPS54350 is a full-featured device including:

- Programmable undervoltage lockout
- Bidirectional synchronization
- Adjustable switching frequency
- Enable and power good functions

Table 1-1. Input Voltage and Current Summary

EVM	INPUT VOLTAGE RANGE[1]	OUTPUT CURRENT RANGE
TPS54350EVM−235	6 V to 18 V	0 A to 3 A

(1)   Operation assured to 4.0 V after initial start-up.

1.2 Performance Specification Summary

A summary of the TPS54350EVM-235 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The ambient temperature is 250°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54350 is 4.5 V to 20 V. The EVM operates over this range but is designed and tested for 6-V to 18-V input range (12-V nominal).

Table 1-2. TPS54350EVM-235 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range			8.0	12.0	18	V
Output voltage set point				3.3		V
Output current range		V_I = 3 V to 5.5 V	0		3	A
Line regulation		I_O = 0–3 A, V_I = 6 V to 18 V		±1%		
Load regulation		V_I = 12 V, I_O = 0 A to 3 A		±0.05%		
Load transient	Voltage change	I_O = 0.75 A to 2.25 A		−10		mV_{PK}
	Recovery time			60		µs
	Voltage range	I_O = 2.25 A to 0.75 A		11		mV_{PK}
	Recovery time			60		µs
Loop bandwidth		V_I = 6 V		28		kHz
Phase margin		V_I = 6 V		70		°
Loop bandwidth		V_I = 18 V		32		kHz
Phase margin		V_I = 18 V		60		°
Input ripple voltage				400		mV_{PP}
Output ripple voltage				40		mV_{PP}
Output rise time				2.8		ms
Operating frequency				500		kHz

Table 1-2. TPS54350EVM-235 Performance Specification Summary (continued)

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum efficiency	V_I = 6.0 V, V_O = 3.3 V, I_O = 1.0 A		87%		

1.3 Modifications

The TPS54350EVM−235 is designed to demonstrate the small size that can be attained when designing with the TPS54350, so many of the features, which allow for extensive modifications, have been omitted from this EVM.

1.3.1 Output Voltage Setpoint

Changing the value of R2 can change the output voltage in the range of 0.9 V to 5 V. The value of R2 for a specific output voltage can be calculated by using Equation 1. Table 1-3 list the values for R2 for some common output voltages.

Table 1-3. Output Voltage Programming

OUTPUT VOLTAGE (V)	R_2 VALUE (Ω)
1.2	2.87 k
1.5	1.47 k
1.8	976
2.5	549
3.3	374
5.0	221

$$R_2 = 1\ k\Omega\ \times\ \frac{0.891\ V}{V_O - 0.891\ V} \tag{1}$$

The minimum output voltage is limited by the minimum controllable on time of the device, 125 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 2:

$$V_{O(min)} = 125\ nsec \times \textit{f}s \times V_{I(max)} \tag{2}$$

1.3.2 Switching Frequency

The switching frequency can be trimmed to any value between 250 kHz and 700 kHz by changing the value of R4. The switching frequency can also be set to pre-programmed values of 250 kHz by shorting the RT pin to AGND, or 500 kHz by floating the RT pin. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased.

1.3.3 Input Filter

An on-board electrolytic input capacitor can be added at C1.

1.3.4 UVLO Programming

The TPS54350 is provided with an internal voltage divider from VIN to AGND. These start and stop thresholds are given in Table 1-4.

Table 1-4. Internal UVLO Setting

	START VOLTAGE THRESHOLD	STOP VOLTAGE THRESHOLD
VIN	4.4 V	3.7 V
UVLO	1.18 V	1.09 V

To set a different set of thresholds, R6 and R7 can be selected using Equation 3 and Equation 4.

$$R6 = \frac{V_{I(start)} \times R7}{UVLO(start)} - R7 \tag{3}$$

$$R6 = \frac{V_{I(stop)} \times R7}{UVLO(stop)} - R7 \tag{4}$$

1.3.5 Synchronization

The SYNC pin can be configured as an input or as an output, depending on the configuration of the RT pin. If the RT pin is open or tied to AGND, the SYNC pin functions as an output. When operating as an output, the falling edge of the signal is one half of the switching cycle and approximately 180° out of phase with the rising edge of the PH pins. Thus, two TPS54350 devices operating in a system can share an input capacitor and draw ripple current at twice the frequency of a single unit.

If the RT pin is programmed with a resistor to AGND, the SYNC pin functions as an input. When operating as an input, the SYNC pin is a falling-edge triggered signal, and the resistor at the RT pin should be set to provide a frequency equal to 90 percent of the SYNC input frequency.

1.3.6 Power Good

An internal circuit monitors the VSENSE input voltage to verify that it is within a guard band around the reference voltage. If these voltages are close to each other in value, and no other fault signals are present, the PWRGD pin presents a high impedance. A low on the PWRGD pin indicates a fault. The PWRGD pin has been designed to provide a weak pulldown and indicates a fault even when the device is unpowered. If the TPS54350 has power and has any fault flag set, the TPS54350 indicates the power is not good by driving the PWRGD pin low. The following events, alone or in combination, indicates power not good:

- VSENSE pin out of bounds
- Overcurrent
- Thermal shutdown
- UVLO undervoltage
- Input voltage not present (weak pulldown)
- Slow starting
- VBIAS voltage is low

The evaluation module provides an external pullup resistor of 10 kW (R8), a test point TP1 that can be tied to an external 3.3-V or 5-V source, and a test point TP2 to monitor the power-good signal.

1.3.7 Synchronous Low-Side FET

The TPS54350EVM-235 is provisioned with a external low-side FET for operation as a synchronous buck regulator. If desired, an external catch diode can be used in place of the FET. The pad for the diode is located on the back side of the PCB. Verify that the inductor is properly sized for operation without the low-side FET. The minimum value for the inductor when operating in this mode is given by Equation 5.

$$L(\text{min}) = \frac{V_O\left(1 - \frac{V_O}{V_{I(max)}}\right)}{fs \times 0.6} \tag{5}$$

1.3.8 Optional Output Filtering

Optional pads are included on the EVM for additional output filter capacitors. One D4 location (C12) and one 0805 location (C5) are provided.

2 Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54350EVM−235 evaluation module. The section also includes test results typical for the TPS54350EVM−235 and covers the following:

- Efficiency
- Output voltage regulation
- Load transients
- Loop response
- Output ripple
- Input ripple
- Start-up

2.1 Input/Output Connections

The TPS54350EVM−235 has the following two input/output connectors: VI(J1) and VO (J3). A diagram showing the connection points is shown in Figure 2-1. A power supply capable of supplying 5 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 20 AWG wires. The maximum load current capability should be 3 A. Wire lengths should be minimized to reduce losses in the wires. Test point TP9 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54350 is intended to be used as a point of load regulator. In typical applications, it is usually located close to the input voltage source. When using the TPS54350EVM−235 with an external power supply as the source for VI, an additional bulk capacitor can be required, depending on the output impedance of the source and length of the hook-up wires. The test results presented are obtained using a 47-mF, 25-V additional input capacitor. Alternately, C1 can be populated with an input filter capacitor.
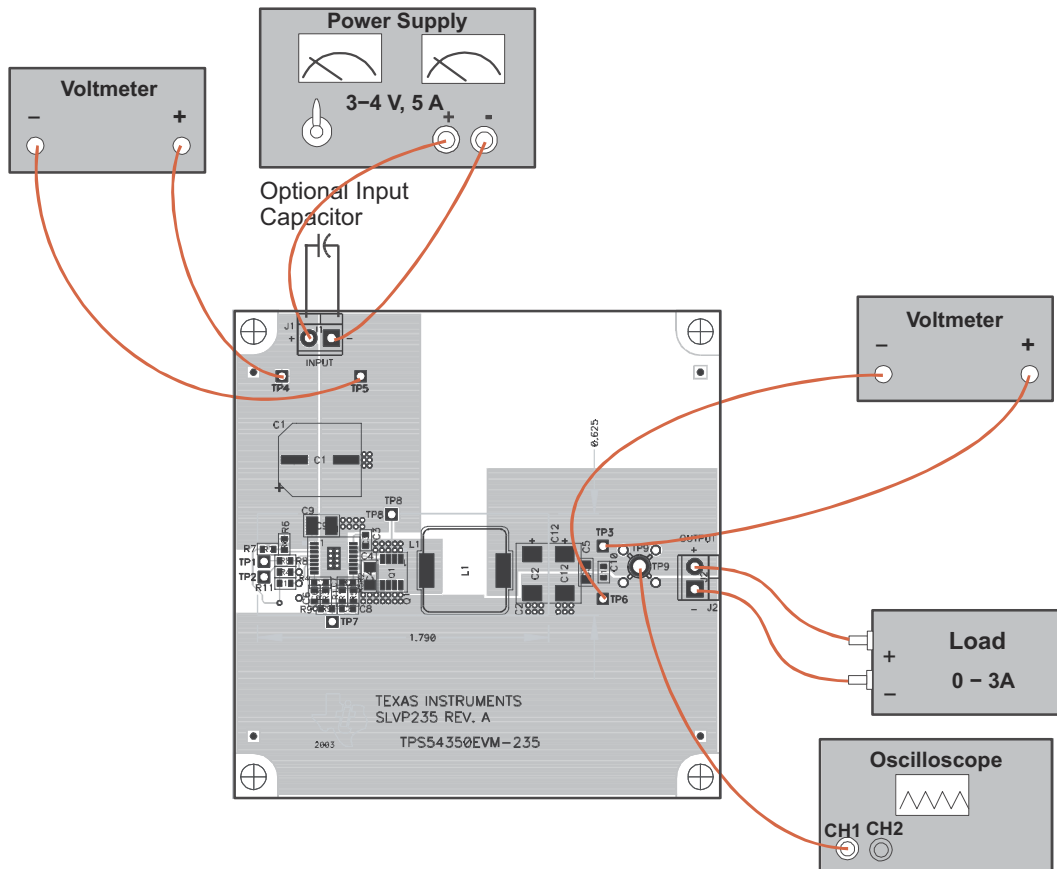

Figure 2-1. Connection Diagram

2.2 Efficiency

The TPS54350EVM−235 efficiency peaks at load current of approximately 1 A and V_I of 6 V, and then decreases as the load current increases towards full load. For higher input voltages, quiescent losses are greater and the efficiency peaks under full load conditions. It is important to consider that this design is optimized for small size and flexibility and does not reflect the high efficiencies that are possible for specific applications using the TPS54350. Figure 2-2 shows the efficiency for the TPS54350 at an ambient temperature of 250°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 500 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.
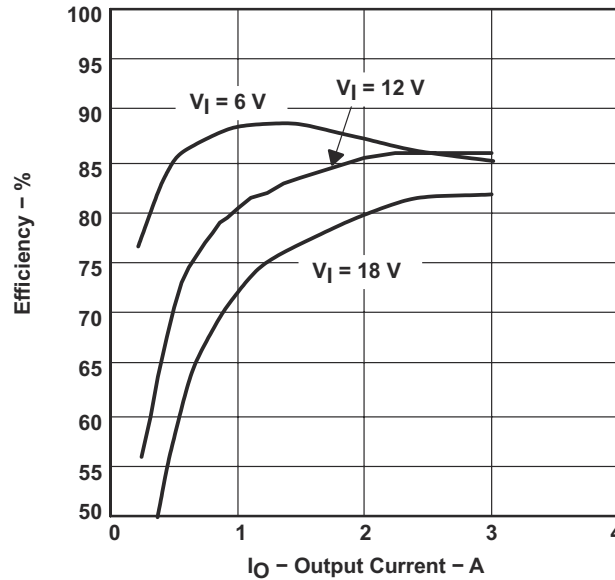
Figure 2-2. Measured Efficiency

2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54350EVM−235 EVMs to output full-rated load current while maintaining safe junction temperatures. With a 12-V input source and a load approaching the current limit of 4.2 A, the junction temperature is approximately 47°C. The total circuit losses at 25°C are shown in Figure 2-3. Power dissipation is shown for input voltages of 6 V, 12 V, and 18 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.
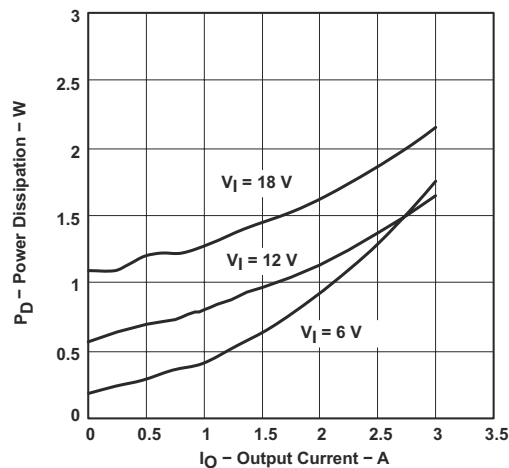

Figure 2-3. Measured Circuit Losses

2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54350EVM−235 is shown in Figure 2-4, while the output voltage line regulation is shown in Figure 2-5. Measurements are given for an ambient temperature of 25°C.
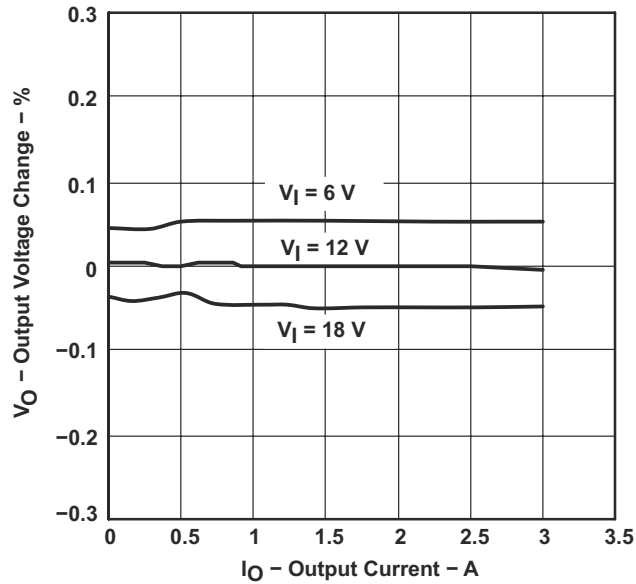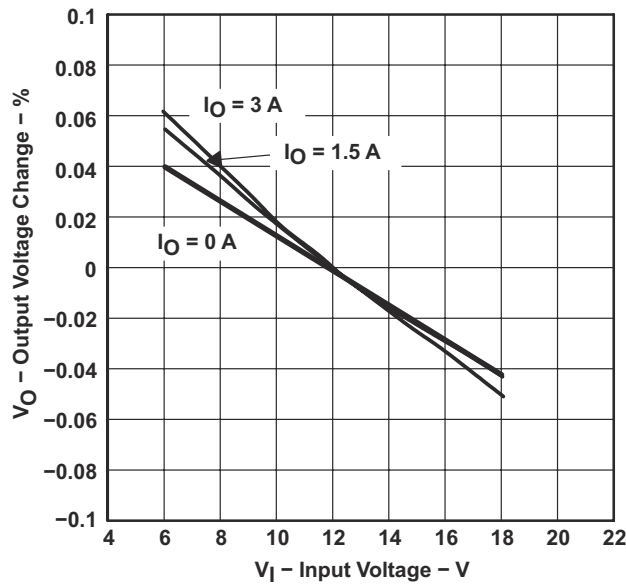

Figure 2-4. Load Regulation

Figure 2-5. Line Regulation

2.5 Load Transients

The TPS54350EVM−235 response to load transients is shown in Figure 2-6. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.
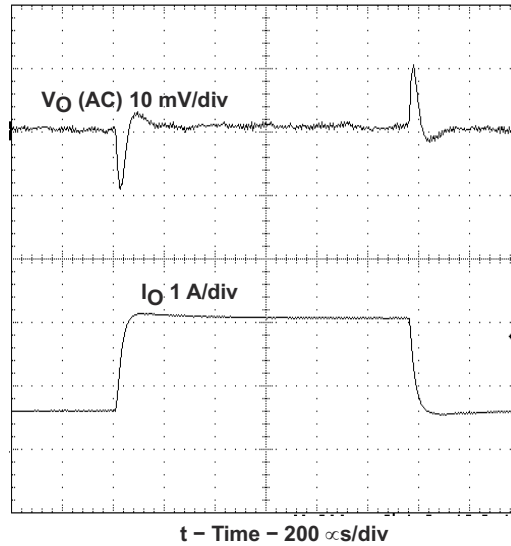

Figure 2-6. Load Transient Response, TPS54350

2.6 Loop Characteristic

The TPS54350EVM−235 loop response characteristics are shown in Figure 2-7 and Figure 2-8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.
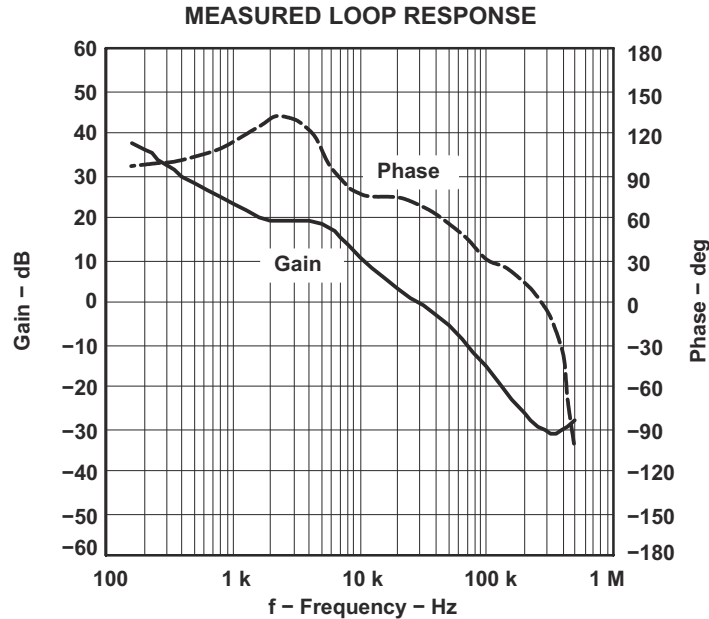

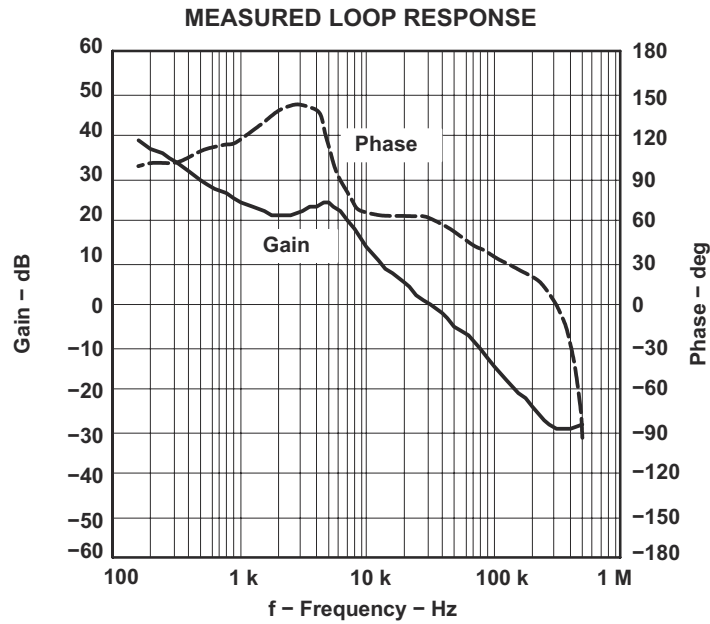**Figure 2-7. Measured Loop Response, TPS54350, V_I = 6 V**

MEASURED LOOP RESPONSE

Figure 2-8. Measured Loop Response, TPS54350, V_I = 18 V

2.7 Output Voltage Ripple

The TPS54350EVM−235 output voltage ripple is shown in Figure 2-9. The input voltage is 3.3 V for the TPS54350. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.
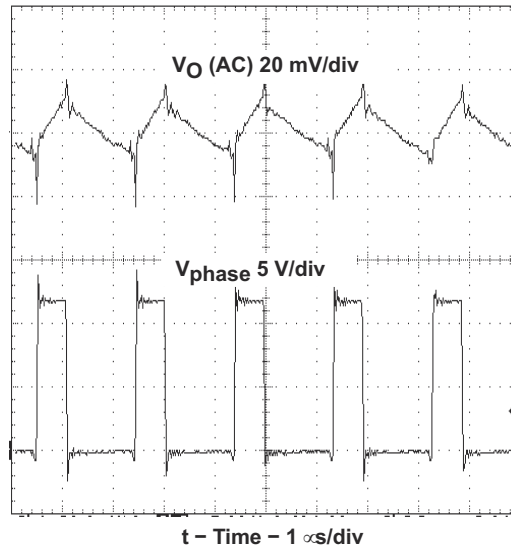

Figure 2-9. Measured Output Voltage Ripple, TPS54350

2.8 Input Voltage Ripple

The TPS54350EVM−235 output voltage ripple is shown in Figure 2-10. The input voltage is 3.3 V for the TPS54350. Output current for each device is rated full load of 3 A.
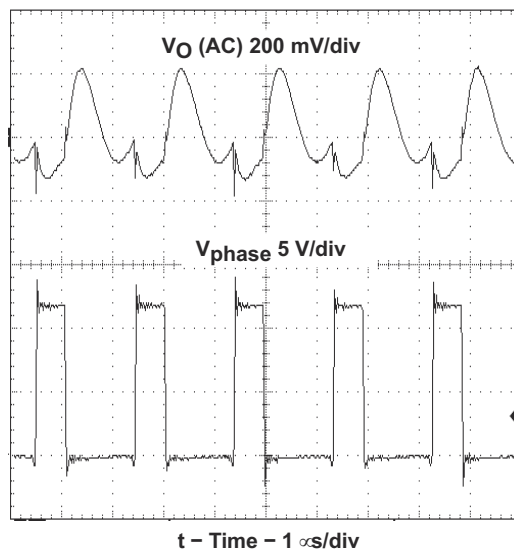
V_O (AC) 200 mV/div

V_{phase} 5 V/div

t − Time − 1 ∝s/div

Figure 2-10. Input Voltage Ripple, TPS54350

2.9 Gate Drive

The TPS54350 provides the gate drive signal for a synchronous low-side FET. This gate drive signal and its relationship to the PHASE signal is shown in Figure 2-11.
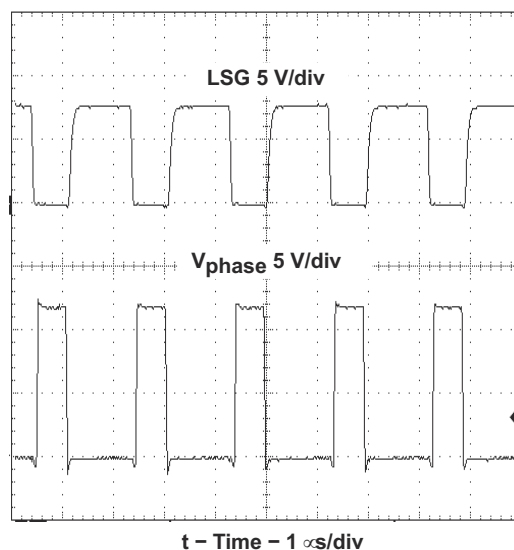
LSG 5 V/div

V_{phase} 5 V/div

t − Time − 1 ∝s/div

Figure 2-11. Gate Drive Signal, TPS54350

2.10 Powering Up and Down

The start-up voltage waveform of the TPS54350EVM−235 is shown in Figure 2-12. The waveform shows the nominal 12-V input voltage in Ch. 1, the 3.3-V output ramping up in Ch. 2, and the PWRGD signal in Ch. 3. Note that the PWRGD signal is pulled up externally to 3.3 V.
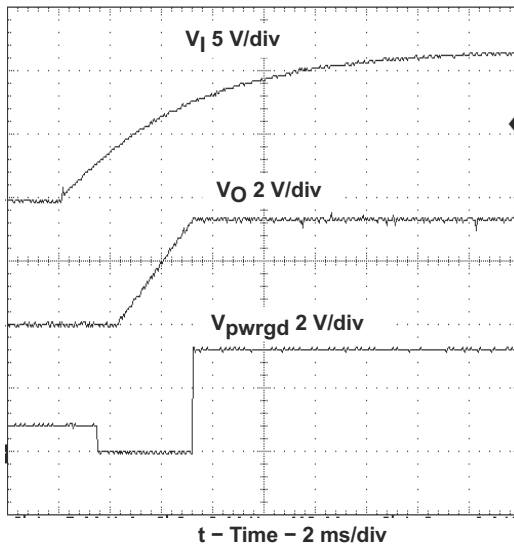

V$_I$ 5 V/div

V$_O$ 2 V/div

V$_{pwrgd}$ 2 V/div

t − Time − 2 ms/div

Figure 2-12. Powering Up

The corresponding power-down waveform is shown in Figure 2-13. The channel assignments are the same as in the power-up waveform in Figure 2-12.
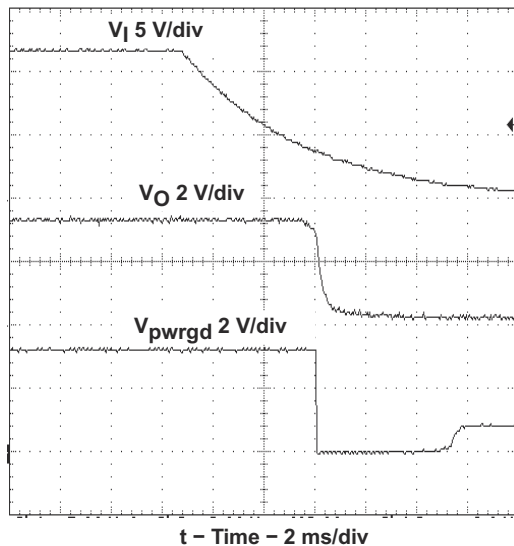

V$_I$ 5 V/div

V$_O$ 2 V/div

V$_{pwrgd}$ 2 V/div

t − Time − 2 ms/div

Figure 2-13. Powering Down

3 Board Layout

This section provides a description of the TPS54350EVM−235 board layout and layer illustrations.

3.1 Layout

Theboard layout for the TPS54350EVM−235 is shown in Figure 3−1 through Figure 3−4. The topside layer of the TPS54350EVM−235 is laid out in a manner typical of a user application that is optimized for small size. The top and bottom layers are 1.5 oz. copper.

The top layer contains the main power traces for VI, VO, and Vphase. Also, on thetop layer are connections for the remaining pins of the TPS54350 and a large area filled with ground. The bottom layer consists of a ground plane along with aVphase area and the Vsense trace. The bottom layer also has pads for placing snubber components (R10 and C11) and an optional catch diode (D1). The top and bottom ground traces are connected with multiple vias placed around the board including 8 directly under the TPS54350 device to provide a thermal path from the PowerPADä landto ground.

The input decoupling capacitor (C9), bias decoupling capacitor (C4), andbootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, at the positive output connection.
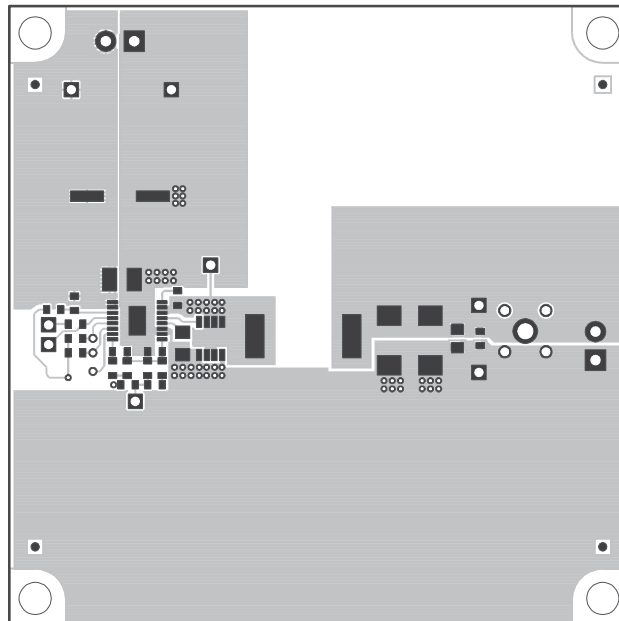

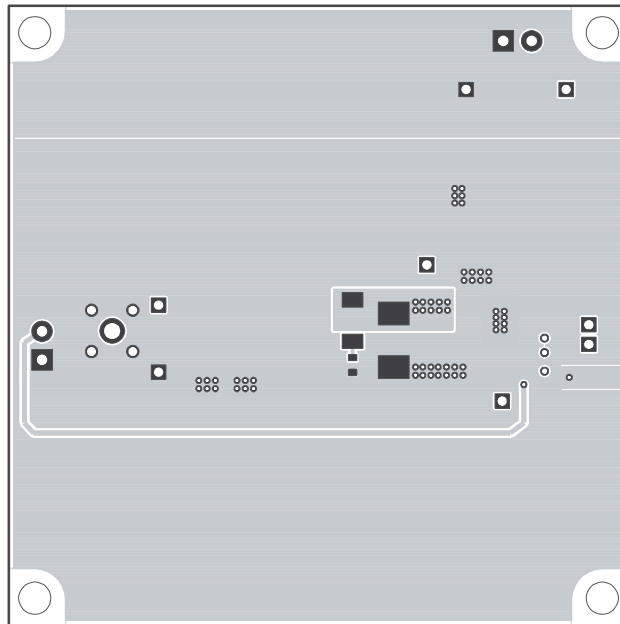**Figure 3-1. Top Side Layout**

Figure 3-2. Bottom Side Layout
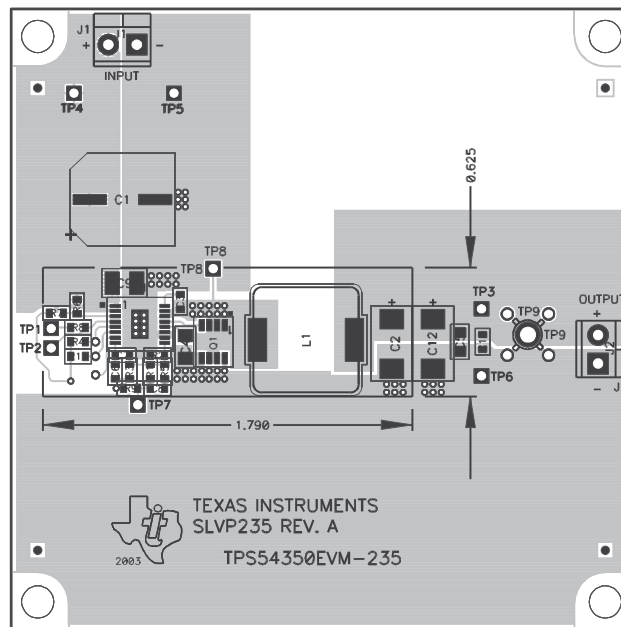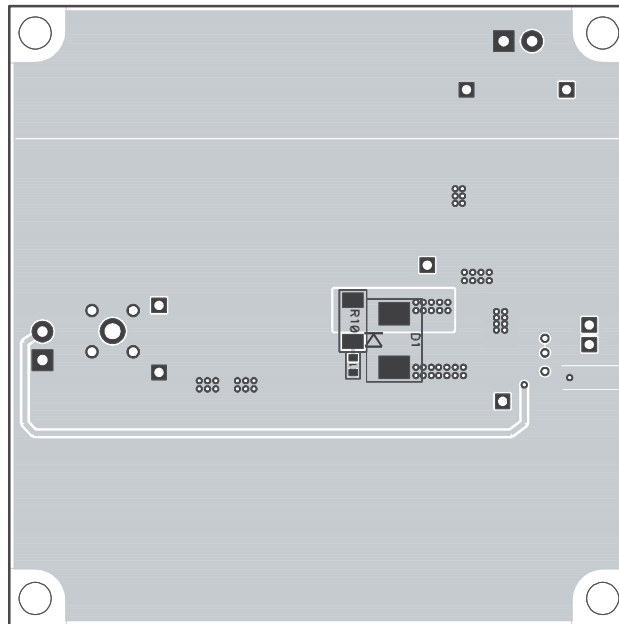

Figure 3-3. Top Side Assmebly

Figure 3-4. Bottom Side Assmebly

4 Schematic and Bill of Materials

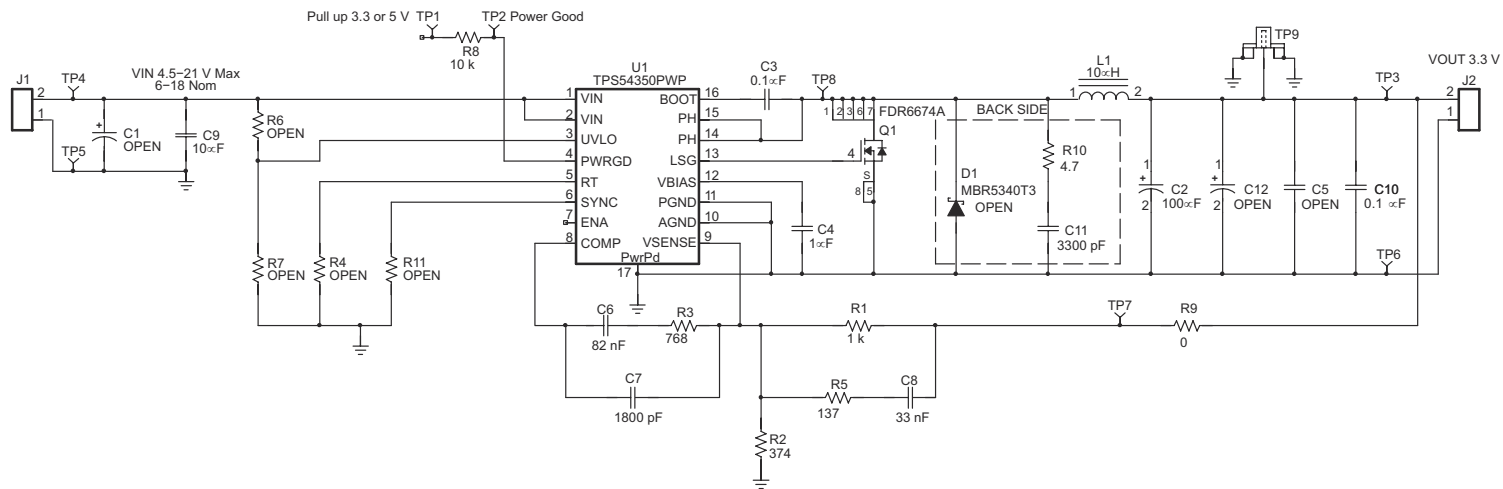The TPS54350EVM−235 schematic and bill of materials are presented in this section.

Figure 4-1. TPS54350EVM-235 Schematic

4.1 Bill of Materials

The bill of materials for the TPS54350EVM—235 is provided in Table 4-1.

Table 4-1. Bill of Materials

Count	RefDes	Description	Size	MFR	PartNumber
—	C1	Capacitor,aluminum, 100 mF, 35 V, 20%, FC Series	0.335x 0.374	Panasonic	EEVFC1V101P
1	C11	Capacitor,ceramic, 3300 pF, 50 V, X7R, 10%	603	std	std
—	C12	Capacitor, aluminum, xxx mF, × V, 20% (UE Series)	7343	std	std
—	C5	Capacitor,ceramic, xxx mF,vv V, [temp], [tol]	805	std	std
1	C2	Capacitor, POSCAP, 100 mF, 6.3 V, 45 mW, 20%	7343(D)	Sanyo	6TPC100M
2	C3,C10	Capacitor,ceramic, 0.1 mF,16 V, X7R, 10%	603	std	std
1	C4	Capacitor,ceramic, 1.0 mF,16 V, X7R, 10%	1206	std	std
1	C6	Capacitor,ceramic, 82 nF, 16 V, X7R, 10%	603	std	std
1	C7	Capacitor,ceramic, 1800 pF, 50 V, X7R, 10%	603	std	std
1	C8	Capacitor,ceramic, 33 nF, 50 V, X7R, 10%	603	std	std
1	C9	Capacitor,ceramic, 10 mF,25 V, X5R, 20%	1210	Taiyo Yuden	TMK325BJ106MN
—	D1	Diode,schottky, 3 A, 40 V	SMC	Motorola	MBRS340T3
2	J1,J2	Terminal block, 2 pin, 6 A, 3.5 mm	75525	OST	ED1514
1	L1	Inductor,SMT, 10 mH, 8 A, 20 mW	0.51 × 0.51	Vishay	IHLP—5050CZ
1	Q1	Transistor,MOSFET, Nch, 11.5 A, 30 V, 9.5 mW	0.160 × 0.130	Fairchild	FDR6674A
1	R1	Resistor,chip, 1.00 kW,1/16 W, 1%	603	std	std
1	R10	Resistor,chip, 4.7 W,1/2 W, 5%	2010	std	std
1	R2	Resistor,chip, 374 W,1/16 W, 1%	603	std	std
1	R3	Resistor,chip, 768 W,1/16 W, 1%	603	std	std
—	R4, R6,R7, R11	Resistor,chip, xx W,1/16 W, 1%	603	std	std
1	R5	Resistor,chip, 137 W,1/16 W, 1%	603	std	std
1	R8	Resistor,chip, 10.0 kW,1/16 W, 1%	603	std	std
1	R9	Resistor,chip, 0 W,1/16 W, 1%	603	std	std
4	TP1, TP3, TP4,TP8	Testpoint, red, 1 mm	0.038	Farnell	240–345
4	TP2, TP5, TP6,TP7	Testpoint, black, 1 mm	0.038	Farnell	240–333
1	TP9	Adaptor,3.5 mm probe clip (or 131–5031–00)	0.2	Tektronix	131–4244–00
1	U1	IC,dc/dc converter	PWP16	TI	TPS54350PWP
1	——	PCB,3 inch × 3 inch × 0.062 inch		Any	SLVP235

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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    1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

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    2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

    2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

    2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:
EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3   *Regulatory Notices:*

   3.1   *United States*

      3.1.1   *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2   *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

      FCC Interference Statement for Class B EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

      - *Reorient or relocate the receiving antenna.*
      - *Increase the separation between the equipment and receiver.*
      - *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
      - *Consult the dealer or an experienced radio/TV technician for help.*

   3.2   *Canada*

      3.2.1   *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

      Concerning EVMs Including Radio Transmitters:

      This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

      (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

      Concernant les EVMs avec appareils radio:

      Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

      Concerning EVMs Including Detachable Antennas:

      Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの

措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4   *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5.   *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6.   *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7.   *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

    8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

    8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

IMPORTANT NOTICE AND DISCLAIMER