CAV24C02, CAV24C04, CAV24C08, CAV24C16

EEPROM Serial 2/4/8/16-Kb I²C - Automotive Grade 1

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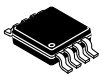


TSSOP−8
Y SUFFIX
CASE 948AL

WLCSP−4*
C4A SUFFIX
CASE 567DC

SOIC−8
W SUFFIX
CASE 751BD

WLCSP−5*
C5A SUFFIX
CASE 567DD

Description

The CAV24C02/04/08/16 are a EEPROM Serial 2/4/8/16−Kb I²C devices organized internally as 16/32/64 and 128 pages respectively of 16 bytes each. All devices support both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non−volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight CAV24C02, four CAV24C04, two CAV24C08 and one CAV24C16 device on the same bus.

Features

- Automotive AEC−Q100 Grade 1 (−40°C to +125°C) Qualified
- Supports Standard and Fast I²C Protocol
- 2.5 V to 5.5 V Supply Voltage Range
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- CAV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

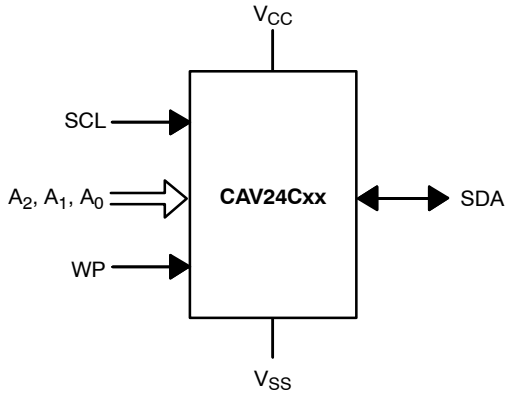
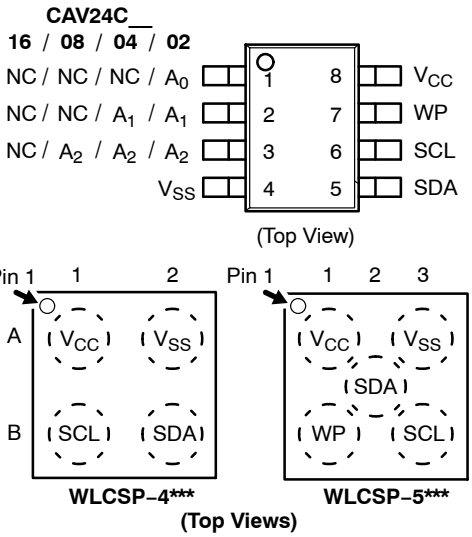


Figure 1. Functional Symbol

PIN CONFIGURATIONS

SOIC (W), TSSOP (Y)



PIN FUNCTION

Pin Name	Function
A0, A1, A2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connect

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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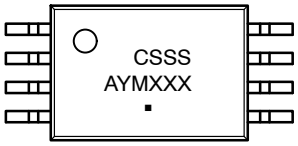
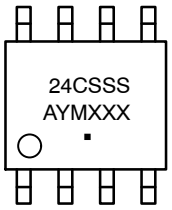
DEVICE MARKINGS

(TSSOP−8)



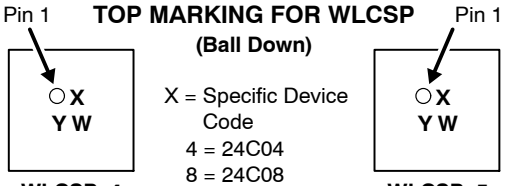
CSSS = Specific Device Code, where
SSS = 02H for CAV24C02
SSS = 04K for CAV24C04
SSS = 08K for CAV24C08
SSS = 16K for CAV24C16
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb−Free Package

(SOIC−8)



24CSSS = Specific Device Code, where
SSS = 02H for CAV24C02
SSS = 04K for CAV24C04
SSS = 08K for CAV24C08
SSS = 16K for CAV24C16
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb−Free Package

TOP MARKING FOR WLCSP
(Ball Down)



Y = Production Year Code
W = Production Workweek Code

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During input transitions, voltage undershoot on any pin should not exceed −1 V for more than 20 ns. Voltage overshoot on pins A_0, A_1, A_2 and WP should not exceed V_{CC} + 1 V for more than 20 ns, while voltage on the I^2C bus pins, SCL and SDA, should not exceed the absolute maximum ratings, irrespective of V_{CC}.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS
(V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz			1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz			2	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +125°C		5	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μA
V_{IL}	Input Low Voltage			−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A_0, A_1, A_2 and WP		0.7 x V_{CC}	V_{CC} + 0.5	V
		SCL and SDA		0.7 x V_{CC}	5.5	V
V_{OL}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3 mA			0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PIN IMPEDANCE CHARACTERISTICS (V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA Pin Capacitance	V_{IN} = 0 V, f = 1.0 MHz, V_{CC} = 5.0 V	8	pF
	Other Pins		6	pF
I_{WP} (Note 5)	WP Input Current	V_{IN} < V_{IH}, V_{CC} = 5.5 V	130	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	120	
		V_{IN} < V_{IH}, V_{CC} = 2.5 V	80	
		V_{IN} > V_{IH}	2	
I_A (Note 5)	Address Input Current (A0, A1, A2)	V_{IN} < V_{IH}, V_{CC} = 5.5 V	50	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	35	
		V_{IN} < V_{IH}, V_{CC} = 2.5 V	25	
		V_{IN} > V_{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (Note 6) (V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		100		ns
T_i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		0.1		0.1	ms

6. Test conditions according to “AC Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Drive Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Time	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Level	0.5 x V_{CC}
Output Test Load	Current Source I_{OL} = 3 mA; C_L = 100 pF

Power−On Reset (POR)

Each CAV24Cxx* incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAV24Cxx device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against ‘brown−out’ failure following a temporary loss of power.

**For common features, the CAV24C02/04/08/16 will be referred to as CAV24Cxx.*

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAV24Cxx supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAV24Cxx acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see AC Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is high. An SDA transition while SCL is high will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/W, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 3. A_2, A_1 and A_0 must match the state of the external address pins, and a_{10}, a_9 and a_8 are internal address bits.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

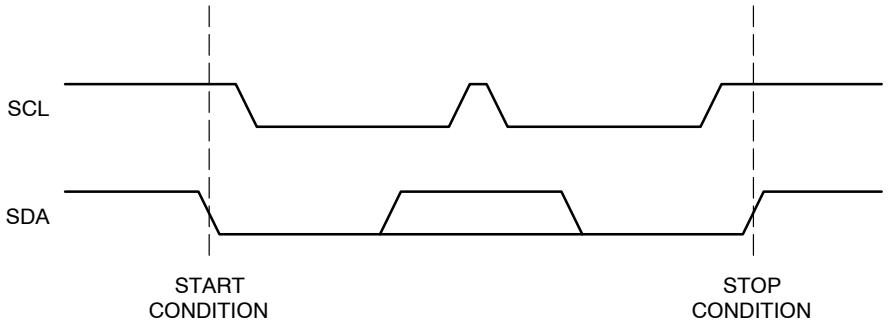


Figure 2. Start/Stop Timing

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$	CAV24C02
1	0	1	0	A_2	A_1	a_8	R/$\overline{W}$	CAV24C04
1	0	1	0	A_2	a_9	a_8	R/$\overline{W}$	CAV24C08
1	0	1	0	a_{10}	a_9	a_8	R/$\overline{W}$	CAV24C16

Figure 3. Slave Address Bits

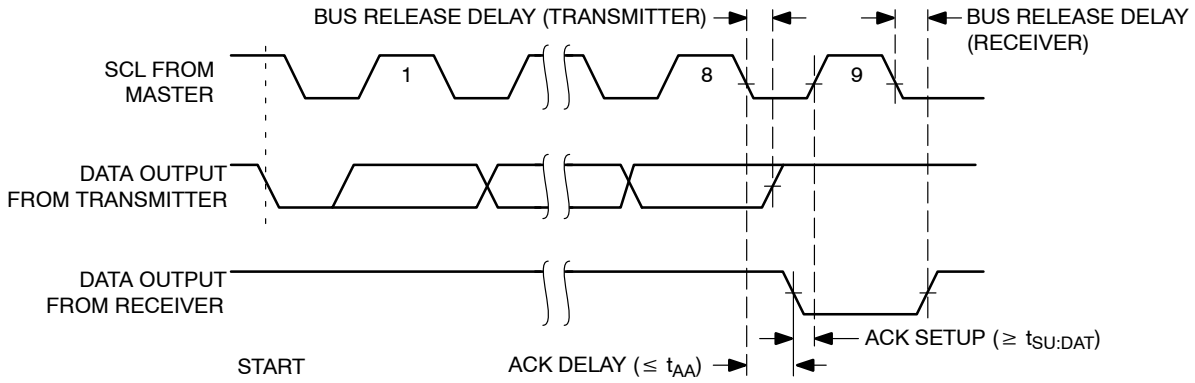


Figure 4. Acknowledge Timing

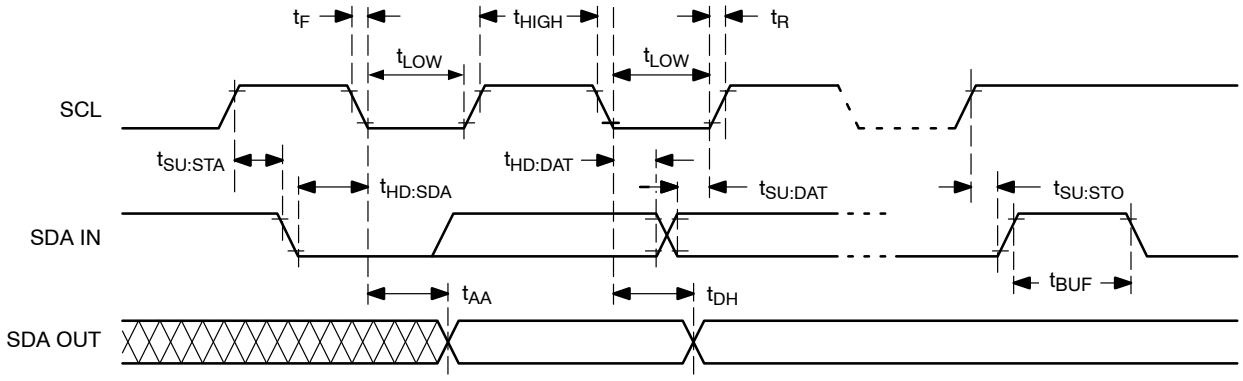


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/W bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAV24Cxx. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAV24Cxx device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress (t_{WR}), the SDA output will be tri−stated and the CAV24Cxx will not respond to any request from the Master device (Figure 7).

Page Write

The CAV24Cxx writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAV24Cxx will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter ‘wraps around’ to the beginning of page and previously transmitted data will be overwritten. Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAV24Cxx in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation, the CAV24Cxx initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAV24Cxx is still busy with the write operation, NoACK will be returned. If the CAV24Cxx has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAV24Cxx. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAV24Cxx will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAV24Cxx is shipped erased, i.e., all bytes are FFh.

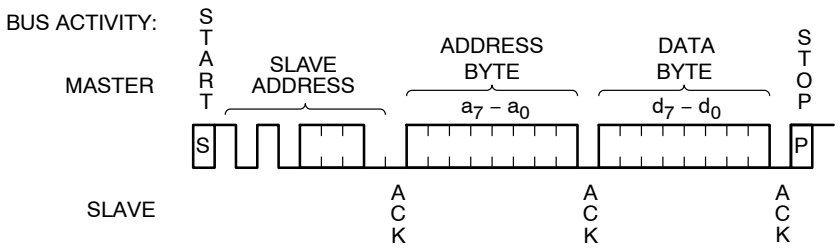


Figure 6. Byte Write Sequence

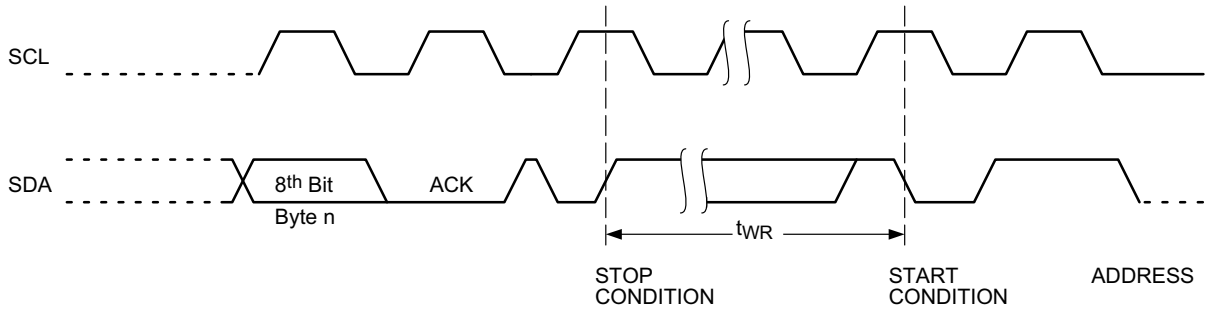


Figure 7. Write Cycle Timing

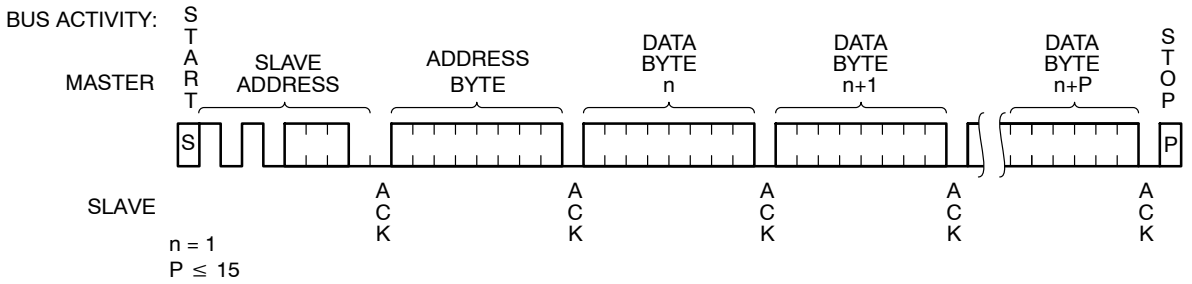


Figure 8. Page Write Sequence

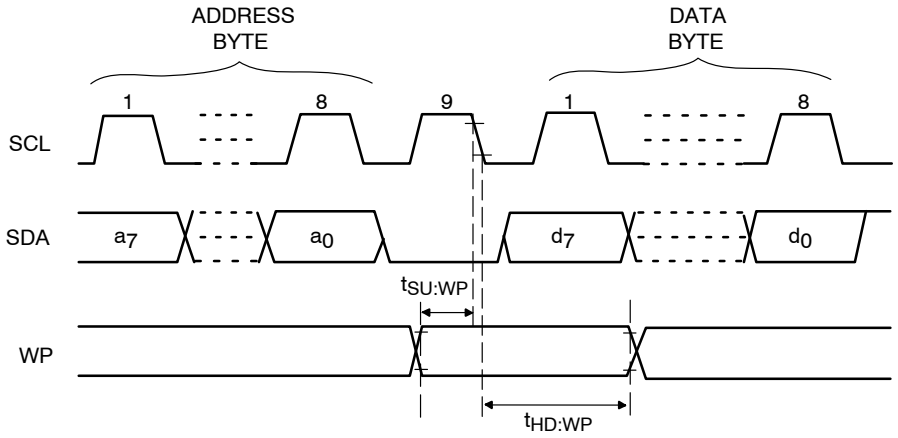


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/W bit set to '1', the CAV24Cxx will interpret this as a request for data residing at the current byte address in memory. The CAV24Cxx will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAV24Cxx returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAV24Cxx acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/W bit set to one. The CAV24Cxx then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAV24Cxx will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap−around at end of memory (rather than end of page).

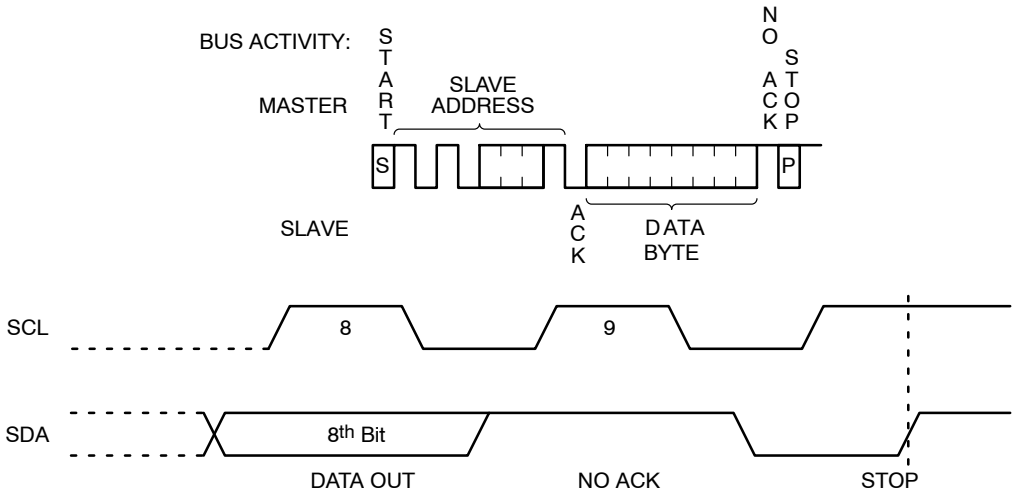


Figure 10. Immediate Read Sequence and Timing

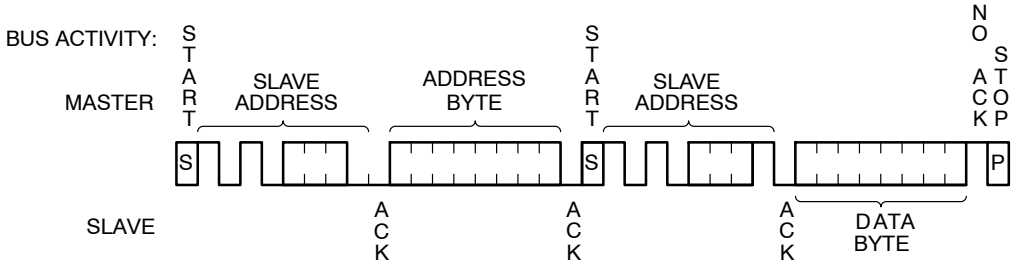


Figure 11. Selective Read Sequence

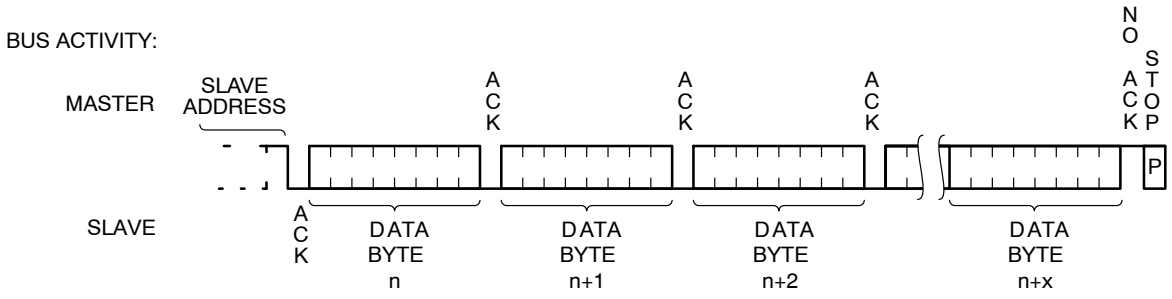


Figure 12. Sequential Read Sequence

CAV24C02 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV24C02WE−GT3	24C02H	SOIC−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C02YE−GT3	C02H	TSSOP−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel

CAV24C04 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV24C04WE−GT3	24C04K	SOIC−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C04YE−GT3	C04K	TSSOP−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C04C4ATR	4	WLCSP−4	−40°C to +125°C	N/A	5,000 Units / Tape & Reel
CAV24C04C5ATR	4	WLCSP−5	−40°C to +125°C	N/A	5,000 Units / Tape & Reel

CAV24C08 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV24C08WE−GT3	24C08K	SOIC−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C08YE−GT3	C08K	TSSOP−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C08C4ATR	8	WLCSP−4	−40°C to +125°C	N/A	5,000 Units / Tape & Reel
CAV24C08C4CTR*	8	WLCSP−4	−40°C to +125°C	N/A	5,000 Units / Tape & Reel
CAV24C08C5ATR	8	WLCSP−5	−40°C to +125°C	N/A	5,000 Units / Tape & Reel

* CAV24C08C4CTR is a backside coated version. Contact factory for other densities.

CAV24C16 Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV24C16WE−GT3	24C16K	SOIC−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C16YE−GT3	C16K	TSSOP−8	−40°C to +125°C	NiPdAu	3,000 Units / Tape & Reel
CAV24C16C4ATR	6	WLCSP−4	−40°C to +125°C	N/A	5,000 Units / Tape & Reel
CAV24C16C5ATR	6	WLCSP−5	−40°C to +125°C	N/A	5,000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. All packages are RoHS−compliant (Lead−free, Halogen−free).

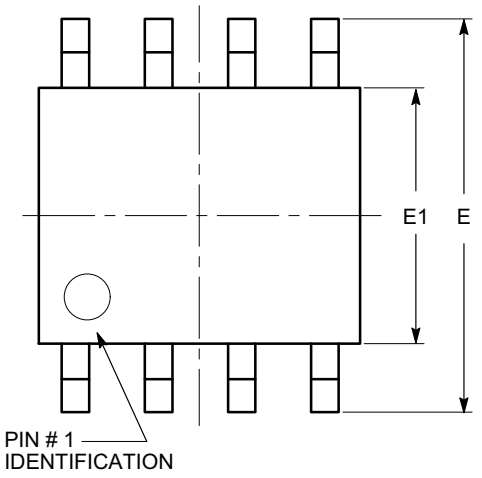
ON Semiconductor is licensed by the Philips Corporation to carry the I^2C bus protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

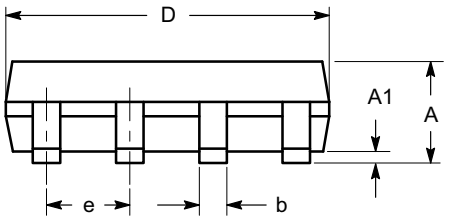
SOIC 8, 150 mils
CASE 751BD–01
ISSUE O

DATE 19 DEC 2008

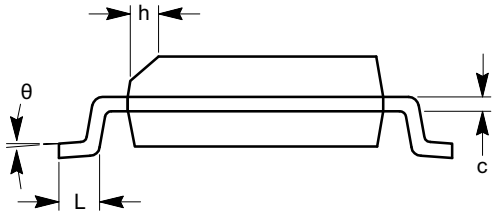


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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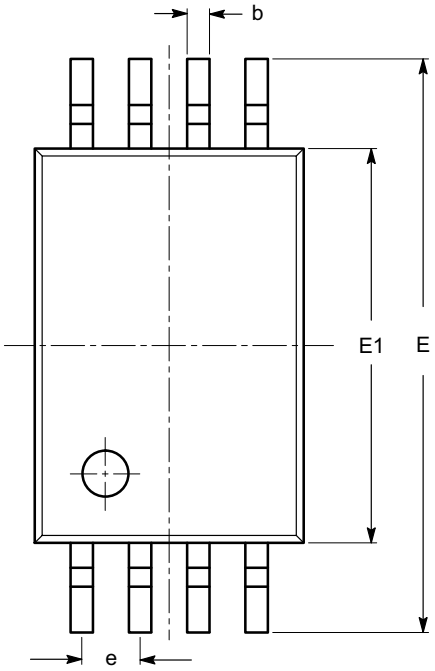
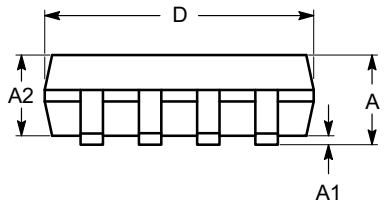
TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

DATE 19 DEC 2008

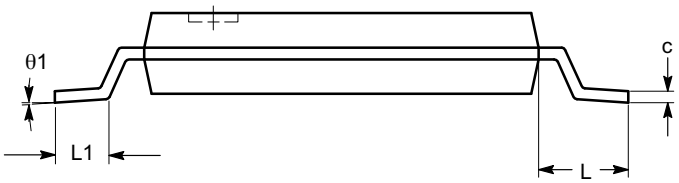


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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