Texas Instruments

THS3202EVM

User's Guide

October 2002 *High Performance Linear Products*

SLOU148

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.The input supply voltage ($\pm V_S$) should be no greater than $\pm$7.5 V for dual supply or 15 V for single supply. The differential input signal (V_{ID}) should be no greater than $\pm$3 V. The output current (I_O) should be no greater than 150 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URLs below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time. Go to the TI website at www.ti.com and search on the literature number (e.g., SLOS242).

- THS3202 data sheet (SLOS242)
- Application report (SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits,* http://www-s.ti.com/sc/psheets/sloa069/sloa069.pdf
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, http://www-s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (SLMA004), PowerPAD Made Easy, http://www-s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (SSYA008), Electrostatic Discharge (ESD), http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf
- High-Speed Amplifier PCB Layout Tips, SLOA102

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Chapter 1

Introduction and Description

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and a monitoring instrument. See Figure 1-1 for the default schematic diagram. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The complete EVM schematic—showing all components—is shown in this chapter.

EVM Channel 1:

The default configuration for EVM channel 1 provides a voltage gain of –1 and about +2 depending on which input is connected to the signal source. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 1) to the voltage at the input at J2 or J3 respectively.

For optimum frequency response and stability at either –1 or +2 gain, 536-Ω is chosen for R6, the gain resistor. R1 is set to the same value to provide a gain of –1 in the inverting configuration. R2 is set to 54.9 Ω to match the signal generator source impedance—the closest value when placed in parallel with R1 (536 Ω) that terminates the inverting input to 50 Ω. R4 is set to 453 Ω because when a high impedance instrument is connected to output connector J1, the amplifier is loaded at about 500 Ω.

When EVM channel 1 is used as an inverting amplifier in the default configuration, and is connected to a 50-Ω input device, R4 causes a slight gain error. The total voltage gain is the negative ratio of feedback resistor R6, and gain resistor R1, times the voltage divider created by R5, R4, and the measurement device input termination resistance. This gain is expressed in the following equation.

$$\frac{V_O}{V_I} = -\frac{R6}{R1}\left(\frac{-\,R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = -\,0.474 \qquad (1)$$

When using the default configuration, the noninverting gain of the EVM channel 1 amplifier is affected by the same slight gain error, plus the gain error imposed by the inverting input termination resistor R2. The following equation shows the gain for this situation.

$$\frac{V_O}{V_I} = \left(1 + \frac{R6}{R1 + R2}\right)\left(\frac{R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = 0.911 \quad (2)$$

EMV Channel 2:

The default configuration for EVM channel 2 is designed to provide a voltage gain of +1. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 7) to the voltage at the J5 input. The value of feedback resistor R7 is chosen to be 619 Ω. This gives optimum frequency response and stability at a gain of +1.

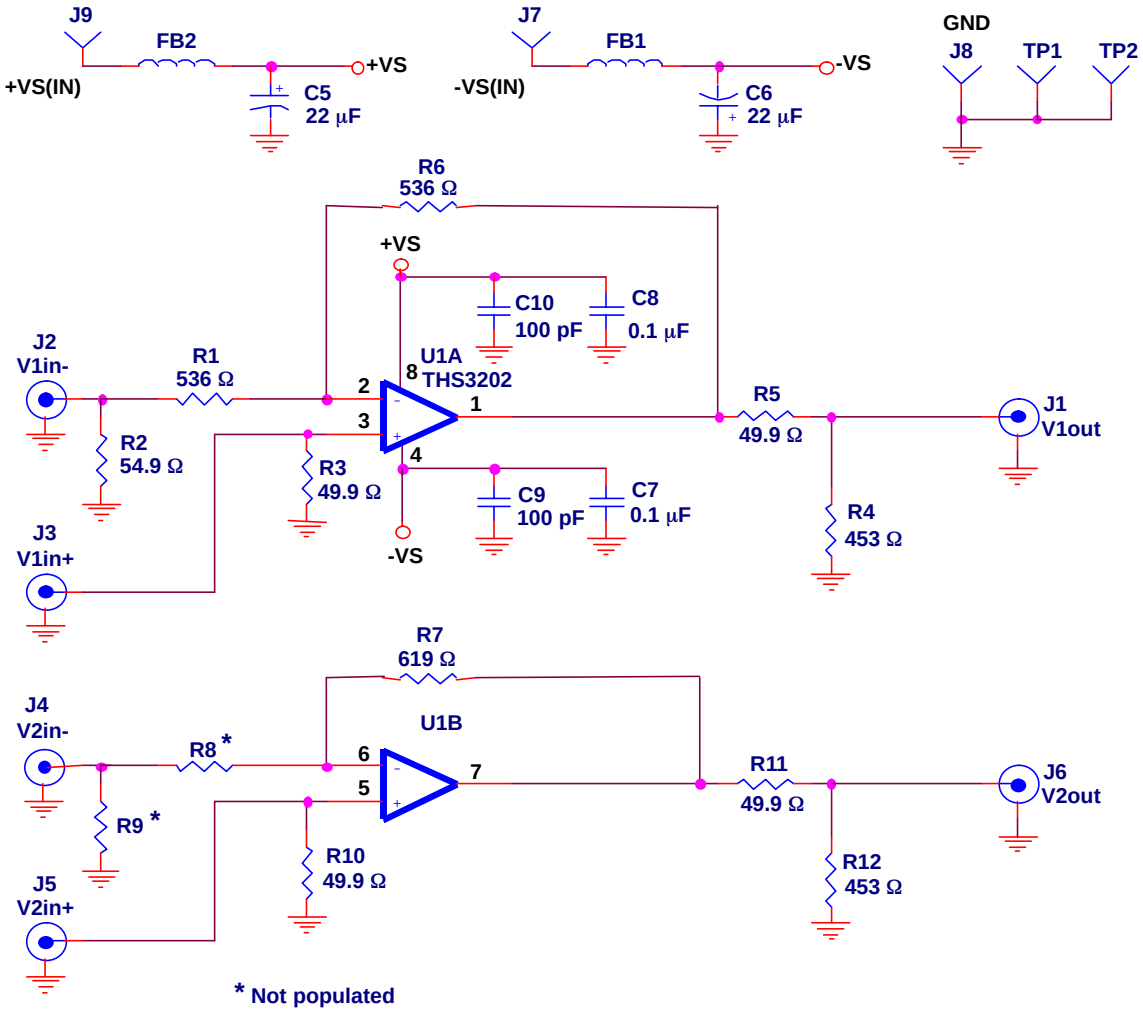
When using the default configuration, the noninverting gain of the EVM channel 2 amplifier is affected by the same slight gain error caused by R12, as shown in Equation 1 and indicated in following equation.

$$\frac{V_O}{V_I} = \left(\frac{-R12 \parallel 50\ \Omega}{R12 \parallel 50\ \Omega + R11}\right) = -0.474 \quad (3)$$

THS3202 dual high-speed operational amplifier EVM features include:

- Wide operating supply voltage range: dual supply ±3 V to dual supply ±7.5 V operation (see the device data sheet). Single supply operation is obtained by connecting both J6 (GND) and J7 (V_S-) to ground.
- Convenient GND test point (TP1)
- Power supply ripple rejection provided by inductors FB1 and FB2, followed by tantalum capacitors C5 and C6
- Decoupling capacitors C7 and C8 are populated with 0.1 μF, and capacitors C9 and C10 are populated with 100 pF—users design the final decoupling in accordance with SLOA069
- Nominal 50-Ω input impedance for each of the configured inputs (V1in–, V1in+ and V2in+. Termination can be configured according to the application requirement.
- A good example of high-speed amplifier PCB design and layout. Also see High-Speed Amplifier PCB Layout Tips, SLOA102.
- 50-Ω series matching resistors (R5 and R11)
- 453-Ω resistor to ground provides minimum load through 500 Ω on each amplifier
- PowerPAD™ heatsinking capability

Figure 1-1. Schematic of the THS3202EVM



Chapter 2

Using the THS3202 EVM

This chapter shows how to connect the THS3202EVM to test equipment. It is recommended that the user connect the EVM as described in this chapter to avoid damage to the EVM, or the THS3202 installed on the board. Figure 2–1 shows how to connect power supplies, a 50-Ω signal source, and 50-Ω monitoring instrument

Figure 2-1. THS3202EVM Interconnection Diagram

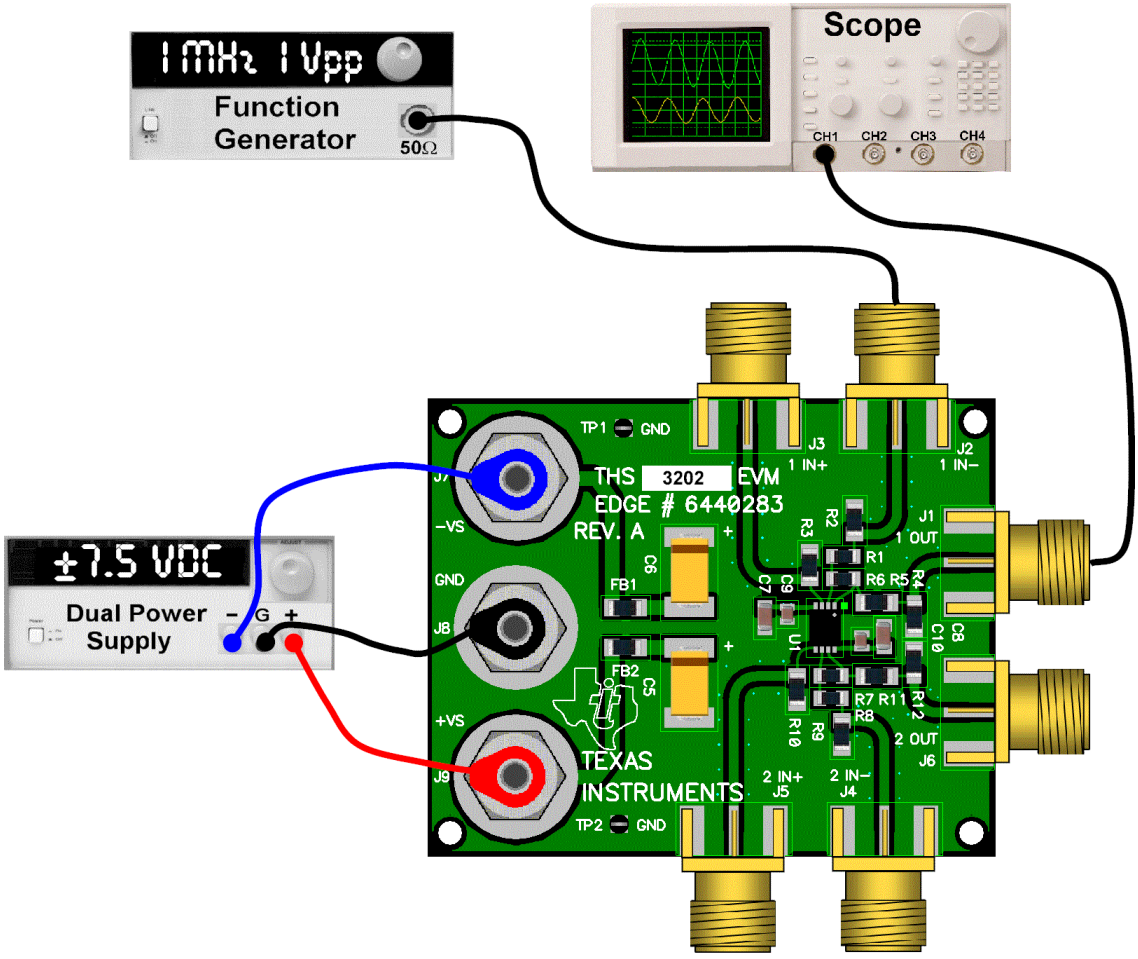


Figure 2-1 shows the connections to measure the EVM output 1 while a signal is inserted into EVM channel 1's inverting input. The signal source can instead be connected to J2 for a noninverting signal path. If the oscilloscope input is connected to J6 and the signal source is connected to J5, EVM channel 2 is also configured for a noninverting signal path.

Chapter 3

THS3202EVM Applications

Example applications are presented in this chapter. These applications are meant to demonstrate the most popular circuits, but many other circuits can be constructed. The user is encouraged to experiment with different circuits—exploring new and creative design techniques, which is the function of an evaluation board.

3.1 Inverting Gain Stage

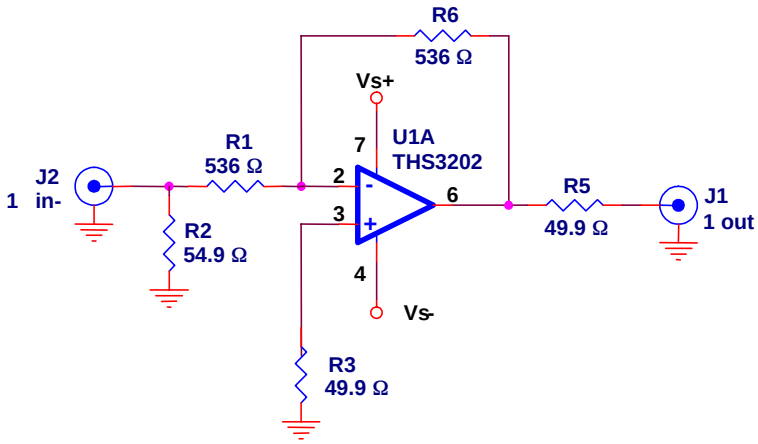
The circuit described in Chapter 2 is an inverting gain stage with a voltage divider on the output. Equation 1 (Chapter 1) indicates the gain when connected to a 50-Ω measurement input device. The 453-Ω R4 is included to provide a 500-Ω load to the amplifier—the user may remove it as shown in Figure 3-1. When this is done the voltage gain equation from J2 to J1 is simplified as shown:

$$\frac{V_O}{V_I} = -\frac{R6}{R1}\left(\frac{50\ \Omega}{50\ \Omega + R5}\right) = 0.5 \qquad (1)$$

R5 is used to match the output impedance of the amplifier to the line being driven and the instrument taking measurements. For short transmission line length, R5 can be replaced with a jumper.

R5 can also be used to isolate the amplifier from extremely large capacitive loads.

Figure 3-1. Inverting Gain Stage

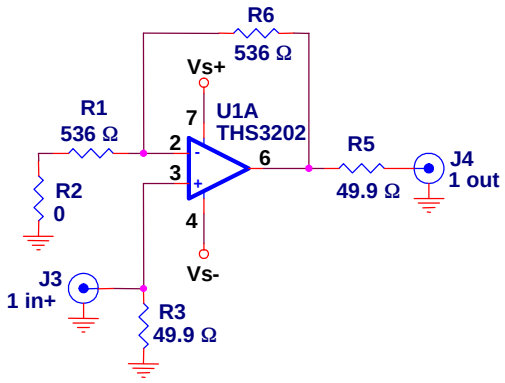


3.2 Noninverting Gain Stage

For a noninverting stage in EVM channel 1, the EVM can be modified to eliminate the gain error imposed by R2 by replacing R2 with a 0-Ω resistor. This is shown in Figure 3-2. R4 has been removed as shown in the inverting gain stage example above. The following equation indicates the voltage gain from J3 to J1:

$$\frac{V_O}{V_I} = \left(1 + \frac{R6}{R1}\right)\left(\frac{50\ \Omega}{50\ \Omega + R5}\right) = 1 \qquad (2)$$

Figure 3-2. Noninverting Gain Stage



This is a common amplifier configuration used to drive a transmission line. The 49.9-Ω resistor in series with the output matches the effective output impedance of the amplifier to the line impedance. In test and measurement instruments the nominal line impedance is assumed to be 50 Ω—for video, the nominal line impedance is assumed to be 75 Ω. If testing this device as a video linear driver TI recommends changing the value of R5 to 75 Ω.

Due to the nature of current feedback high speed amplifiers, the gain of the THS3202 can be increased by decreasing the values of R1 and R8 with little change in bandwidth. R6 should be reduced to maintain optimum compensation. See the device data sheet for recommended resistor values.

3.3 Applications for EVM Channel 2

Since the board layout of EVM channel 2 is identical to EVM channel 1, the applications above can be applied identically. The only physical difference is that different values have been installed in the default configuration for different EVM channels. In addition, the components are labeled differently for each EVM channel. Refer to the complete schematic and board silkscreen to resolve component locations and values.

Chapter 4

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed-circuit board layout.

Table 4-1. THS3202EVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB	Manufacturer's Part Number	Distributor's Part Number
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Capacitor, 22 μF, tanatalum, 25 V, 10%	D	C5, C6	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Capacitor, 0.1 μF, ceramic, X7R, 50 V	0805	C7, C8	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Capacitor, 100 pF, ceramic, 5%, 150V	AQ12	C9, C10	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
5	Open	0805	R8	1		
6	Resistor, 619 Ω, 1/8W, 1%	0805	R7	1	(Phycomp) 9C08052A6190FKHFT	(Garrett) 9C08052A6190FKHFT
7	Resistor, 536 Ω, 1/8W, 1%	0805	R1, R6	2	(Phycomp) 9C08052A5360FKHFT	(Garrett) 9C08052A5360FKHFT
8	Open	1206	R9	1		
9	Resistor, 54.9 Ω, 1/4W, 1%	1206	R2	1	(Phycomp) 9C12063A54R9FKRFT	(Garrett) 9C12063A54R9FKRFT
10	Resistor, 49.9 Ω, 1/4W, 1%	1206	R3, R5, R10, R11	4	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
11	Resistor, 453 Ω, 1/4W, 1%	1206	R4, R12	2	(Phycomp) 9C12063A4530FKRFT	(Garrett) 9C12063A4530FKRFT
12	Jack, banana receptacle 0.25" diameter hole		J7, J8, J9	3	(HH Smith) 101	(Newark) 35F865
13	Test point, black		TP1, TP2	2	(Keystone) 5001	(Allied) 839-3601
14	Connector, edge, SMA PCB jack		J1, J2, J3, J4, J5, J6	6	(Johnson) 142-0701-801	(Allied) 528-0238
15	IC, THS3202		U1	1	(TI) THS3202DGN	
16	Board, printed-circuit			1	(TI) EDGE # 6440283	

Figure 4-1. Top Layer 1 (Signals and Silk Screen) for THS3202EVM

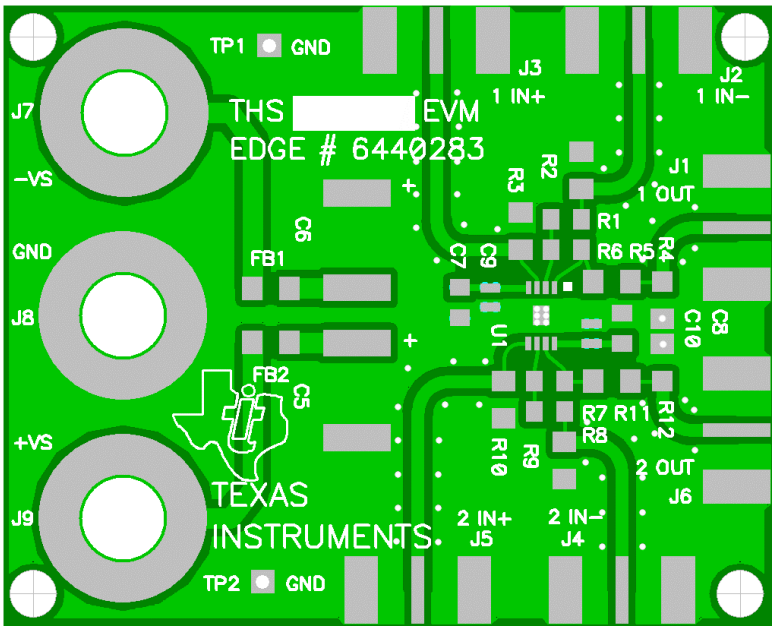


Figure 4-2. Internal Plane (Layer 2) Ground Plane

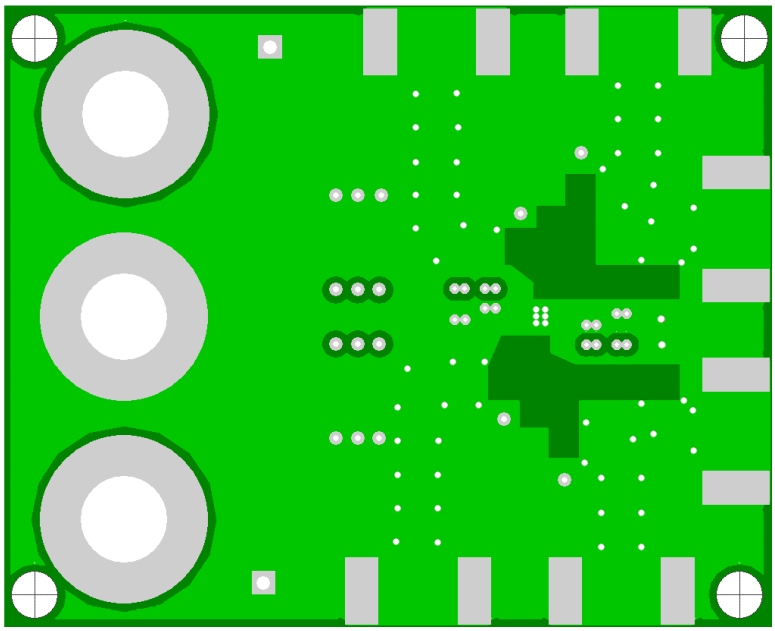


Figure 4-3. Internal Plane (Layer 3) Power Plane

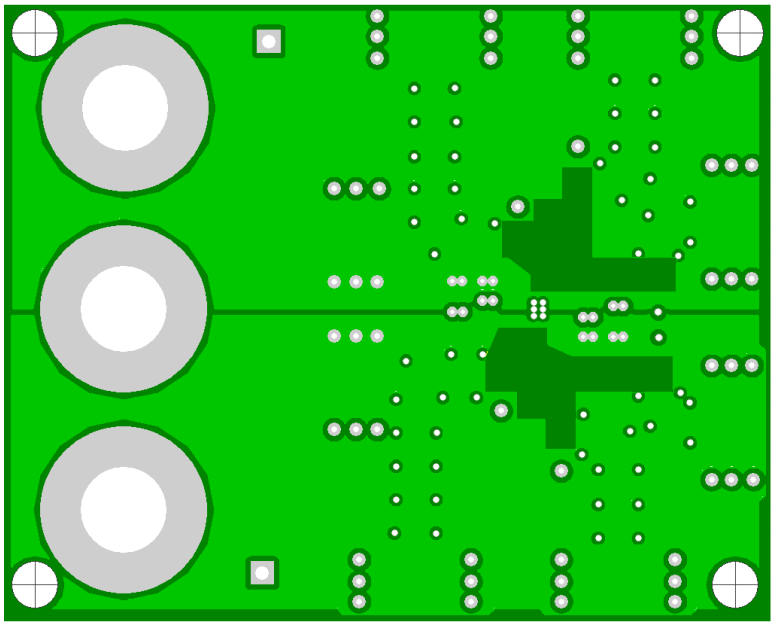


Figure 4-4. Bottom (Layer 4) Ground and Signal