MGA-82563

0.1 – 6 GHz 3 V, 17 dBm Amplifier

Data Sheet

Description

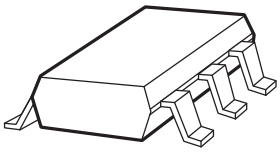
Avago's MGA-82563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent power and low noise figure for applications from 0.1 to 6 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The input and output of the amplifier are matched to 50Ω (below 2:1 VSWR) across the entire bandwidth, eliminating the expense of external matching. The amplifier allows a wide dynamic range by offering a 2.2 dB NF coupled with a +31 dBm Output IP_3.

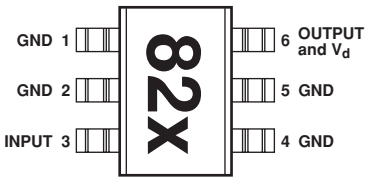
The circuit uses state-of-the-art PHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3 V power supply, while resistive feedback ensures stability (K>1) over all frequencies and temperatures.

Surface Mount Package

SOT-363 (SC-70)



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

"82" = Device Code
"x" = Date code character identifies month of manufacture

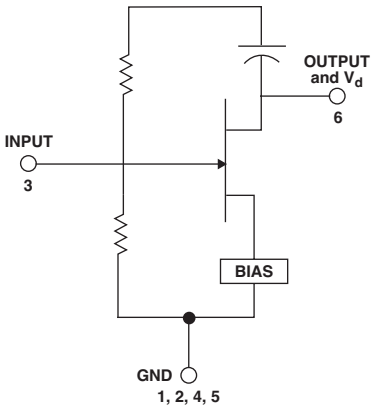
Features

- Lead-free Option Available
- +17.3 dBm $P_{1\,dB}$ at 2.0 GHz
  +20 dBm P_{sat} at 2.0 GHz
- Single +3V Supply
- 2.2 dB Noise Figure at 2.0 GHz
- 13.2 dB Gain at 2.0 GHz
- Ultra-miniature Package
- Unconditionally Stable

Applications

- Buffer or Driver Amp for PCS, PHS, ISM, SATCOM and WLL Applications
- High Dynamic Range LNA

Simplified Schematic



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

MGA-82563 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Device Voltage, RF Output to Ground	V	5.0
V_{gd}	Device Voltage, Gate to Drain	V	-6.0
V_{in}	Range of RF Input Voltage to Ground	V	+0.5 to -1.0
P_{in}	CW RF Input Power	dBm	+13
T_{ch}	Channel Temperature	°C	165
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:

$\theta_{ch-c} = 180°C/W$

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the top of the package.)

MGA-82563 Electrical Specifications, $T_C = 25°C$, $Z_0 = 50\ \Omega$, $V_d = 3\ V$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std Dev[2]
G_{test}	Gain in test circuit[1]	f = 2.0 GHz		12.0	13.2	15	0.35
NF_{test}	Noise Figure in test circuit[1]	f = 2.0 GHz			2.2	2.9	0.20
NF_{50}	Noise Figure in 50 Ω system	f = 0.5 GHz	dB		2.3		
		f = 1.0 GHz			2.2		
		f = 2.0 GHz			2.2		0.20
		f = 3.0 GHz			2.2		
		f = 4.0 GHz			2.4		
		f = 6.0 GHz			2.7		
$\|S_{21}\|^2$	Gain in 50 Ω system	f = 0.5 GHz	dB		14.7		
		f = 1.0 GHz			14.5		
		f = 2.0 GHz			13.5		0.35
		f = 3.0 GHz			12.1		
		f = 4.0 GHz			10.7		
		f = 6.0 GHz			8.8		
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.4		
		f = 1.0 GHz			17.5		
		f = 2.0 GHz			17.3		0.54
		f = 3.0 GHz			17.1		
		f = 4.0 GHz			17.0		
		f = 6.0 GHz			16.8		
IP_3	Output Third Order Intercept Point	f = 2.0 GHz	dBm		+31		1.0
$VSWR_{in}$	Input VSWR	f = 0.2 – 5.0 GHz			1.8:1		
$VSWR_{out}$	Output VSWR	f = 0.2–5.0 GHz			1.2:1		
I_d	Device Current		mA	63	84	101	

Notes:

1. Guaranteed specifications are 100% tested in the circuit in Figure 10 in the Applications Information section.
2. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

MGA-82563 Typical Performance, $T_c = 25°$ C, $V_d = 3$ V

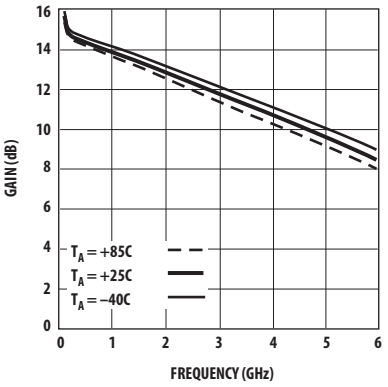


Figure 1. 50 Power Gain vs. Frequency and Temperature.

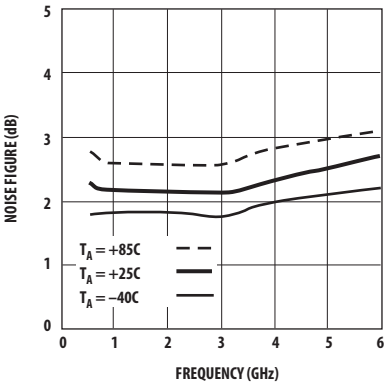


Figure 2. Noise Figure (into 50) vs. Frequency and Temperature.

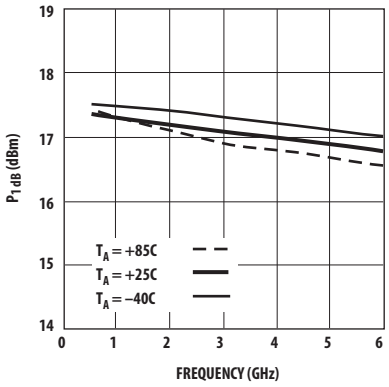


Figure 3. Output Power @ 1 dB Gain Compression vs. Frequency and Temperature.

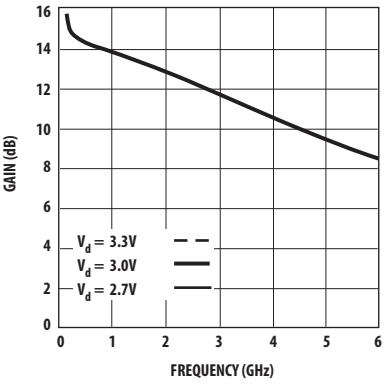


Figure 4. 50 Power Gain vs. Frequency and Voltage.

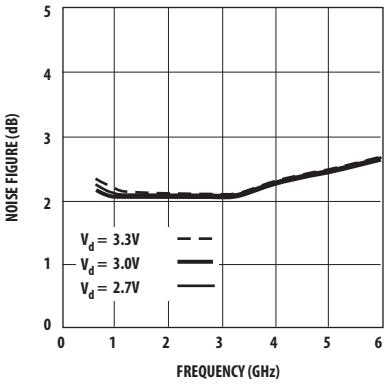


Figure 5. Noise Figure (into 50) vs. Frequency and Voltage.

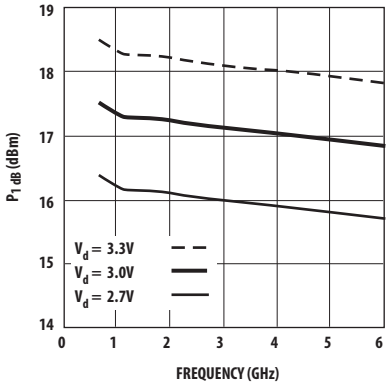


Figure 6. Output Power @ 1 dB Gain Compression vs. Frequency and Voltage.

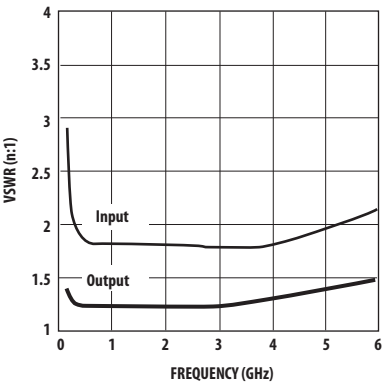


Figure 7. Input and Output VSWR into 50 vs. Frequency.

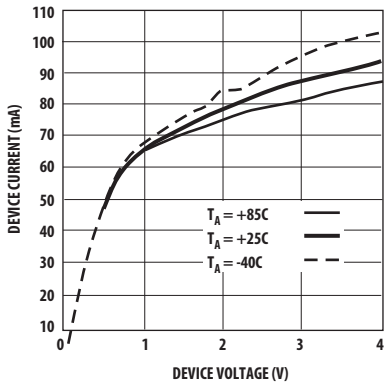


Figure 8. Device Current vs. Voltage and Temperature.

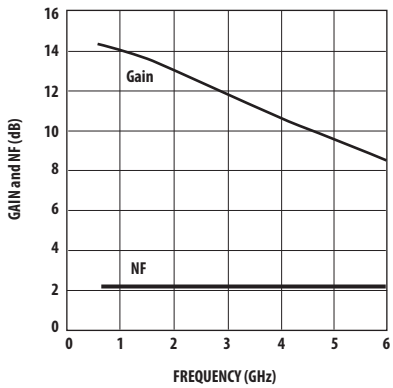


Figure 9. Minimum Noise Figure and Associated Gain vs. Frequency.

MGA-82563 Typical Scattering Parameters[1], $T_C = 25°C$, $Z_0 = 50\ \Omega$, $V_d = 3\ V$

Freq.	S_{11}		S			S			S		K
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	Factor
0.1	0.48	-39	15.71	6.10	164	-23	0.070	27	0.16	-99	1.02
0.2	0.35	-35	14.81	5.50	165	-22	0.076	14	0.12	-134	1.20
0.5	0.29	-37	14.34	5.21	159	-22	0.079	6	0.11	177	1.29
1.0	0.29	-57	13.95	4.98	144	-22	0.080	3	0.11	156	1.33
1.5	0.29	-78	13.50	4.73	128	-22	0.082	2	0.10	142	1.37
2.0	0.29	-99	12.99	4.46	114	-22	0.085	1	0.10	131	1.41
2.5	0.29	-118	12.45	4.19	99	-21	0.089	-1	0.10	124	1.44
3.0	0.28	-138	11.84	3.91	86	-21	0.093	-3	0.11	118	1.48
3.5	0.28	-158	11.24	3.65	74	-21	0.098	-6	0.12	111	1.51
4.0	0.29	-177	10.67	3.42	61	-20	0.103	-9	0.13	106	1.52
4.5	0.30	166	10.11	3.20	50	-20	0.107	-13	0.15	100	1.53
5.0	0.32	151	9.58	3.01	38	-19	0.112	-18	0.16	94	1.54
5.5	0.34	136	9.07	2.84	27	-19	0.117	-23	0.18	87	1.55
6.0	0.36	123	8.57	2.68	16	-19	0.121	-29	0.19	82	1.54
6.5	0.38	110	8.06	2.53	5	-19	0.125	-35	0.22	74	1.55
7.0	0.40	97	7.51	2.37	-5	-18	0.126	-41	0.24	66	1.59

MGA-82563 Typical Noise Parameters[1]

$T_C = 25°C$, $Z_0 = 50\ \Omega$, $V_d = 3\ V$

Frequency	NF_0	Γ_{opt}		$R_n / 50\ \Omega$
GHz	dB	Mag.	Ang.	—
0.5	2.10	0.15	25	1.20
1.0	2.10	0.15	45	0.60
1.5	2.10	0.14	65	0.29
2.0	2.12	0.15	75	0.27
2.5	2.12	0.15	94	0.25
3.0	2.15	0.144	113	0.23
3.5	2.16	0.14	134	0.21
4.0	2.16	0.15	155	0.19
4.5	2.19	0.17	177	0.18
5.0	2.18	0.20	-166	0.18
5.5	2.19	0.22	-152	0.18
6.0	2.23	0.25	-138	0.19
6.5	2.28	0.27	-125	0.23
7.0	2.39	0.29	-111	0.28

Note:

1. Reference plane per Figure 11 in Applications Information section.

MGA-82563 Applications Information

Introduction

This medium power GaAs MMIC amplifier was developed for commercial wireless applications from 100 MHz to 6 GHz. The MGA-82563 runs on only 3 volts and typically requires only 84 mA to deliver over 17 dBm of output power at 1 dB gain compression.

The 17.3 dBm output power ($P_{1\,dB}$) makes the MGA-82563 extremely useful for pre-driver and driver stages in transmit cascades or for final output stages in lower power systems. For transmitter gain stage applications that require even higher output power, the MGA-82563 can provide 100 mW (20 dBm) of saturated output power with a power added efficiency approaching 50%. The low cost of the MGA-82563 makes it feasible to power combine two (or more) devices for even higher output power amplifiers.

The MGA-82563 offers an excellent combination of high linearity (+31 dBm output IP_3) and very low noise figure (2.2 dB) for applications requiring a very high dynamic range.

The MGA-82563 uses resistive feedback to simultaneously achieve flat gain over a wide bandwidth and to match the input and output impedances to 50Ω. The MGA-82563 is also unconditionally stable (K>1) over its entire frequency range, making it both very easy to use and yielding consistent performance in the manufacture of high volume wireless products.

An innovative internal bias circuit regulates the device's internal current to enable the MGA-82563 to operate over a wide temperature range with a single, positive power supply of 3 volts. The MGA-82563 will operate with reduced power and gain with a bias supply as low as 1.5 volts.

Test Circuit

The circuit shown in Figure 10 is used for 100% RF testing of Gain and Noise Figure. The test circuit is merely a 50Ω input/output PC board with a RFC at the output to apply DC bias to the device under test. Tests in this circuit are used to guarantee the NF_{test} and G_{test} parameters shown in the table of Electrical Specifications.

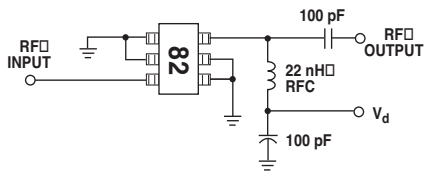


Figure 10. Test Circuit.

Phase Reference Planes

The positions of the reference planes used to specify the S-Parameters and Noise Parameters for this device are shown in Figure 11. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

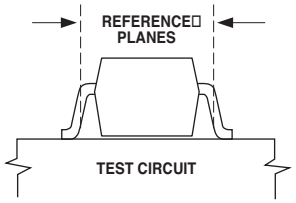


Figure 11. Phase Reference Planes.

Specifications and Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either "minimum or maximum," "typical," or "standard deviations."

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard "bell curve."

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the MGA-82563, these parameters are: Gain (G_{test}), Noise Figure (NF_{test}), and Device Current (I_d). Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as the Noise and S-parameter tables or performance curves, the data represents a nominal part taken from the "center" of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the MGA-82563, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 12 for example, the probability of a parameter being between ±1σ is 68.3%; between ±2σ is 95.4%; and between ±3σ is 99.7%.

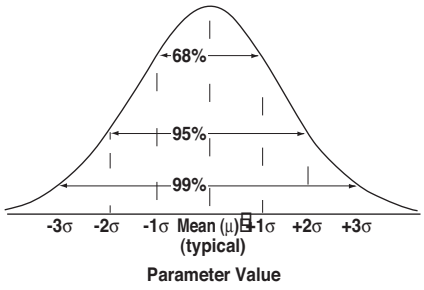


Figure 12. Normal Distribution.

RF Layout

The RF layout in Figure 13 is suggested as a starting point for microstripline designs using the MGA-82563 amplifier. Adequate grounding is needed to obtain optimum performance and to maintain stability. All of the ground pins of the MMIC should be connected to the RF groundplane on the backside of the PCB by means of plated through holes (vias) that are placed near the package terminals. As a minimum, one via should be located next to each ground pin to ensure good RF grounding. It is a good practice to use multiple vias to further minimize ground path inductance.

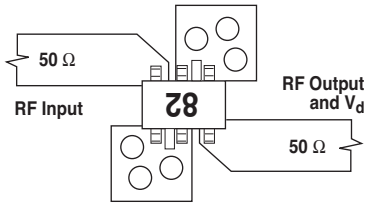


Figure 13. RF Layout.

In addition to the RF considerations, the use of multiple vias for grounding is important for the purpose of providing a lower resistance thermal path to the heatsink.

It is recommended that the PCB pads for the ground pins *not* be connected together underneath the body of the package. PCB traces hidden under the package cannot be adequately inspected for SMT solder quality.

PCB Material

FR-4 or G-10 printed circuit board materials are a good choice for most low cost wireless applications. Typical board thickness is 0.020 to 0.031 inches. The width of the 50 Ω microstriplines on PC boards in this thickness range is also very convenient for mounting chip components such as the series inductor at the input or DC blocking and bypass capacitors.

For higher frequencies or for noise figure critical applications, the additional cost of PTFE/glass dielectric materials may be warranted to minimize transmission line loss at the amplifier's input. A 0.5 inch length of 50 Ω microstripline on FR-4, for example, has approximately 0.3 dB loss at 4 GHz. This loss will add directly to the noise figure of the MGA-82563.

Biasing

The MGA-82563 is a voltage-biased device and is designed to operate from a single, +3 volt power supply with a typical current drain of 84 mA. The internal current regulation circuit allows the amplifier to be operated with voltages as low as +1.5 volts. Refer to the section titled "Operation at Bias Voltages Other than 3 Volts" for information on performance and precau tions when using other voltages.

Typical Application Example

The printed circuit layout in Figure 14 can serve as a design guide. This layout is a microstripline design (solid groundplane on the backside of the circuit board) with a 50 Ω input and output. The circuit is fabricated on 0.031-inch thick FR-4 dielectric material. Plated through holes (vias) are used to bring the ground to the top side of the circuit where needed. Multiple vias are used to reduce the inductance of the paths to ground.

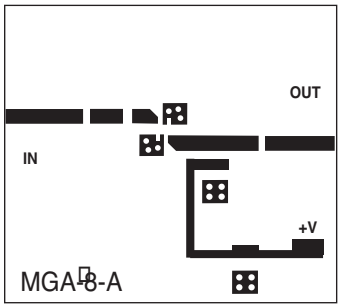


Figure 14. PCB Layout.

A schematic diagram of the application circuit is shown in Figure 15. DC blocking capacitors (C1 and C2) are used at the input and output of the MMIC to isolate the device from adjacent circuits. While the input terminal of the MGA-82563 is at ground potential, it is not a current sink. If the input is connected to a preceding stage that has a voltage present, the use of the DC blocking capacitor (C1) is required.

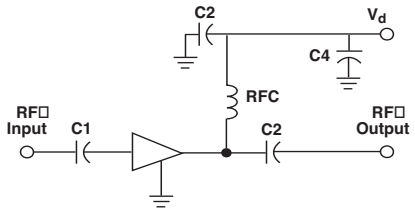


Figure 15. Schematic Diagram.

DC bias is applied to the MGA-82563 through the RF Output pin. An inductor (RFC), or length of high impedance transmission line (preferably λ/4 at the band center), is used to isolate the RF from the DC supply.

The power supply is bypassed to ground with capacitor C3 to keep RF off of the DC lines and to prevent gain dips or peaks in the response of the amplifier.

An additional bypass capacitor, C4, may be added to the bias line near the V_d connection to eliminate unwanted feedback through bias lines that could cause oscillation. C4 will not normally be needed unless several stages are cascaded using a common power supply.

When multiple bypass capacitors are used, consideration should be given to potential resonances. It is important to ensure that the capacitors when combined with additional parasitic L's and C's on the circuit board do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate the effect of a resonance.

The value of the DC blocking and RF bypass capacitors (C1 - C3) should be chosen to provide a small reactance (typically <5 ohms) at the lowest operating frequency. The reactance of the RF choke (RFC) should be high (e.g., several hundred ohms) at the lowest frequency of operation.

The MGA-82563's response at low frequencies is limited to approximately 100 MHz by the size of capacitors integrated on the MMIC chip.

The input and output of the MGA-82563 are well matched to 50 Ω. Without external matching elements, the input VSWR of the MGA-82563 is ≤ 2.0:1 from 300 MHz to 6 GHz and the Output VSWR is ≤ 1.6:1 from 100 MHz through 6 GHz.

For applications requiring minimum noise figure (NF_o), some improvement over a 50Ω match is possible by matching the signal input to the optimum noise match impedance, Γ_o, as specified in the "Typical Noise Parameters" table. The data in the table shows the noise match to be very close to 50Ω.

The completed application amplifier with all components and SMA connectors is shown in Figure 16.

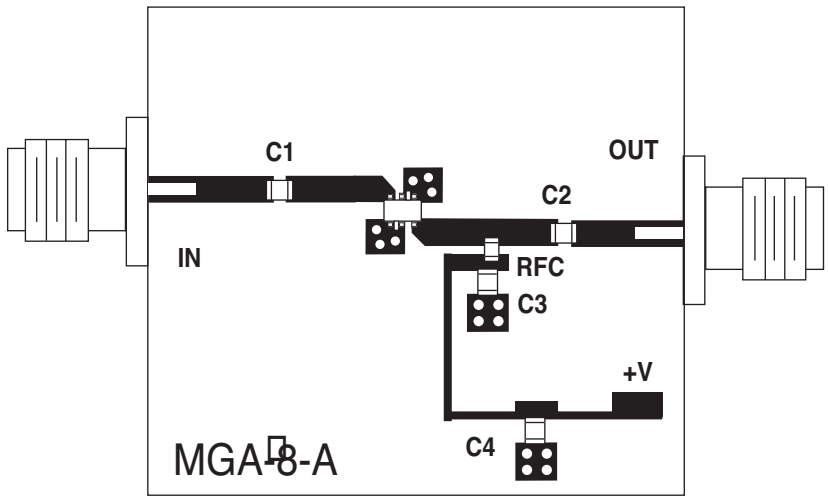


Figure 16. Complete Application Circuit.

Operation in Saturation for Higher Output Power

For applications such as pre-driver, driver, and output stages in transmitters, the MGA-82563 can be operated in saturation to deliver up to 100 mW (20 dBm) of output power. The power added efficiency approaches 50% at these power levels.

There are several design considerations related to reliability and performance that should be taken into account when operating the amplifier in saturation.

First of all, it is important that the stage preceding the MGA-82563 not overdrive the device. Referring to the "Absolute Maximum Ratings" table, the maximum allowable input power is +13 dBm. This should be regarded as the input power level above which the device could be permanently damaged.

Driving the amplifier into saturation will also affect electrical performance. Figure 17 presents the Output Power, Third Order Intercept Point (Output $IP_{3)}$, and Power Added Efficiency (PAE) as a function of Input Power. This data represents performance into a 50Ω load. Since the output impedance of the device changes when driven into saturation, it is possible to obtain even more output power with a "power match." The optimum impedance match for maximum output power is dependent on specific frequency and actual output power level and can be arrived at empirically.

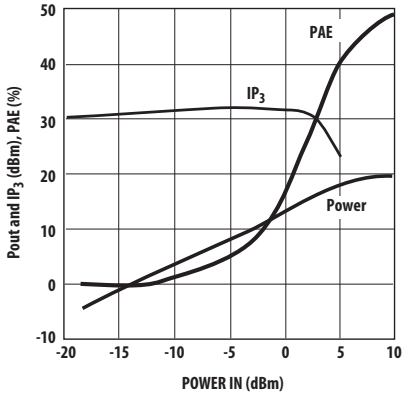


Figure 17. Output Power, IP_3, and Power-Added-Efficiency vs. Input Power. (V_d = 3.0 V)

As the input power is increased beyond the linear range of the amplifier, the gain becomes more compressed. Gain as a function of either input or output power may be derived from Figure 17. Gain compression renders the amplifier less sensitive to variations in the power level from the preceding stage. This can be a benefit in systems requiring fairly constant output power levels from the MGA-82563.

Increased efficiency (up to 45% at full output power) is another benefit of saturated operation. At high output power levels, the bias supply current drops by about 15%. This is normal and is taken into account for the PAE data in Figure 17.

Like other active devices, the intermodulation products of the MGA-82563 increase as the device is driven further into nonlinear operation. The 3rd, 5th, and 7th order intermodulation products of the MGA-82563 are shown in Figure 18 along with the fundamental response. This data was measured in the test circuit in Figure 10.

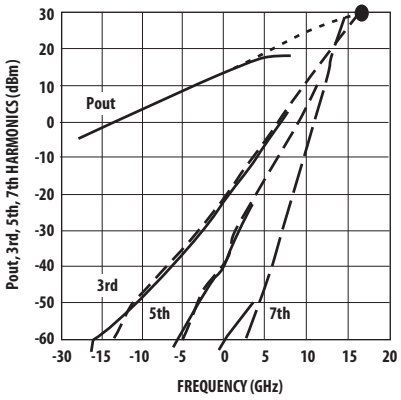


Figure 18. Intermodulation Products vs. Input Power. (V_d = 3.0 V)

Operation at Bias Voltages Other than 3 Volts

While the MGA-82563 is designed primarily for use in +3 volt applications, the internal bias regulation circuitry allows it to be operated with power supply voltages from +1.5 to +4 volts. Performance of Gain, Noise Figure, and Output Power over a wide range of bias voltage is shown in Figure 19. (This data was measured in the test circuit in Figure 10.) As can be seen, the gain and NF are fairly flat, but an increase in output power is possible by using higher voltages. The use of +4 volts increases the P_{1dB} by over 2 dBm.

If bias voltages greater than 3 volts are used, particular attention should be given to thermal management. Refer to the "Thermal Design Considerations" section for more details.

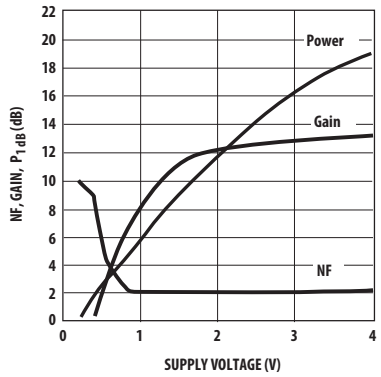


Figure 19. Gain, Noise Figure, and Output Power vs. Supply Voltage.

There are several means of biasing the MGA-82563 at 3 volts in systems that use higher power supply voltages. The simplest method, shown in Figure 20a, is to use a series resistor to drop the device voltage to 3 volts. For example, a 24 Ω resistor will drop a 5-volt supply to 3 volts at the nominal current of 84 mA. Some variation in performance could be expected for this method due to variations in current within the specified 63 to 101 mA min/max range.

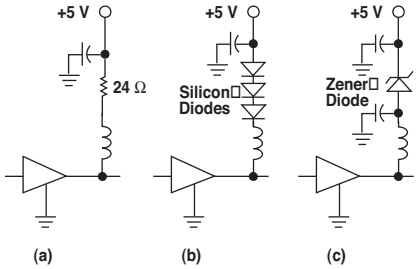


Figure 20. Biasing From Higher Supply Voltages.

A second method illustrated in Figure 20b, is to use forward-biased diodes in series with the power supply. For example, three silicon diodes connected in series will drop a 5-volt supply to approximately 3 volts.

The use of the series diode approach has the advantage of less dependency on current variation in the amplifiers since the forward voltage drop of a diode is somewhat current independent.

Reverse breakdown diodes (e.g., Zener diodes) could also be used as in Figure 20c. However, care should be taken to ensure that the noise generated by diodes in either Zener or reverse breakdown is adequately filtered (e.g., bypassed to ground) such that the diode's noise is not added to the amplifier's signal.

Note that the voltage-dropping component in each of these three methods must be able to safely dissipate up to 200 mW.

SOT-363 PCB Footprint

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the MGA-82563 is shown in Figure 21 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the MGA-82563. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

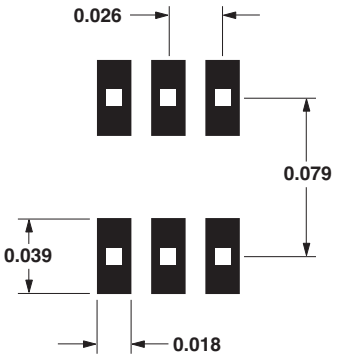
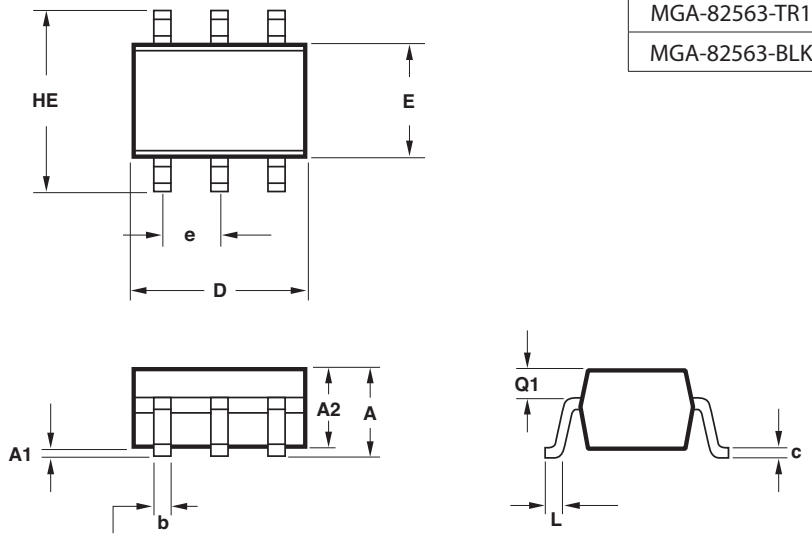


Figure 21. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

Package Dimensions

Outline 63 (SOT-363/SC-70)



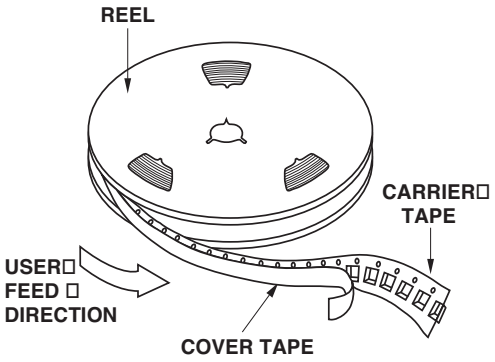
SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.650 BCS	
b	0.15	0.30
c	0.10	0.20
L	0.10	0.30

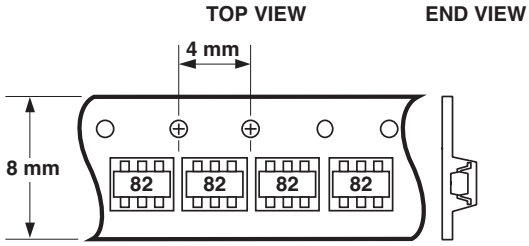
NOTES:
1. All dimensions are in mm.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to EIAJ SC70.
5. Die is facing up for mold and facing down for trim/form, ie: reverse trim/form.
6. Package surface to be mirror finish.

Part Number Ordering Information

Part Number	No. of Devices	Container
MGA-82563-TR1G	3000	7" Reel
MGA-82563-BLKG	100	antistatic bag

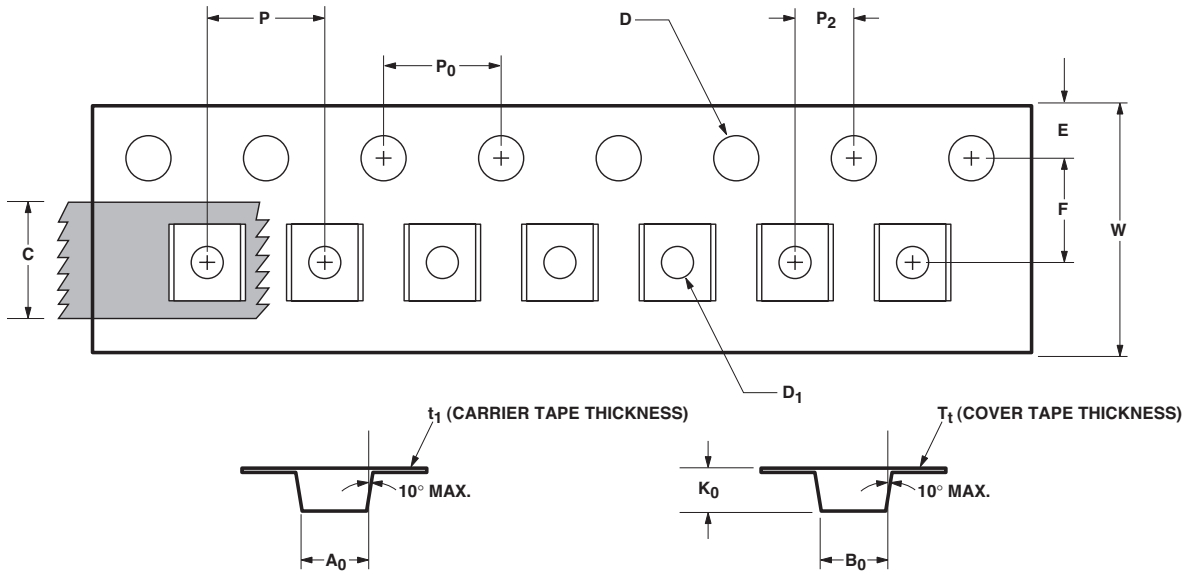
Device Orientation





Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.10	0.061 + 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.40 ± 0.10	0.205 + 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1985EN - May 22, 2010