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## Features

- Very high speed: 45 ns
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 1.5  $\mu$ A
  - Maximum standby current: 12  $\mu$ A
- Ultra low active power
  - Typical active current: 7 mA at  $f = 1$  MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball FBGA package. For Pb-free 48-pin TSOP I package, refer to [CY62167EV30](#) data sheet.

## Functional Description

The CY62168EV30 is a high performance CMOS static RAM organized as 2M words by 8-bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $CE_2$ ) LOW). The input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when: the device is deselected (Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $CE_2$ ) LOW), outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress (Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 ( $CE_2$ ) HIGH and  $\overline{WE}$  LOW).

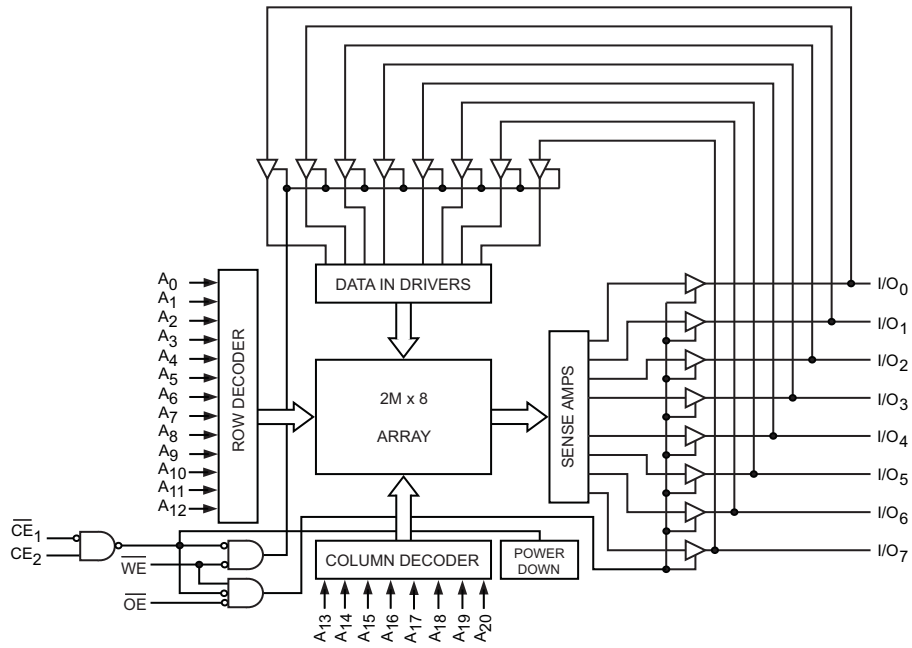
Write to the device by taking Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 ( $CE_2$ ) HIGH and the Write Enable ( $\overline{WE}$ ) input LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{20}$ ).

Read from the device by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW and Chip Enable 2 ( $CE_2$ ) HIGH while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and  $\overline{WE}$  LOW). See the [Truth Table on page 12](#) for a complete description of read and write modes.

For a complete list of related documentation, click [here](#).

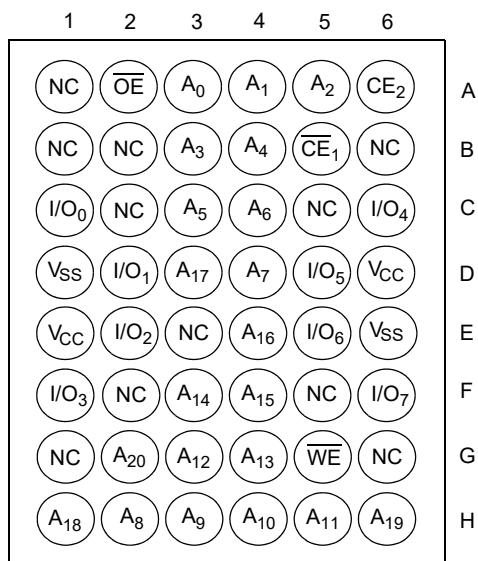
**Logic Block Diagram**



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## Pin Configuration

**Figure 1. 48-ball FBGA pinout (Top View)<sup>[1]</sup>**


## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA) <sup>[3]</sup>				Standby I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>max</sub>							
	Min	Typ <sup>[2]</sup>	Max		Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62168EV30LL	2.2	3.0	3.6	45	7	9	29	35	1.5	12

**Notes**

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
3. Refer to PIN#183401 for details of changes.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
to ground potential [4, 5] ..... -0.3 V to  $V_{CC(max)} + 0.3$  V

DC voltage applied to outputs  
in high Z state [4, 5] ..... -0.3 V to  $V_{CC(max)} + 0.3$  V

DC input voltage<sup>[4, 5]</sup> ..... -0.3 V to  $V_{CC(max)} + 0.3$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ ) <sup>[6]</sup>	$V_{CC}$ <sup>[7]</sup>
Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## DC Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	CY62168EV30-45			Unit	
			Min	Typ <sup>[8]</sup>	Max		
$V_{OH}$	Output HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1$ mA	2.0	–	–	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0$ mA	2.4	–	–	
$V_{OL}$	Output LOW voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1$ mA	–	–	0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = 2.1$ mA	–	–	0.4	
$V_{IH}$	Input HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8	–	$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2	–	$V_{CC} + 0.3$	
$V_{IL}$	Input LOW voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3	–	0.6	V
		$2.7 \leq V_{CC} \leq 3.6$		-0.3	–	0.8	
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	–	+1	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output disabled		-1	–	+1	
$I_{CC}$ <sup>[9]</sup>	$V_{CC}$ operating supply current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6$ V, $I_{OUT} = 0$ mA, CMOS level	–	29	35	mA
		$f = 1$ MHz		–	7	9	
$I_{SB1}$ <sup>[10]</sup>	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{MAX}$ (address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ )		–	1.5	12	$\mu$ A
$I_{SB2}$ <sup>[10]</sup>	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.6$ V		–	1.5	12	$\mu$ A

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- $T_A$  is the "Instant-On" case temperature.
- Full device AC operation assumes a 100  $\mu$ s ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu$ s wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Refer to PIN#183401 for details of changes.
- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

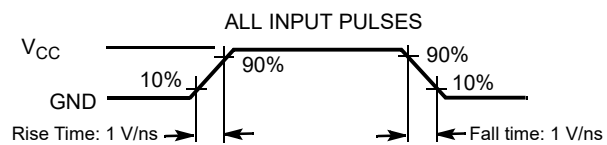
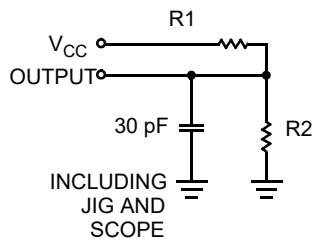
Parameter <sup>[11, 12]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

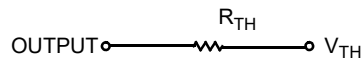
Parameter <sup>[11, 12]</sup>	Description	Test Conditions	48-ball FBGA	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.5	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		15.75	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R <sub>1</sub>	16600	1103	Ω
R <sub>2</sub>	15400	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.2	1.75	V

### Notes

11. Tested initially and after any design or process changes that may affect these parameters.
12. Refer to PIN#183401 for details of changes.

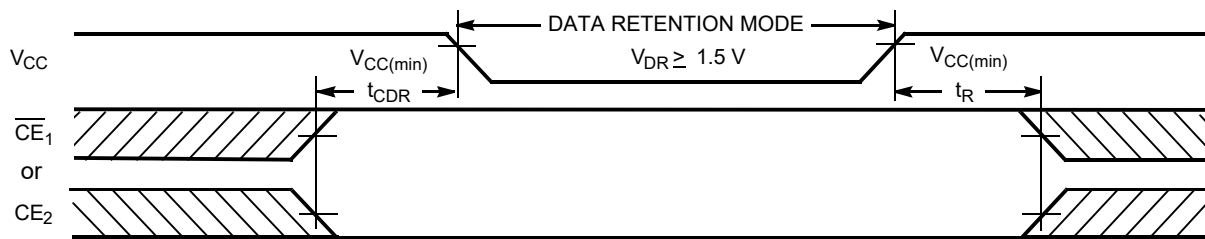
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[13]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	3.6	V
$I_{CCDR}$ <sup>[14]</sup>	Data retention current	$V_{CC} = 1.5\text{ V}$ $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	10	$\mu\text{A}$
$t_{CDR}$ <sup>[15]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[16]</sup>	Operation recovery time		45	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}(typ)$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
14. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(min) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(min) \geq 100\text{ }\mu\text{s}$ .



## Switching Characteristics

Over the Operating Range

Parameter <sup>[17]</sup>	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	45	–	ns
$t_{AA}$	Address to data valid	–	45	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	–	45	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low $Z^{[18]}$	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high $Z^{[18, 19]}$	–	18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to low $Z^{[18]}$	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to high $Z^{[18, 19]}$	–	18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to power-down	–	45	ns
<b>Write Cycle<sup>[20, 21]</sup></b>				
$t_{WC}$	Write cycle time	45	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	35	–	ns
$t_{AW}$	Address setup to write end	35	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high $Z^{[18, 19]}$	–	18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low $Z^{[18]}$	10	–	ns

### Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in [Figure 2 on page 6](#).

18. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

19.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

21. The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled)<sup>[22, 23]</sup>

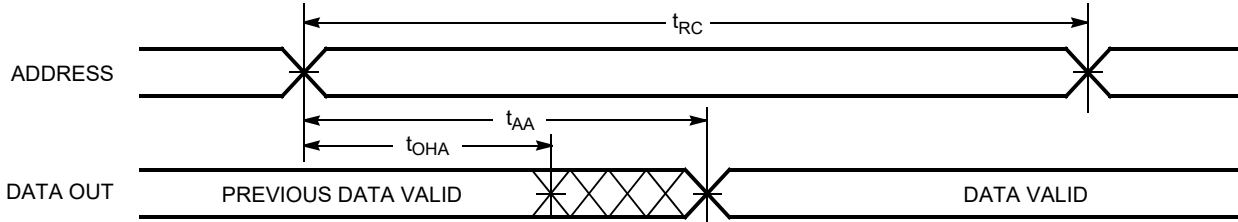
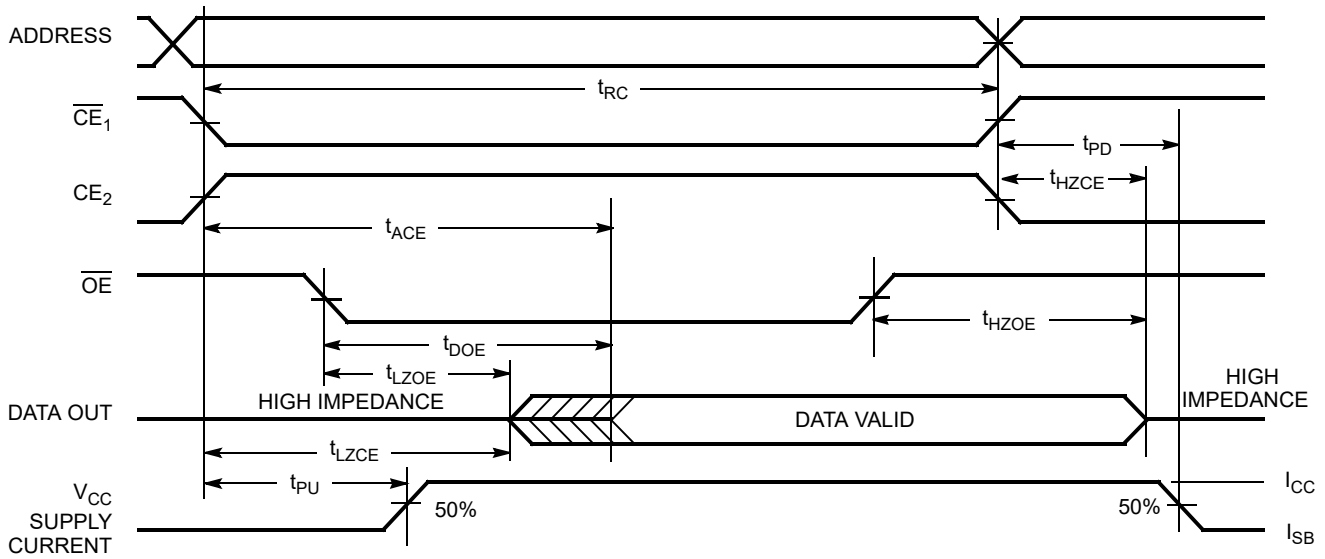


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[23, 24]</sup>



**Notes**

- 22. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 23.  $\overline{WE}$  is HIGH for read cycle.
- 24. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[25, 26, 27]</sup>

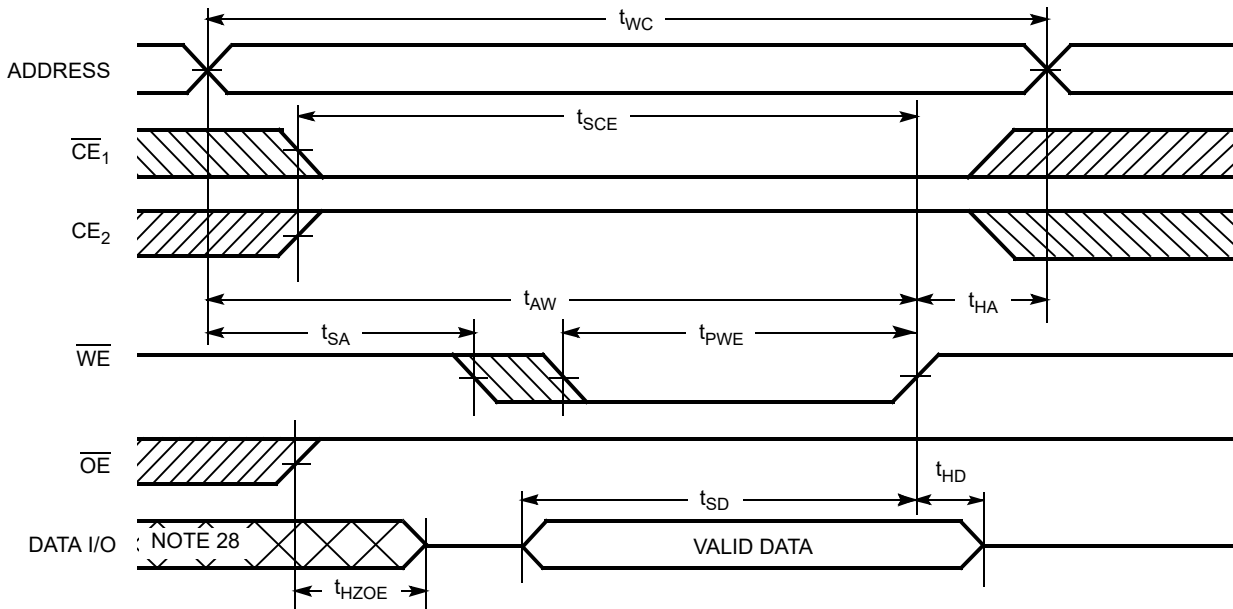
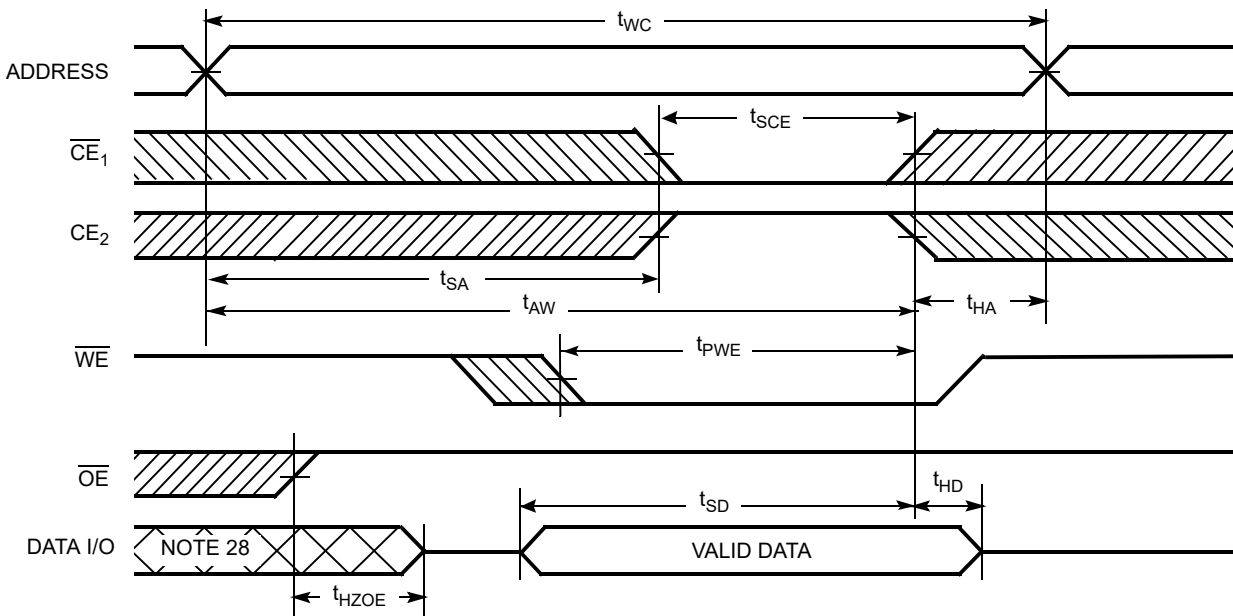


Figure 7. Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[25, 26, 27]</sup>

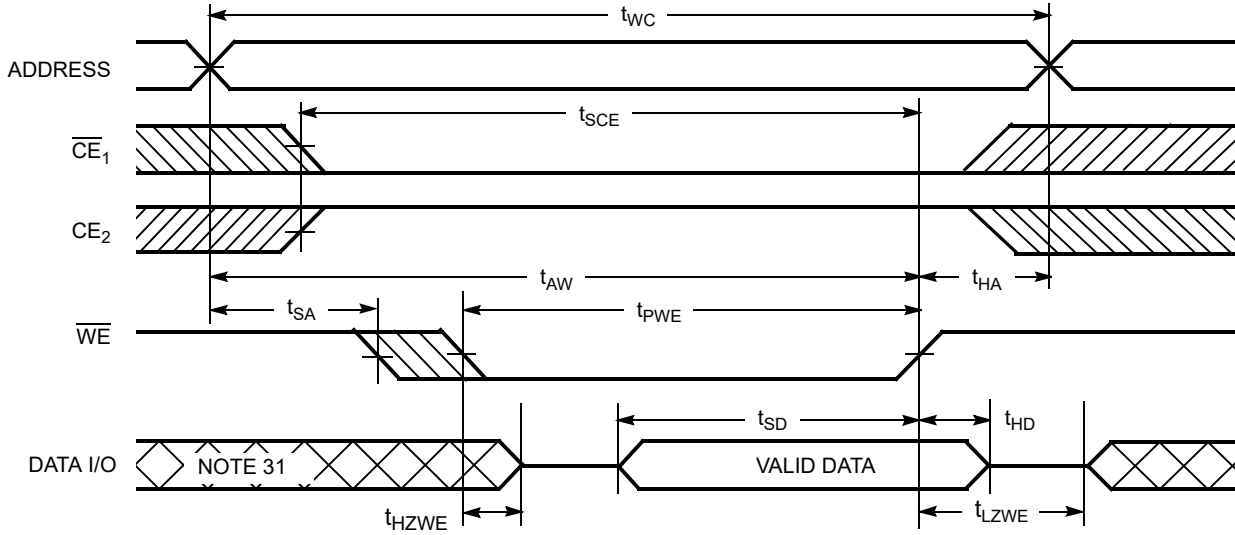


Notes

- 25. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 27. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 28. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[29, 30]</sup>



Notes

- 29. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 30. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .
- 31. During this period the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H	X <sup>[32]</sup>	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
X <sup>[32]</sup>	L	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data out ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	Data in ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )

**Note**

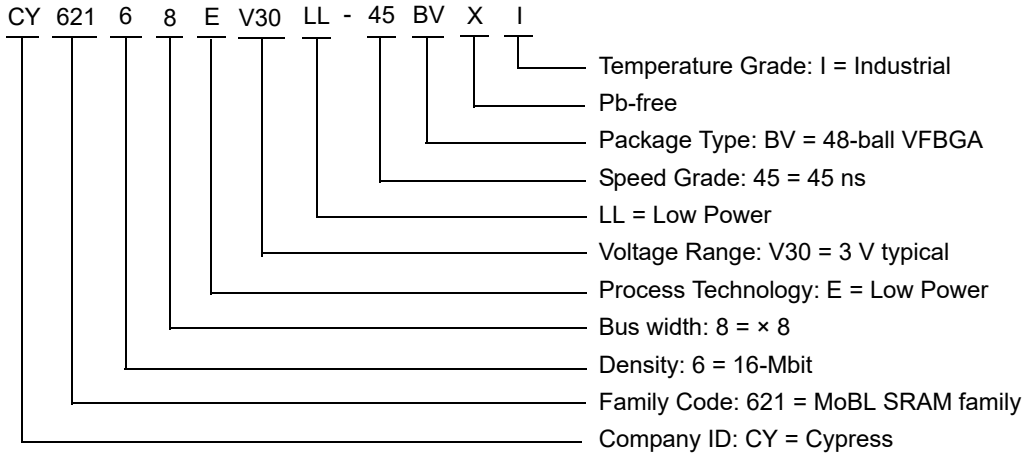
<sup>32</sup>. The 'X' (Do not care) state for the chip enables in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

The below table lists the CY62168EV30 MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>.

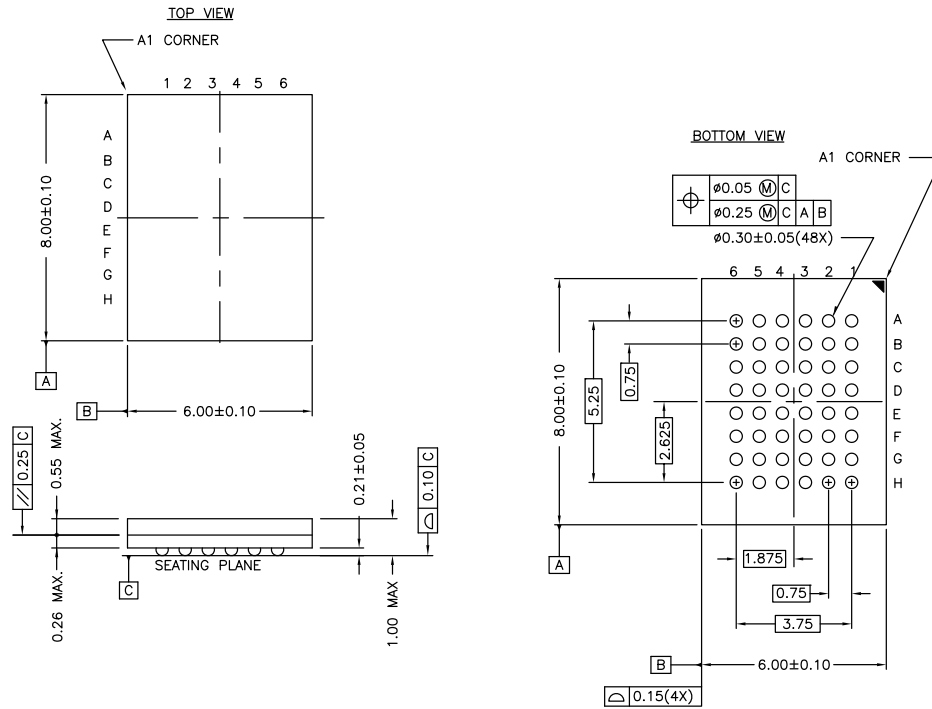
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62168EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

## Ordering Code Definitions



Package Diagram

Figure 9. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

## Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

## Document Conventions

### Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



**Document History Page**

Document Title: CY62168EV30 MoBL <sup>®</sup> , 16-Mbit (2M × 8) Static RAM Document Number: 001-07721				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	457686	NXR	04/26/2006	New data sheet.
*A	464509	NXR	05/26/2006	Removed TSOP I package related information in all instances across the document. Updated <a href="#">Features</a> : Added Note "For 48-pin TSOP I pin configuration and ordering information, please refer to CY62167EV30 Data sheet." and referred the same note in 48-pin TSOP I package. Updated <a href="#">DC Electrical Characteristics</a> : Changed typical value of I <sub>CC</sub> parameter from 15 mA to 22 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed maximum value of I <sub>CC</sub> parameter from 40 mA to 25 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed typical value of I <sub>CC</sub> parameter from 2 mA to 2.2 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I <sub>SB2</sub> parameter from 1.3 μA to 1.5 μA. Updated <a href="#">Data Retention Characteristics</a> : Changed maximum value of I <sub>CCDR</sub> parameter from 8.5 μA to 8 μA. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : Removed spec 51-85183 Rev. *A.
*B	1138883	VKN	06/08/2007	Changed status from Preliminary to Final. Updated <a href="#">Features</a> : Removed Note "For 48-pin TSOP I pin configuration and ordering information, please refer to CY62167EV30 Data sheet." and its reference. Added "For Pb-free 48-pin TSOP I package, refer to CY62167EV30 data sheet." in the last bullet point. Updated <a href="#">DC Electrical Characteristics</a> : Changed typical value of I <sub>CC</sub> parameter from 22 mA to 25 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed maximum value of I <sub>CC</sub> parameter from 25 mA to 30 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed maximum value of I <sub>CC</sub> parameter from 2.8 mA to 4.0 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I <sub>SB1</sub> and I <sub>SB2</sub> parameters from 8.5 μA to 12 μA. Added Note 10 and referred the same note in I <sub>SB1</sub> and I <sub>SB2</sub> parameters. Updated <a href="#">Data Retention Characteristics</a> : Changed maximum value of I <sub>CCDR</sub> parameter from 8 μA to 10 μA. Added Note 14 and referred the same note in I <sub>CCDR</sub> parameter.
*C	2934385	VKN	06/03/2010	Updated <a href="#">Functional Description</a> : Corrected typo. Updated <a href="#">Operating Range</a> : Updated Note 7 (Changed wait time after VCC stabilization from 100 μs to 200 μs). Updated <a href="#">Truth Table</a> : Added Note 32 and referred the same note in "CE <sub>1</sub> " column and "CE <sub>2</sub> " column. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *D to *E. Updated to new template.

**Document History Page** (continued)

Document Title: CY62168EV30 MoBL®, 16-Mbit (2M × 8) Static RAM				
Document Number: 001-07721				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	3279426	RAME	06/10/2011	Updated <a href="#">Functional Description</a> : Removed Note "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines." in page 1 and its reference. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*E	4100078	VINI	08/20/2013	Updated <a href="#">Switching Characteristics</a> : Added Note 17 and referred the same note in "Parameter" column. Updated <a href="#">Package Diagram</a> : spec 51-85150 – Changed revision from *F to *H. Updated to new template.
*F	4126351	NILE	09/17/2013	Updated <a href="#">Maximum Ratings</a> : Updated Note 4.
*G	4434949	VINI	07/09/2014	Updated <a href="#">Switching Characteristics</a> : Added Note 21 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 30 and referred the same note in <a href="#">Figure 8</a> . Completing Sunset Review.
*H	4576406	VINI	01/16/2015	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated to new template.
*I	4841338	VINI	07/20/2015	Updated <a href="#">Maximum Ratings</a> : Referred Notes 4, 5 in "Supply Voltage to Ground Potential". Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Changed value of $\Theta_{JA}$ parameter from 55 °C/W to 52.3 °C/W corresponding to 48-ball FBGA package. Changed value of $\Theta_{JC}$ parameter from 16 °C/W to 7.91 °C/W corresponding to 48-ball FBGA package. Completing Sunset Review.
*J	6284382	NILE	08/17/2018	Updated <a href="#">Maximum Ratings</a> : Changed value of Latch-Up current from "> 200 mA" to "> 140 mA". Updated <a href="#">DC Electrical Characteristics</a> : Changed typical value of $I_{CC}$ parameter from 25 mA to 29 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed maximum value of $I_{CC}$ parameter from 30 mA to 35 mA corresponding to Test Condition "f = f <sub>max</sub> ". Changed typical value of $I_{CC}$ parameter from 2.2 mA to 7 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of $I_{CC}$ parameter from 4 mA to 9 mA corresponding to Test Condition "f = 1 MHz". Updated <a href="#">Capacitance</a> : Changed value of $C_{IN}$ parameter from 8 pF to 10 pF. Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Changed value of $\Theta_{JA}$ parameter from 52.3 °C/W to 31.50 °C/W corresponding to 48-ball FBGA package. Changed value of $\Theta_{JC}$ parameter from 7.91 °C/W to 15.75 °C/W corresponding to 48-ball FBGA package.

**Document History Page** (continued)

Document Title: CY62168EV30 MoBL®, 16-Mbit (2M × 8) Static RAM				
Document Number: 001-07721				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*J (cont.)	6284382	NILE	08/17/2018	Updated <a href="#">Switching Characteristics</a> : Removed Note "In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note <a href="#">AN66311</a> . However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production." and its reference in "Parameter" column. Updated to new template. Completing Sunset Review.
*K	6294735	NILE	08/29/2018	Added Footnotes 3 and 12, referring to PIN# 183401 associated with the changes in Rev *J of this document.

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