

## FEATURES

- White LED driver based on an inductive boost controller
- Wide input voltage range: 4.5 V to 40 V
- Adaptive output voltage to minimize power dissipation
- Adjustable operating frequency: 200 kHz to 1.2 MHz
- Programmable UVLO
- Programmable soft start time for boost converter
- Programmable external MOSFET switching rising/falling time
- Drives up to 4 LED current sinks with internal MOSFETs
- Brightness control with PWM input
- Adjustable LED current: 40 mA to 200 mA
- Headroom control to maximize efficiency
- LED dimming frequency: up to 25 kHz
- PWM dimming at 300 Hz: 1000:1
- Open-drain fault indicator
- LED open and LED short fault protection
- Thermal shutdown
- Undervoltage lockout (UVLO)
- 24-lead, 4 mm × 4 mm LFCSP

## APPLICATIONS

- LCD monitor and TV LED backlights
- Industrial lighting

## GENERAL DESCRIPTION

The **ADD5211** is a four-string, white LED driver for backlight applications based on high efficiency, current mode, step-up converter technology. The boost controller drives an external MOSFET switch for step-up regulation from an input voltage of 4.5 V to 40 V and a pin adjustable operating frequency from 200 kHz to 1.2 MHz. An adjustable UVLO function is implemented to reduce input current during power-off.

The **ADD5211** provides four regulated current sinks for uniform brightness intensity. Each current sink can be driven from 40 mA to 200 mA; the LED driving current is pin adjustable using an external resistor. With an input PWM interface, the **ADD5211** drives up to four parallel strings of multiple series connected LEDs.

Additional features include LED short protection, LED open protection, boost output short protection, overvoltage protection, cycle-by-cycle current limit, and thermal shutdown for both the IC and the LED array. An open-drain fault output is also included. A programmable soft start is implemented to reduce inrush current during startup.

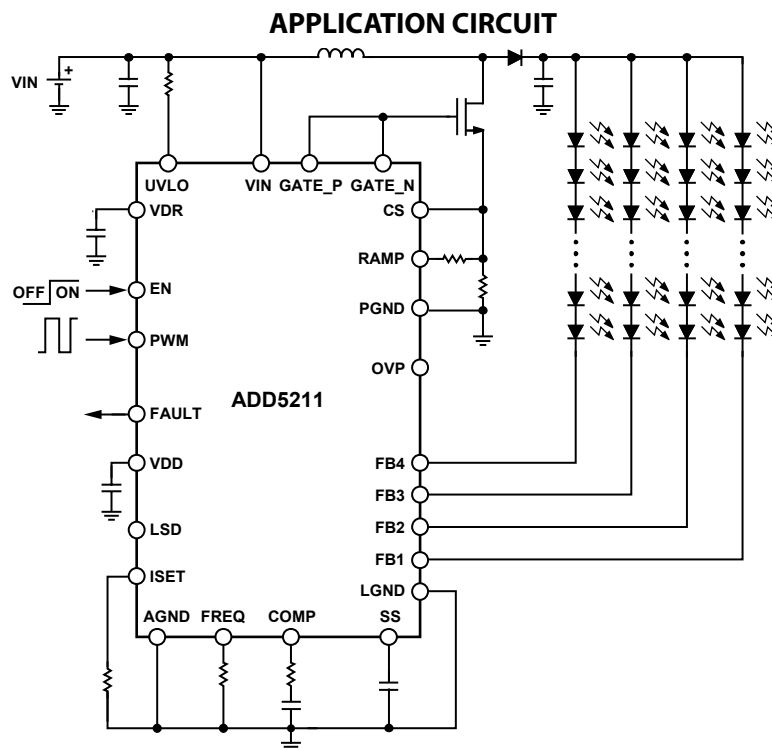


Figure 1.

Rev. A

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**REVISION HISTORY**

**10/2017—Rev. 0 to Rev. A**

Changed CP-24-7 to CP-24-15 .....	Throughout
Change to Operating Temperature Range ( $T_A$ ), Table 4 .....	6
Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	18

**10/2013—Revision 0: Initial Version**

# DETAILED FUNCTIONAL BLOCK DIAGRAM

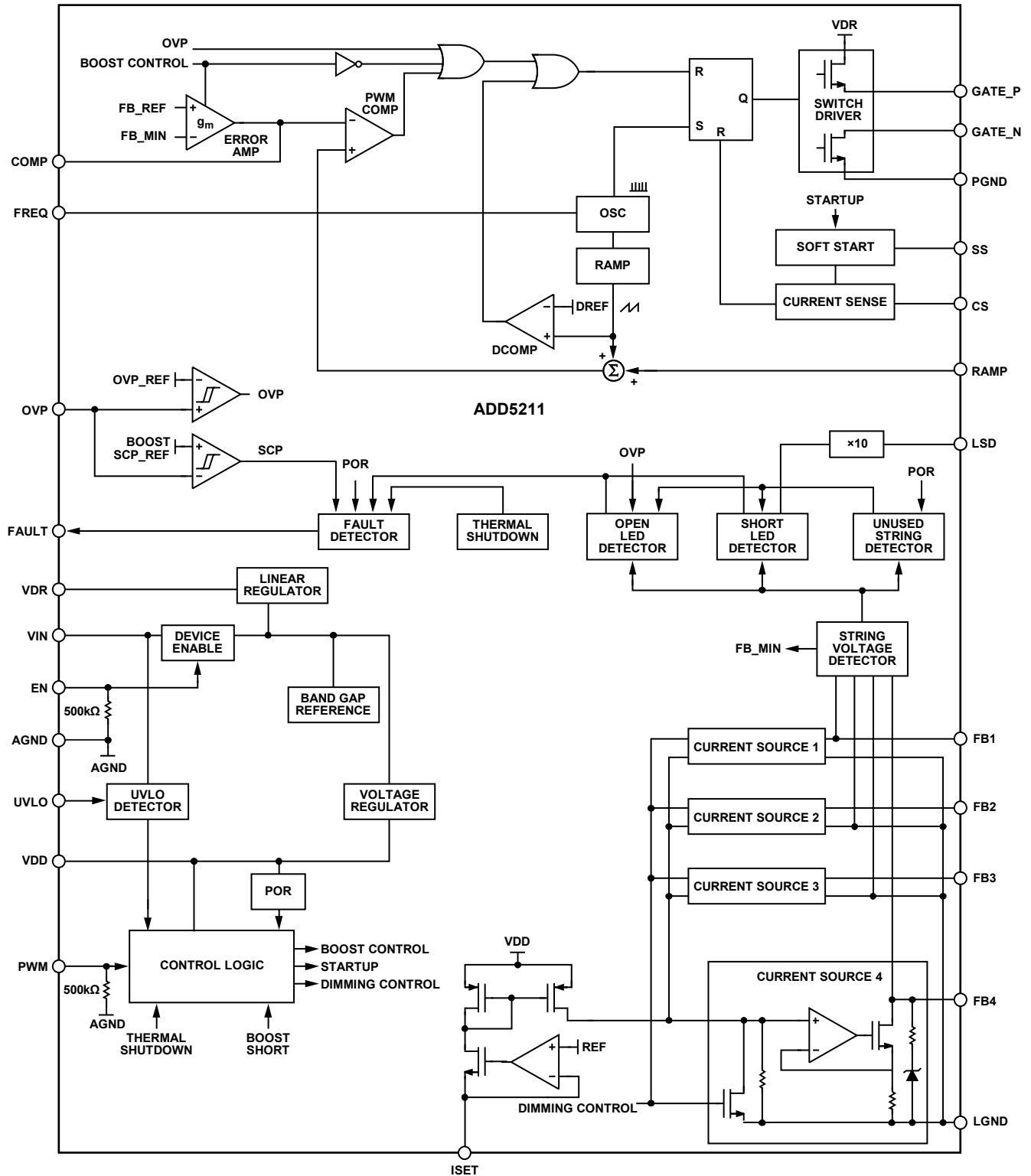


Figure 2.

10555-002

## SPECIFICATIONS

$V_{IN} = 12\text{ V}$ ,  $EN = 3.3\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ .

### GENERAL SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SUPPLY</b>						
Input Voltage Range	$V_{IN}$		4.5		40	V
Quiescent Current	$I_Q$			2.8	6	mA
Shutdown Supply Current	$I_{SD}$	$EN = 0\text{ V}$			1	$\mu\text{A}$
$V_{IN}$ Rising Threshold	$V_{UVLOR\_VIN}$	Minimum $V_{IN}$ for startup		4	4.3	V
$V_{IN}$ Falling Threshold	$V_{UVLOF\_VIN}$		3.2	3.65		V
<b>VDR REGULATOR</b>						
Regulated Output	$V_{VDR\_REG}$		4.75	5.1	5.45	V
Dropout Voltage	$V_{VDR\_DROP}$	$V_{IN} = 4.5\text{ V}$		350	580	mV
<b>VDD REGULATOR</b>						
Regulated Output	$V_{VDD\_REG}$		3.0	3.3	3.6	V
<b>PWM INPUT</b>						
Input High Voltage	$V_{PWM\_HIGH}$		2.2		8	V
Input Low Voltage	$V_{PWM\_LOW}$				0.8	V
PWM Input Current		PWM = 5 V		11	30	$\mu\text{A}$
PWM High to LED Turn-On Delay <sup>1</sup>				1.6		$\mu\text{s}$
PWM Low to LED Turn-Off Delay <sup>1</sup>				0.8		$\mu\text{s}$
<b>EN CONTROL</b>						
EN Voltage High			2.2		17	V
EN Voltage Low					0.8	V
EN Pin Input Current		$EN = 5\text{ V}$		13	30	$\mu\text{A}$
<b>UNDERVOLTAGE LOCKOUT</b>						
UVLO Threshold (Rising)			1.10	1.19	1.27	V
UVLO Hysteresis				100		mV
<b>FAULT</b>						
Sink Resistance				40	100	$\Omega$
Fault Pin Leakage Current					1.5	$\mu\text{A}$
<b>LED SHORT DETECTION</b>						
LED Short Detection Enable Threshold	$V_{LSD}$		2.2	2.5	VDD	V
LED Short Gain		LSD = 1.0 V	7.5	10	13	
LED Short Gain Control Range <sup>1</sup>			0.3		2.0	V
<b>LED FAULT DETECTION DELAY<sup>1</sup></b>						
LED Open Fault Delay				5		$\mu\text{s}$
LED Short Fault Delay				15		$\mu\text{s}$
<b>OVERVOLTAGE PROTECTION</b>						
Overshoot Threshold (Rising)	OVP_REF		2.3	2.5	2.7	V
Overshoot Hysteresis	OVP_HYS			100		mV
Overshoot Pin Leakage Current					200	nA
Output Short-Circuit Threshold (Falling)	$V_{SCPF}$			100		mV
Output Short-Circuit Recovery (Rising)	$V_{SCPR}$			150		mV
<b>THERMAL SHUTDOWN<sup>1</sup></b>						
Thermal Shutdown Threshold	$T_{SD}$			150		$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{SDHYS}$			25		$^\circ\text{C}$

<sup>1</sup> Guaranteed by design.

## STEP-UP SWITCHING CONTROLLER SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BOOST FREQUENCY OSCILLATOR						
Switching Frequency Range			200		1200	kHz
Switching Frequency	$f_{SW}$	$R_{FREQ} = 50 \text{ k}\Omega$	280	360	430	kHz
PWM COMPARATOR						
Maximum Duty Cycle		$R_{FREQ} = 50 \text{ k}\Omega$	89	94	98	%
Leading Edge Blanking Time				145		ns
CURRENT SENSE LIMIT COMPARATOR						
Current-Limit Threshold	$CS_{LIMIT}$	Independent of duty cycle	275	345	400	mV
SLOPE COMPENSATION						
Peak Slope Compensation Ramp		$R_{RAMP} = 5 \text{ k}\Omega$		45		$\mu\text{A}$
ERROR AMPLIFIER						
Transconductance	$g_m$			570		$\mu\text{A}/\text{V}$
Output Resistance	$R$			72		$\text{M}\Omega$
COMP Sink Current				400		$\mu\text{A}$
COMP Source Current				400		$\mu\text{A}$
MOSFET DRIVER						
Source Voltage		$8 \text{ V} < V_{IN} < 40 \text{ V}$		5.1		V
Gate On Resistance	$R_{DS\_GATE\_P}$			5.8		$\Omega$
Gate Off Resistance	$R_{DS\_GATE\_N}$			2.4		$\Omega$
Rising Time	$t_R$	$C = 1 \text{ nF}$		26		ns
Falling Time	$t_F$	$C = 1 \text{ nF}$		21		ns
SOFT START						
Soft Start Pin Current	$I_{SS}$			2.1		$\mu\text{A}$

## LED CURRENT REGULATION SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SINK						
Current Sink Range	$I_{LED}$		40		200	mA
Current Sink	$I_{LED100}$	$R_{SET} = 15 \text{ k}\Omega, T_A = 25^\circ\text{C}$	98		102	mA
String-to-String Tolerance <sup>1</sup>	$\Delta I_{FB100}$	$R_{SET} = 15 \text{ k}\Omega, T_A = 25^\circ\text{C}$		0.45	2.5	%
Current Accuracy <sup>2</sup>	$\Delta I_{LED100}$	$R_{SET} = 15 \text{ k}\Omega, T_A = 25^\circ\text{C}$			2.0	%
Minimum Headroom Voltage	$V_{HR}$	$R_{SET} = 15 \text{ k}\Omega, T_A = 25^\circ\text{C}$	0.4	0.55	0.85	V
Off Current	$I_{OFF}$	$V_{FB} = 40 \text{ V}, EN = 0 \text{ V}$			1.5	$\mu\text{A}$
Off State Clamping Current	$I_{CLAMP}$	$V_{FB} = 55 \text{ V}, EN = 0 \text{ V}$	4	20	80	$\mu\text{A}$

<sup>1</sup> String-to-string tolerance is the greatest delta between FBx currents with respect to the average of the FBx currents.

$$\Delta I_{FB100} = \text{Max} \left( \left| \frac{I_{FB100(\text{MAX})} - I_{LED100}}{I_{LED100}} \times 100\% \right|, \left| \frac{I_{FB100(\text{MIN})} - I_{LED100}}{I_{LED100}} \times 100\% \right| \right)$$

where  $I_{FB100}$  is the LED current of each string.

<sup>2</sup> Current accuracy is the delta between average current,  $I_{LED100}$ , and 100 mA with respect to 100 mA.

$$\Delta I_{LED100} = \left| \frac{I_{LED100} - 100 \text{ mA}}{100 \text{ mA}} \right| \times 100\%$$

$$\text{where } I_{LED100} = \frac{I_{FB1} + I_{FB2} + I_{FB3} + I_{FB4}}{4}$$

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VIN, UVLO	-0.3 V to +45 V
FB1, FB2, FB3, FB4	-0.3 V to +55 V
EN	-0.3 V to +17 V
PWM, FAULT	-0.3 V to +8 V
VDR, GATE_N, GATE_P	-0.3 V to +7 V
COMP, CS, FREQ, ISET, LSD, OVP, RAMP	-0.3 V to +3.6 V
SS	-0.3 V to VDD
AGND, PGND, LGND	-0.3 V to +0.3 V
Maximum Junction Temperature (T <sub>J</sub> max)	150°C
Operating Temperature Range (T <sub>A</sub> )	-40°C to +125°C
Storage Temperature Range (T <sub>S</sub> )	-65°C to +150°C
Reflow Peak Temperature (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

θ<sub>JA</sub> is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

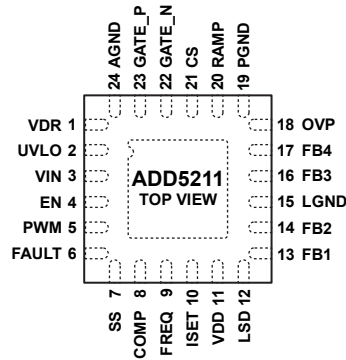
Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
24-Lead LFCSP	40.5	3.8	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. CONNECT THE EXPOSED PAD TO GROUND.

Figure 3. Pin Configuration

10656-003

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDR	Switching MOSFET Gate Driver Supply Pin. Bypass VDR to AGND with a 1 $\mu$ F bypass capacitor.
2	UVLO	Input Undervoltage Lockout. Set the start-up and shutdown input voltage level by connecting this pin to the input voltage with a resistor divider.
3	VIN	Supply Input Pin. Bypass VIN to AGND with a 0.1 $\mu$ F bypass capacitor.
4	EN	Shutdown Control Pin for PWM Input Operation Mode.
5	PWM	PWM Signal Input.
6	FAULT	Open-Drain Fault Output.
7	SS	Soft Start Pin.
8	COMP	Compensation for the Boost Converter. A capacitor and a resistor are connected in series between ground and this pin for stable operation.
9	FREQ	Frequency Select. A resistor from this pin to ground sets the boost switching frequency from 200 kHz to 1.2 MHz.
10	ISET	Full-Scale LED Current Set Pin. A resistor from this pin to ground sets the LED current up to 200 mA.
11	VDD	Internal Linear Regulator Output. This regulator provides power to the <a href="#">ADD5211</a> . Bypass VDD to AGND with a 1 $\mu$ F bypass capacitor.
12	LSD	LED Short Voltage Level Setting Pin. To disable LED short protection, connect this pin to VDD.
13	FB1	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect FB1 to LGND.
14	FB2	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect FB2 to LGND.
15	LGND	LED Current Sink Ground.
16	FB3	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect FB3 to LGND.
17	FB4	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect FB4 to LGND.
18	OVP	Overvoltage Protection. The boost converter output is connected to this pin with a resistor divider.
19	PGND	Power Ground.
20	RAMP	Ramp Compensation Pin.
21	CS	Current Sense Input. Allows the current sensing to control the boost converter and to limit the switching current.
22	GATE_N	Switching MOSFET Gate Low Driving Pin.
23	GATE_P	Switching MOSFET Gate High Driving Pin.
24	AGND	Analog Ground.
	EP	Exposed Pad. Connect the exposed pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

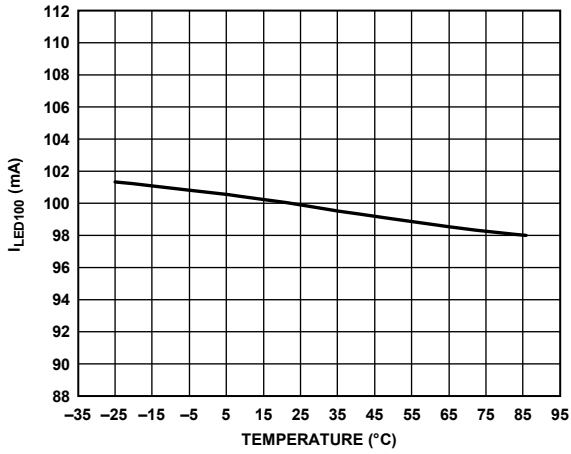


Figure 4. I<sub>LED100</sub> vs. Temperature

10555-004

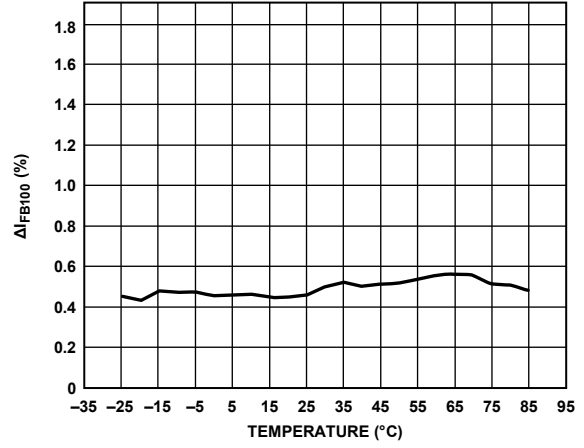


Figure 7. ΔI<sub>FB100</sub> vs. Temperature

10555-005

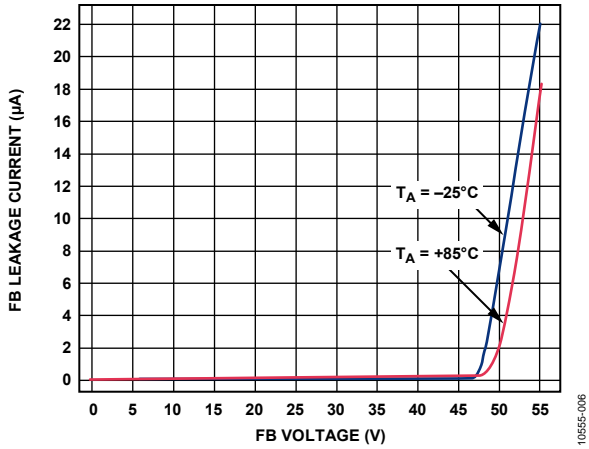


Figure 5. FB Leakage Current vs. FB Voltage

10555-006

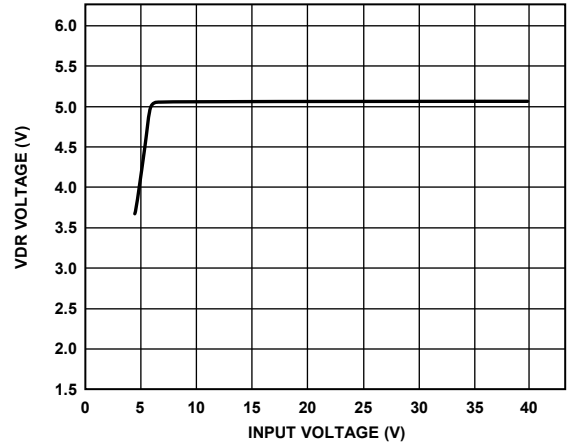


Figure 8. VDR Voltage vs. Input Voltage

10555-007

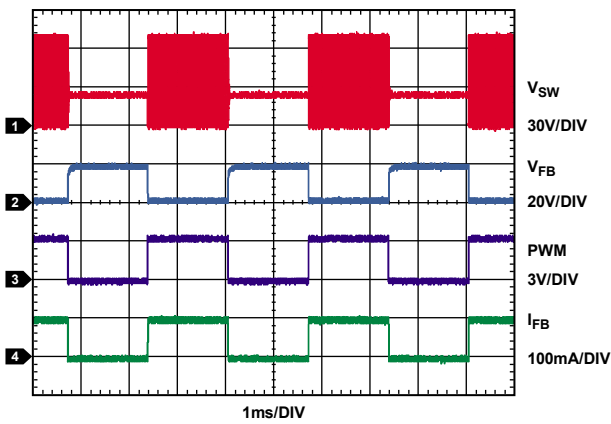


Figure 6. PWM Dimming Waveform, PWM Duty Cycle = 50%

10555-008

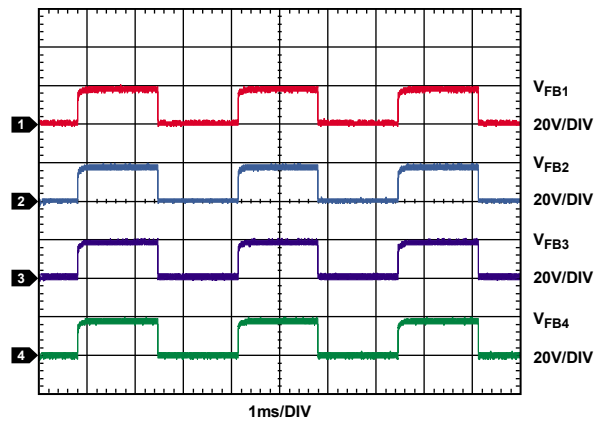


Figure 9. FB1 to FB4 Waveforms, PWM Duty Cycle = 50%

10555-009



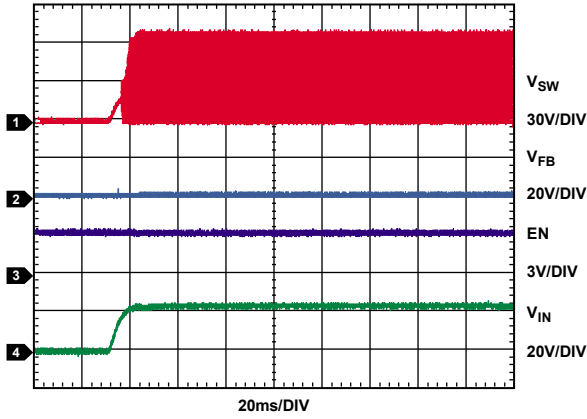


Figure 10. Startup (Brightness = 100%, EN Is High,  $V_{IN}$  Goes from Low to High)

10555-010

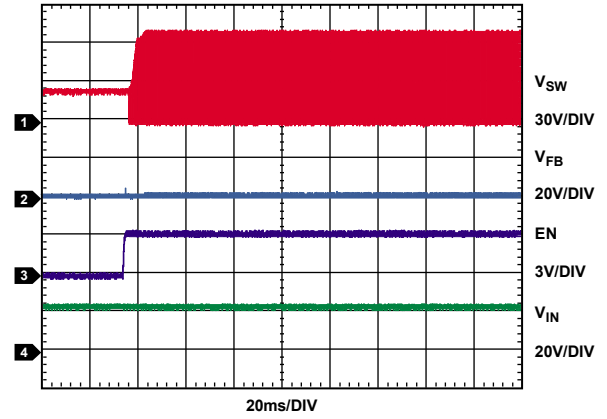


Figure 13. Startup (Brightness = 100%,  $V_{IN}$  Is High, EN Goes from Low to High)

10555-011

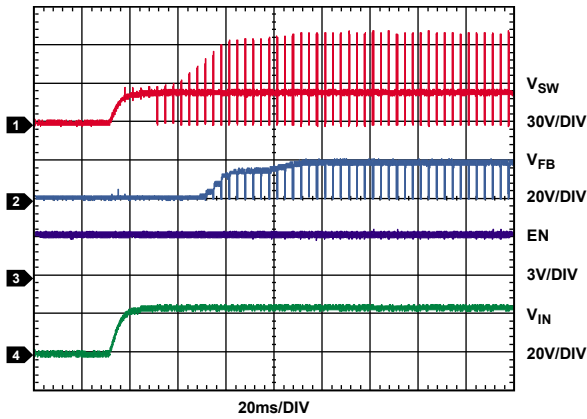


Figure 11. Startup (Brightness = 10%, EN Is High,  $V_{IN}$  Goes from Low to High)

10555-012

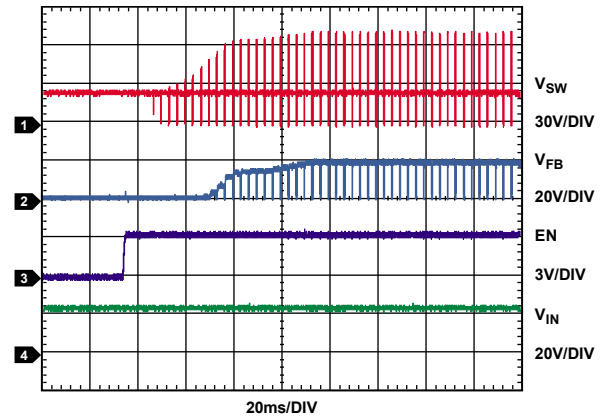


Figure 14. Startup (Brightness = 10%,  $V_{IN}$  Is High, EN Goes from Low to High)

10555-013

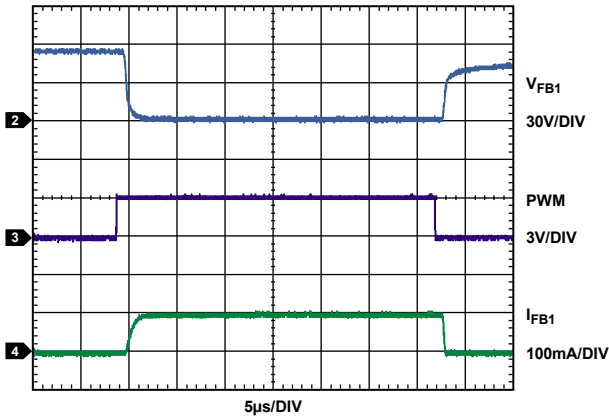


Figure 12. LED Current Rising and Falling Waveform

10555-014

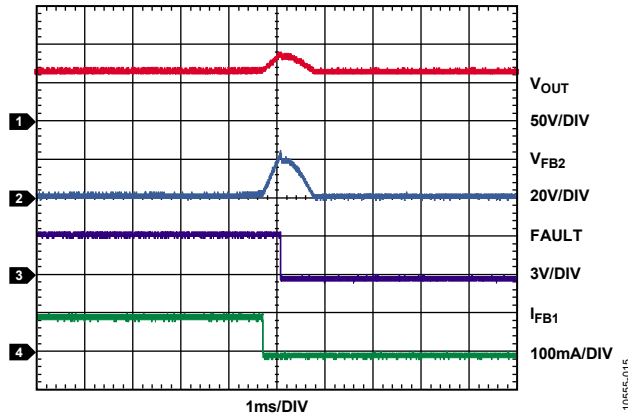


Figure 15. LED Open Protection (Open LED on FB2)

10555-015

## THEORY OF OPERATION

The **ADD5211** uses a PWM boost controller to generate the minimum output voltage required to drive the LED string at the programmed LED current. The current mode control architecture allows a fast transient response while maintaining a stable output voltage. The boost converter provides power to the LED strings, and the four current sinks control the LED current with dynamic headroom control to improve efficiency.

### CURRENT MODE, STEP-UP SWITCHING CONTROLLER

The **ADD5211** is a current mode, PWM boost controller that operates at a fixed switching frequency from 200 kHz to 1.2 MHz. The switching frequency is set by an external resistor connected from the **FREQ** pin to **AGND**. The minimum headroom voltage—which is monitored at the **FB1**, **FB2**, **FB3**, and **FB4** pins—is compared with the internal reference voltage by the internal transconductance error amplifier to create an error current at **COMP**. A resistor and capacitor connected from the **COMP** pin to **AGND** convert the error current to an error voltage.

At the beginning of the switching cycle, the MOSFET is turned on and the inductor current ramps up. The MOSFET current is measured and converted to a voltage using the current sense resistor ( $R_{CS}$ ) and is added to the stabilizing slope compensation ramp from the ramp resistor ( $R_{RAMP}$ ). The resulting voltage sum passes through the current sense amplifier to generate the current sense voltage. Under light loads, the converter can also operate in discontinuous mode with pulse skip modulation to maintain output voltage regulation.

The current mode regulation system of the **ADD5211** allows fast transient responses while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from **COMP** to **AGND**, the regulator response can be optimized for a wide range of input voltages, output voltages, and load currents.

#### Input Voltage

The **ADD5211** can be powered directly from the **VIN** pin, which accepts a voltage from 4.5 V to 40 V. The voltage on the **VIN** pin must exceed  $V_{UVLOR\_VIN}$  (4.0 V typical) for startup. The **ADD5211** has two linear regulators: a 3.3 V linear regulator (**VDD**), which supplies power to the internal control circuitry, and a 5.1 V linear regulator (**VDR**), which supplies power to the internal **GATE\_P** and **GATE\_N** drivers.

#### UVLO Pin

The **UVLO** pin is used to control the **VIN** voltage at which the **ADD5211** starts up. This function is accomplished using a resistor divider between the input voltage and the **UVLO** pin, as shown in Figure 16.

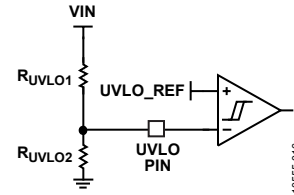


Figure 16. Undervoltage Lockout Circuit

The startup voltage, as determined by the resistor divider to the **UVLO** pin, can be calculated using the following equation:

$$V_{IN(START)} = (1.19 \text{ V}/R_{UVLO2}) \times (R_{UVLO1} + R_{UVLO2})$$

To start the device at the lowest possible **VIN** level, select an  $R_{UVLO1}$  value of 100 k $\Omega$  (or greater) and do not connect  $R_{UVLO2}$ . If **UVLO** is controlled from a separate voltage source, make sure that a 100 k $\Omega$  (or greater) resistor is in series between the voltage source and the **UVLO** pin.

#### Enable and Disable

To enable the **ADD5211**, the voltage at the **EN** pin must be higher than 2.2 V. To disable the **ADD5211**, the voltage at the **EN** pin must be lower than 0.8 V. An internal 500 k $\Omega$  resistor is connected between **EN** and **AGND**.

#### Internal 3.3 V Regulator (VDD)

The **ADD5211** contains a 3.3 V linear regulator (**VDD**) that is used to bias the internal control circuitry. The **VDD** regulator requires a 1  $\mu$ F bypass capacitor. Place this bypass capacitor between **VDD** and **AGND**, as close as possible to the **VDD** pin.

#### Internal 5.1 V Regulator (VDR)

The **ADD5211** contains a 5.1 V linear regulator (**VDR**) that is used to supply the MOSFET gate driver. The **VDR** regulator requires a 1  $\mu$ F bypass capacitor. Place this bypass capacitor between **VDR** and **AGND**, as close as possible to the **VDR** pin.

**Frequency**

The ADD5211 boost converter switching frequency ( $f_{sw}$ ) is user adjustable from 200 kHz to 1.2 MHz using an external resistor,  $R_{FREQ}$  (see Figure 17).

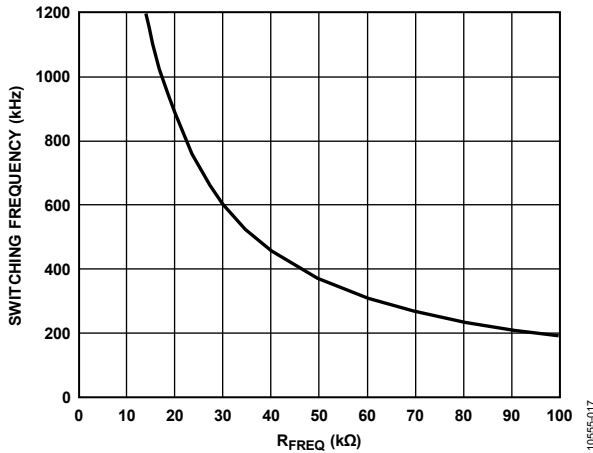


Figure 17. Switching Frequency vs.  $R_{FREQ}$

The following equation can also be used to calculate the typical switching frequency:

$$f_{sw} \text{ (kHz)} = \frac{19,000}{R_{FREQ} \text{ (k}\Omega)} - \frac{30,000}{(R_{FREQ} \text{ (k}\Omega))^2}$$

**Soft Start**

At startup, the voltage at the SS pin ramps up slowly by charging the soft start capacitor ( $C_{SS}$ ) from an internal 2.1  $\mu\text{A}$  (typical) current source. The peak inductor current follows the SS pin ramp to provide a controlled start-up profile. The soft start cycle is complete when the SS pin reaches its final value of 1.19 V (typical). A capacitor must always be connected to the SS pin. The soft start time can be calculated as follows:

$$t_{ss} = (C_{SS} \times 1.19 \text{ V}) / 2.1 \mu\text{A}$$

For a typical setup, a 27 nF soft start capacitor results in negligible input current overshoot at startup, making it suitable for most applications. However, if an unusually large output capacitor is used, a longer soft start period is required to prevent input inrush current and output voltage overshoot of the boost switching regulator. Conversely, if fast startup is required, the value of the soft start capacitor can be reduced to allow the boost output to start quickly, but allow greater peak switch current during startup and larger boost output overshoot.

**LED CURRENT REGULATION**

**Current Sink**

The ADD5211 contains four current sinks to provide accurate current sinking for each LED string. The current for each LED string is adjusted from 40 mA to 200 mA using an external resistor. Connect any unused FBx pins to LGND.

If the ADD5211 current sink voltage is greater than 45 V, a Zener diode and a 410 k $\Omega$  resistor in parallel with the current sink are activated (see Figure 18).

**Programming the LED Current**

As shown in Figure 22, the ADD5211 has an LED current set pin (ISET). A resistor ( $R_{SET}$ ) from the ISET pin to AGND adjusts the LED current from 40 mA to 200 mA. The LED current level can be set using the following equation:

$$I_{LED} \text{ (mA)} = 1500 / R_{SET} \text{ (k}\Omega)$$

The resulting minimum current sink voltage ( $FB\_REF$ ) is given by

$$FB\_REF = 0.23 + 0.0041 \times I_{LED} \text{ (mA)}$$

where 40 mA <  $I_{LED}$  < 200 mA.

If only one or two LED strings are used, it is most efficient to connect the FBx pins in parallel and adjust  $R_{SET}$  accordingly. This configuration gives the lowest  $V_{FB}$  operating voltage and improves efficiency. For example, to drive two LED strings at 100 mA, connect FB1 and FB2 together for one LED string, and connect FB3 and FB4 together for the other LED string. Then, set  $R_{SET}$  to 30.1 k $\Omega$  (50 mA). The minimum FBx voltage is now 0.44 V (typical) instead of 0.64 V (typical). See Figure 23 for an example of a two-string application.

**PWM Dimming Control**

The ADD5211 features LED brightness control using an external PWM signal applied at the PWM pin. A logic high signal on the PWM input enables the LED current sinks; a logic low signal disables them. If the PWM input remains low for 50 ms, the ADD5211 stops boost regulation and enters shutdown mode. If the PWM input returns high after the ADD5211 enters shutdown, the device initiates a new soft start sequence.

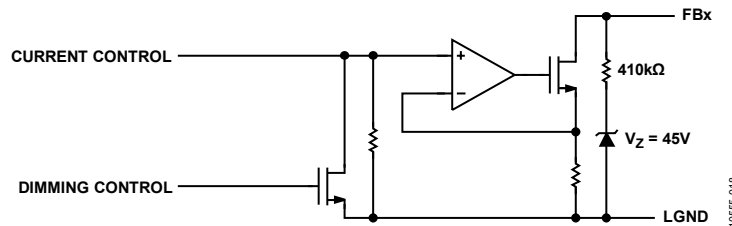


Figure 18. Current Sink Circuit

**FAULT PROTECTION**

Fault protections in the ADD5211 include boost output over-voltage protection, LED short protection, LED open protection, boost output short-circuit protection, and thermal shutdown. The FAULT pin provides an alert for some of these conditions (see Table 7).

**Boost Output Overvoltage Protection (OVP)**

The ADD5211 contains an overvoltage protection (OVP) circuit to prevent potential damage if the output voltage becomes excessive for any reason. OVP is implemented with a resistor divider from the boost output to the OVP pin. When the OVP pin voltage reaches 2.5 V (typical), the boost controller stops switching, which causes the output voltage and the OVP pin voltage to decrease. When the OVP pin voltage decreases below the OVP falling threshold (2.4 V typical), the boost converter resumes switching.

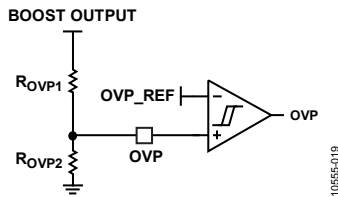


Figure 19. Boost Output Overvoltage Protection Circuit

The OVP threshold can be calculated using the following equation:

$$V_{OUT\_OVP} = (2.5 \text{ V}/R_{OVP2}) \times (R_{OVP1} + R_{OVP2})$$

**LED Short Protection**

If an LED in one of the LED strings is shorted, the voltage of the FBx pin that is connected to the faulty LED string increases to regulate the LED current. If this FBx pin reaches the LED short protection threshold (10× the voltage at the LSD pin) during normal operation, the ADD5211 disables the FBx pin that is connected to the shorted LED string and pulls down the FAULT pin.

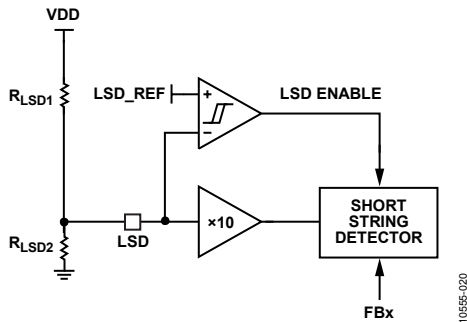


Figure 20. LED Short Protection Circuit

The LED short protection threshold can be calculated using the following equations:

$$V_{LSD} = (3.3 \text{ V}/(R_{LSD1} + R_{LSD2})) \times R_{LSD2}$$

$$V_{LED\_SHORT\_THRESHOLD} = 10 \times V_{LSD}$$

To disable LED short protection, set the voltage of the LSD pin to a value greater than 3 V, or connect the pin to the VDD pin.

**LED Open Protection**

The ADD5211 contains a headroom control circuit to minimize power loss at each current sink. Therefore, the minimum feedback voltage is achieved by regulating the output voltage of the boost converter. If any LED string is open circuit during normal operation, the current sink voltage ( $V_{FBx}$ ) will be near 0 V. LED open protection is activated if  $V_{FBx}$  is less than 100 mV (typical) and the boost converter output voltage reaches  $V_{OUT\_OVP}$ . The ADD5211 then disables the open LED string and pulls the open-drain fault indicator low. The remaining LED strings continue to operate normally. If all LED strings are open, the ADD5211 shuts down.

**Boost Output Short-Circuit Protection (SCP)**

The ADD5211 contains an SCP circuit to prevent boost converter damage if the Schottky diode becomes open or the boost converter output is shorted to ground for any reason. When the voltage on the OVP pin falls below 100 mV (typical), the boost converter stops switching until the OVP voltage rises to 150 mV (typical). The SCP function is disabled during boost converter soft start.

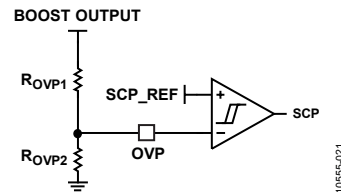


Figure 21. Boost Output Short-Circuit Protection Circuit

The boost output short-circuit protection threshold can be calculated using the following equation:

$$V_{OUT\_SCP} = (0.15 \text{ V}/R_{OVP2}) \times (R_{OVP1} + R_{OVP2})$$

**Thermal Shutdown (TSD)**

Thermal overload protection prevents excessive power dissipation from overheating and damaging the ADD5211. When the junction temperature ( $T_j$ ) exceeds 150°C (typical), a thermal sensor immediately activates the fault protection, which shuts down the device and allows it to cool. The device restarts when the junction temperature ( $T_j$ ) of the die falls below 125°C (typical).

Table 7. Fault Protection

Fault	Description	Boost Regulation Response	FAULT Pin State
Boost output overvoltage	$V_{OVP} > OVP\_REF$	Stop switching until $V_{OVP} < 2.4\text{ V}$ (typical)	Open
LED string short	$V_{FBx} > 10 \times V_{LSD}$ ; PWM pin is high	Shorted LED string disabled; other LED strings operate normally	Pulled down
LED string open	$V_{FBx} < 0.1\text{ V}$ ; $V_{OVP} > OVP\_REF$ ; PWM pin is high	Open LED string disabled; other LED strings operate normally	Pulled down
R <sub>SET</sub> short to AGND	R <sub>SET</sub> is shorted to AGND	ADD5211 shuts down; automatic restart if R <sub>SET</sub> returns to normal resistance range	Open
Boost output short	$V_{OVP} < 100\text{ mV}$ (typical) after soft start	ADD5211 shuts down; automatic restart if $V_{OVP}$ rises above 150 mV (typical)	Pulled down
Thermal shutdown	$T_J > 150^\circ\text{C}$ (typical)	ADD5211 shuts down; automatic restart after $T_J$ falls below 125°C (typical)	Pulled down

## APPLICATIONS INFORMATION

### LAYOUT GUIDELINES

To achieve high efficiency, good regulation, and stability, a good PCB layout is required. Use the following general guidelines when designing PCBs:

- Ensure that the high current loop from  $C_{IN}$  to L1 to Q1 to  $R_{CS}$  then back to the ground of  $C_{IN}$  is as short as possible.
- Ensure that the high current loop from  $C_{IN}$  to L1 to D1 to  $C_{OUT}$  then back to the ground of  $C_{IN}$  is as short as possible.
- Make high current traces as short and wide as possible.
- Keep nodes that are connected to L1, Q1, and D1 away from sensitive traces, such as COMP, to prevent coupling of the traces. If such traces must be run near each other, place a ground trace between the two as a shield.
- Place the compensation components as close as possible to the COMP pin.
- Use thermal vias and a thermal pad with the same dimensions as the exposed pad on the bottom of the package.

### Heat Sinking

When using a surface-mount power IC or external power switches, the PCB can often be used as the heat sink. This is achieved by using the copper area of the PCB to transfer heat from the device; maximizing this area optimizes thermal performance.

### BOOST COMPONENT SELECTION

#### Calculating the Peak Inductor Current and Duty Cycle

To select the optimal external components, the first step is to calculate the peak inductor current and maximum duty cycle. The peak inductor current is given by

$$I_{PK} = I_{L(AVG)} + (\Delta I_L / 2)$$

where:

$$\Delta I_L = (V_{IN} \times D) / (L \times f_{SW})$$

$$I_{L(AVG)} = (4 \times I_{LED}) / (\eta \times (1 - D))$$

$I_{LED}$  is the LED current per string.

$D$  is the duty cycle ( $D = (V_{OUT} - V_{IN}) / V_{OUT}$ ).

Verify that the worst-case duty cycle does not exceed the maximum allowed value (89%) given in Table 2. For the worst-case duty cycle, use the minimum  $V_{IN}$  and the maximum  $V_{OUT}$ . The maximum  $V_{OUT}$  is given by

$$V_{OUT\_MAX} = N \times V_{F\_MAX} + 1 \text{ V}$$

where:

$N$  is the number of LEDs per string.

$V_{F\_MAX}$  is the maximum LED forward voltage.

#### Selecting the Inductor

When selecting the inductor, consider these inductor properties: inductance, maximum saturation current, resistance (DCR), and physical size.

Choose an inductance such that  $\Delta I_L$  is 20% to 40% of  $I_{L(AVG)}$ .

$$L = \frac{V_{IN} \times D \times (1 - D)}{0.3 \times f_{SW} \times I_{OUT}}$$

where  $I_{OUT}$  is the total LED current through all the strings.

The saturation current is generally listed as the current at which the inductance is reduced by 30%. Ensure that this current is greater than the calculated peak inductor current.

Of the inductors that meet the required inductance and saturation current, choose one that provides the best trade-off between DCR and layout footprint for your application. The power dissipation due to the DCR of the inductor is given by

$$P_L = DCR \times I_{L(AVG)}^2$$

#### Selecting the Current Sense (CS) Resistor

To calculate the worst-case inductor peak current, use the maximum duty cycle, minimum inductance, and minimum switching frequency. Then select the current sense resistor ( $R_{CS}$ ) as follows:

$$R_{CS} = CS_{LIMIT(MIN)} / I_{PK(MAX)}$$

Ensure that the selected inductor can tolerate the maximum peak current given by this current sense resistor.

$$I_{PK(CS)} = CS_{LIMIT(MAX)} / R_{CS(MIN)}$$

The power dissipation from the sense resistor is given by

$$P_{RCS} = D \times R_{CS} \times I_{L(AVG)}^2$$

### Selecting the NMOS Switch

The external NMOS switch must have an adequate drain-to-source breakdown voltage ( $BV_{DSS}$ ) and rms current rating. The breakdown voltage rating should be at least

$$BV_{DSS} > V_{OUT(MAX)} + 10 V$$

The rms current rating should exceed the following:

$$I_{NMOS(RMS)} = I_{L(AVG)} \times \sqrt{D}$$

The power dissipation from the NMOS switch arises from two components:  $RDS_{ON}$  losses and switching losses. These losses can be calculated as follows:

$$P_{NMOS(RDSON)} = D \times RDS_{ON} \times I_{L(AVG)}^2$$

$$P_{NMOS(SW)} = 0.5 \times V_{OUT} \times I_{L(AVG)} \times (t_R + t_F) \times f_{SW}$$

The rise and fall times ( $t_R$  and  $t_F$ ) are a function of the strength of the ADD5211 gate drivers and the gate capacitance of the NMOS. Typical values are given in Table 2, but these times vary substantially for various power FETs. Therefore,  $t_R$  and  $t_F$  are best measured in the application.

### Selecting the Diode

The diode must be selected for a low forward voltage ( $V_F$ ) and fast switching times. Generally, a fast Schottky diode provides the best performance for the cost. Ensure that the breakdown voltage ( $V_D$ ) is greater than the maximum  $V_{OUT}$  plus some margin. Also ensure that the rated current of the diode is greater than the output current (total LED current). The power dissipation of the diode is as follows:

$$P_{DIODE} = V_F \times I_{OUT}$$

### Selecting $C_{OUT}$

To provide stability and reduce the output voltage ripple, particularly when PWM dimming of the LED currents is in effect, the output capacitance should be in the range of 4.7  $\mu F$  to 22  $\mu F$ .

### Boost Converter Loop Gain Calculations

The total closed-loop gain is given by  $G_{EA} \times G_P(s)$ .  $G_{EA}$  is the compensation gain.  $G_P(s)$  is the control to output gain.  $G_P(s)$  is the gain of the power stage and includes  $L$ ,  $C_{OUT}$ , and the PWM modulator. The  $G_P(s)$  gain is

$$G_P(s) =$$

$$A_{PS} \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_{ZESR}}\right) \times \left(1 - \frac{s}{2 \times \pi \times f_{RHP}}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_{LFP}}\right) \times \left(1 + \frac{s}{Q_n \times 2 \times \pi \times f_n} + \frac{s^2}{(2 \times \pi \times f_n)^2}\right)}$$

where  $A_{PS}$  is the dc gain and includes the PWM modulator gain, as follows:

$$A_{PS} = \frac{(1-D) \times V_{OUT} \times G_{CS}}{2 \times R_{CS} \times 4 \times I_{LED}}$$

The equation for  $G_P(s)$  shows that there are two zeros ( $f_{ZESR}$  and  $f_{RHP}$ ). The  $f_{ZESR}$  zero is formed by the ESR of the output capacitance. Because ceramic capacitors are used in this application, this value should be small and can usually be ignored. The zero is given by

$$f_{ZESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The right half plane zero ( $f_{RHP}$ ) is given by

$$f_{RHP} = \frac{V_{OUT}}{2 \times \pi \times L \times 4 \times I_{LED}} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2$$

This RHP zero results in a gain boost, but a phase drop. Because of its dependence on so many variables,  $f_{RHP}$  is extremely difficult to compensate for. Therefore, it is best to choose a loop crossover frequency well before the phase drop of this RHP zero is seen. Typically, this is an order of magnitude less than the frequency of the RHP zero.

$G_P(s)$  also gives two poles at  $f_{LFP}$  and  $f_n$ . The low frequency pole ( $f_{LFP}$ ) is formed by the output capacitance and is found at

$$f_{LFP} = \frac{4 \times I_{LED}}{\pi \times V_{OUT} \times C_{OUT}}$$

$f_n$  is the double pole formed by the current sense sampling action. It is always located at half the switching frequency.

The  $f_n$  double pole becomes unstable if  $Q_n$  (the quality factor) is not sufficiently damped.  $Q_n$  is damped by adding external ramp compensation ( $S_e$ ).

$$Q_n = \frac{1}{\pi \times \left(-D + 0.5 + (1-D) \times \frac{S_e}{S_n}\right)}$$

where:

$S_e$  is the external ramp compensation =  $75\% \times ((V_{OUT} - V_{IN})/L)$ .

$S_n$  is the inductor up slope =  $V_{IN}/L$ .

The external ramp compensation slope is usually set to a value from 50% to 75% of the inductor down slope as reflected across the sense resistor. Given the wide variation in parameters, it is best to stay closer to 75%.

$$R_{RAMP}(\Omega) = \frac{3}{4} \times \frac{R_{CS} \times (V_{OUT} - V_{IN})}{45 \mu A \times f_{SW} \times L}$$

**Compensation Component Selection**

To increase the crossover frequency (beyond the LFP frequency), some kind of phase boost is required. Because the **ADD5211** operates in current mode, only one zero is needed to counteract  $f_{LFP}$ . Therefore, a Type II compensator should be sufficient. This compensator (see Figure 2) has a gain,  $G_{EA}$ , that is expressed as follows:

$$G_{EA} = \frac{V_{FB}}{V_{OUT}} \times g_m \times \frac{s \times R_C \times C_C + 1}{s \times C_C}$$

$G_{EA}$  gives one zero and one pole at the origin, as follows:

$$f_{zEA} = 1/(2\pi \times R_C \times C_C)$$

$$f_{pEA} = 1/(2\pi \times R_O \times C_C)$$

where  $R_O$  is the output impedance of the error amplifier.

To boost the phase and increase the crossover frequency, place the compensation zero ( $f_{zEA}$ ) at or near the LFP pole. This placement gives the following equation for  $C_C$ :

$$C_C = \frac{V_{OUT} \times C_{OUT}}{2 \times R_C \times I_{OUT}}$$

These values may need to be adjusted experimentally to achieve satisfactory phase margin over all operating conditions and tolerances. Table 8 provides recommended values for switching frequencies of 360 kHz and 1 MHz.

**Table 8. Recommended Values for Compensation Components**

<b>f<sub>sw</sub> (kHz)</b>	<b>L (μH)</b>	<b>C<sub>OUT</sub> (μF)</b>	<b>R<sub>RAMP</sub> (kΩ)</b>	<b>R<sub>c</sub> (Ω)</b>	<b>C<sub>c</sub> (μF)</b>
360	33	10	6.81	100	2.2
1000	22	4.7	6.81	100	1.0



TYPICAL APPLICATION CIRCUITS

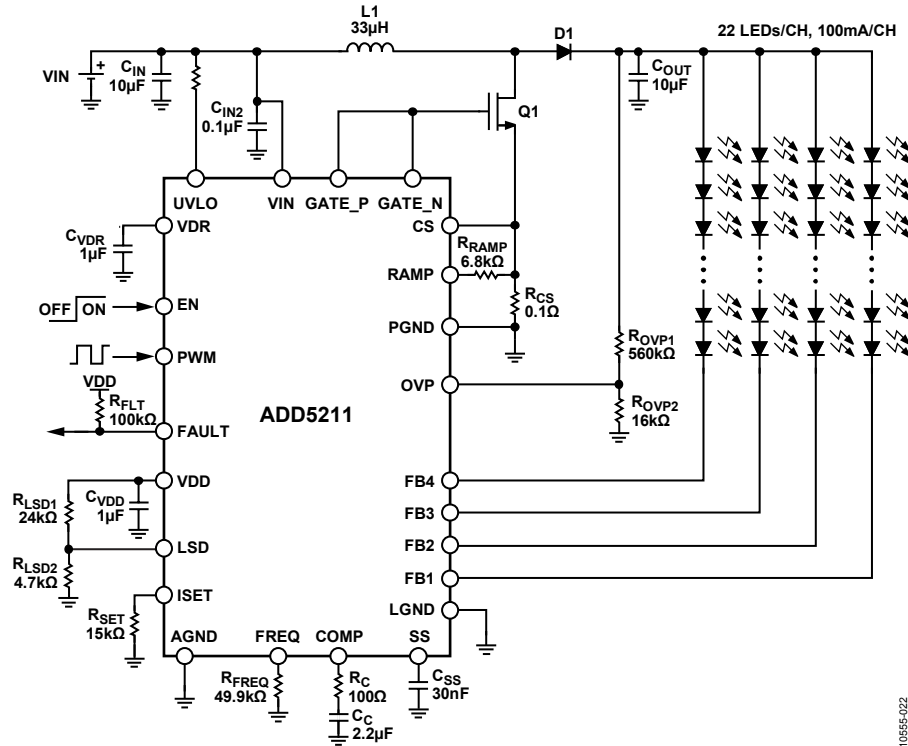


Figure 22. Typical Four-String Application Circuit

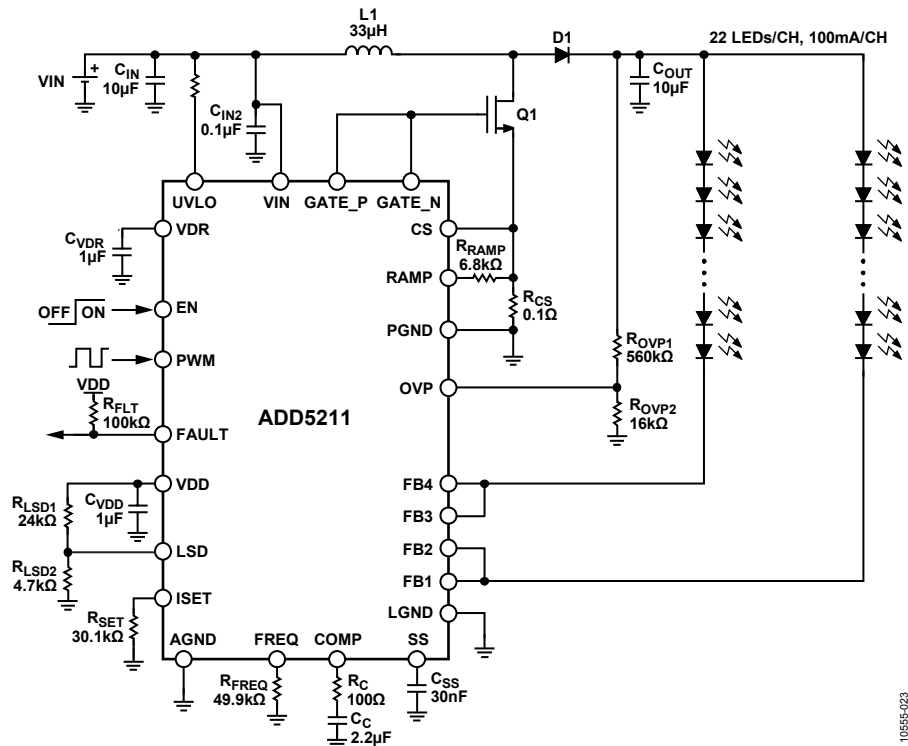
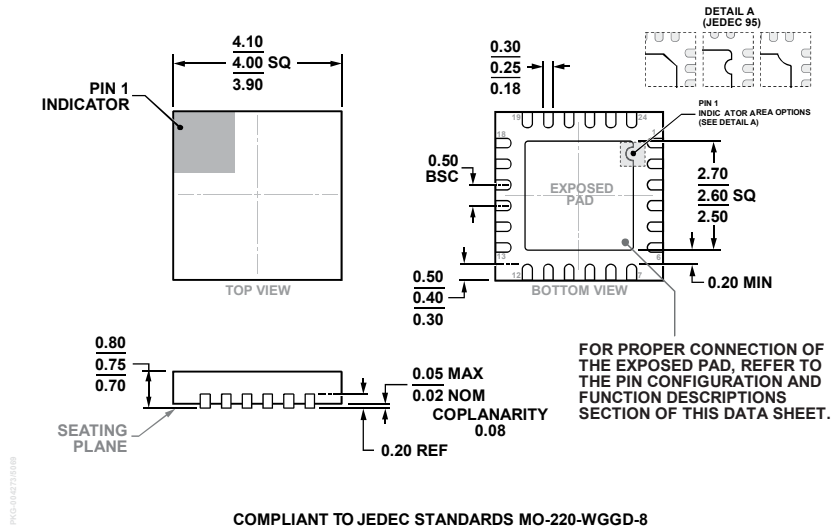


Figure 23. Typical Two-String Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8  
 Figure 24. 24-Lead Lead Frame Chip Scale Package [LFCSPP]  
 4 mm × 4 mm Body and 0.75 mm Package Height  
 (CP-24-15)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADD5211ACPZ-R7	-40°C to +125°C	24-Lead LFCSPP, 7" Tape and Reel	CP-24-15
ADD5211ACPZ-RL	-40°C to +125°C	24-Lead LFCSPP, 13" Tape and Reel	CP-24-15
ADD5211CP-EVALZ		Evaluation Board and LED Array	
AD5211EB-EVALZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**