

DESCRIPTION

The MPQ9842 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves 2A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input supply range. The switching frequency is programmable or can be synchronized to an external clock in the range of 350kHz to 2.5MHz. Synchronous operation and ultra-low 14μA sleep mode quiescent current provide high efficiency over the output current load range, allowing the MPQ9842 to be used in a variety of step-down applications in automotive input environments and battery-powered applications.

Peak-current-mode operation provides fast transient response and eases loop stabilization. The excellent low dropout performance allows the MPQ9842 to be used in high duty cycle applications.

Full protection features include over-current protection (OCP), short-circuit protection (SCP), and thermal shutdown. An open-drain power good (PG) signal indicates when the output is within 10% of its nominal voltage.

The MPQ9842 is available in a space-saving QFN-16 (3mmx4mm) package.

FEATURES

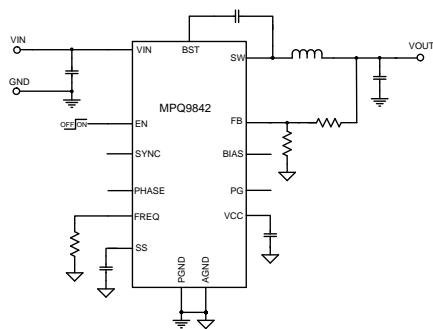
- 2μA Low Shutdown Supply Current
- 14μA No-Load Quiescent Current
- Internal 125mΩ High-Side and 55mΩ Low-Side MOSFET
- 350kHz to 2.5MHz Programmable Switching Frequency
- Power Good (PG) Output
- External Soft Start (SS)
- 80ns Minimum On Time
- Selectable Forced CCM and AAM
- Hiccup Over-Current Protection (OCP)
- AEC-Q100 Grade-1
- Available in a QFN-16 (3mmx4mm) Package

APPLICATIONS

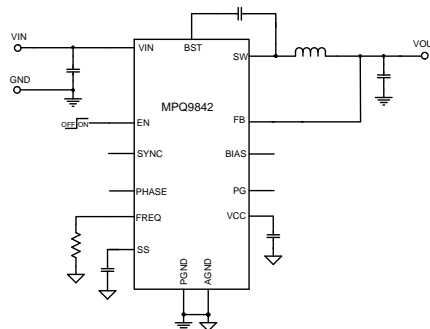
- Automotive Systems
- Industrial Power Systems

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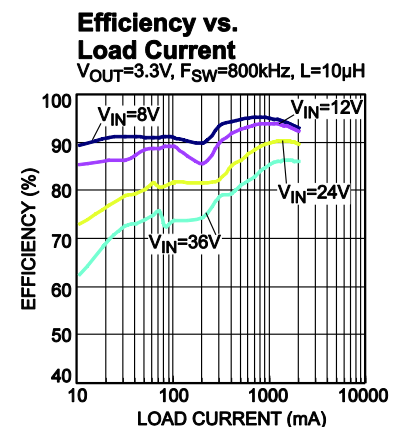
TYPICAL APPLICATION



Output Adjustable Version



Output Fixed Version



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ9842GL	QFN-16 (3mmx4mm)	See Below	1
MPQ9842GL-AEC1			
MPQ9842GLE-AEC1***			
MPQ9842GLE-33-AEC1***			
MPQ9842GLE-5-AEC1***			

* For Tape & Reel, add suffix -Z (e.g. MPQ9842GL-Z)

** Moisture Sensitivity Level Rating

***Wettable Flank

TOP MARKING (MPQ9842GL & MPQ9842GL-AEC1)

MPYW
9842
LLL

MP: MPS prefix
Y: Year code
WW Week code
9842 : First four digits of the part number
LLL: Lot number

TOP MARKING (MPQ9842GLE-AEC1)

MPYW
9842
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
9842: First four digits of the part number
LLL: Lot number
E: Wettable lead flank

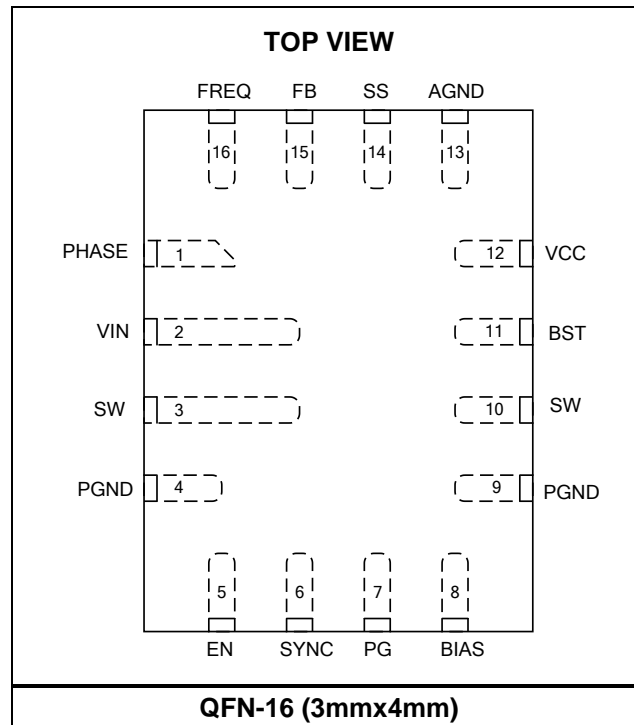
TOP MARKING (MPQ9842GLE-33-AEC1)**MPYW****9842****LLL****E33**

MP: MPS prefix
Y: Year code
W: Week code
9842: First four digits of the part number
LLL: Lot number
E: Wettable lead flank
33: 3.3V fixed output

TOP MARKING (MPQ9842GLE-5-AEC1)**MPYW****9842****LLL****E5**

MP: MPS prefix
Y: Year code
W: Week code
9842: First four digits of the part number
LLL: Lot number
E: Wettable lead flank
5: 5V fixed output

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (VIN).....	-0.3V to 40V
Switch voltage (V _{SW})	-0.3V to V _{IN} + 0.3V
BST voltage (V _{BST})	V _{SW} + 6.5V
EN voltage (V _{EN})	-0.3V to 40V
BIAS voltage (V _{BIAS})	-0.3V to 20V
All other pins	-0.3V to 6V
Continuous power dissipation (T _A = +25°C) ⁽²⁾⁽⁵⁾	
QFN-16 (3mmx4mm)	2.9W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM).....	±2kV
Charged device model (CDM).....	±750V

Recommended Operating Conditions

Supply voltage (VIN).....	3.3V to 36V
Operating junction temp. (T _J) ⁽³⁾	
.....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾ θ_{JA} θ_{JC}

QFN-16 (3mmx4mm)		
JESD51-7	48.....	11..°C/W ⁽⁴⁾
EV9842-L-00A	43.....	5..°C/W ⁽⁵⁾

NOTES:

- 1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX) = (T_J(MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Mission profiles requiring operation above 125°C T_J may be supported; contact MPS for details.
- 4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
- 5) Measured on an MPS EVB: 6.35cmx6.35cm, 2oz. copper thickness, 4-layer PCB, the value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $V_{EN} = 2V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}C$.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN quiescent current	I _Q	V _{FB} = 0.85V, no load, no switching, T _J = +25°C		14	21	μA
		V _{FB} = 0.85V, no load, no switching			29	
VIN shutdown current	I _{SHDN}	V _{EN} = 0V		2	6	μA
VIN under-voltage lockout threshold rising	INUV _{RISING}		2.4	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	INUV _{HYS}			150		mV
EN rising threshold	V _{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V _{EN_HYS}			120		mV
Feedback reference voltage	V _{REF}		784	800	816	mV
		T _J = +25°C	792	800	808	mV
Output voltage accuracy for the MPQ9842-33			3217	3300	3383	mV
		T _J = +25°C	3250	3300	3350	mV
Output voltage accuracy for the MPQ9842-5			4875	5000	5125	mV
		T _J = +25°C	4925	5000	5075	mV
HS switch on resistance	R _{ON_HS}	V _{BST} - V _{SW} = 5V		125	165	mΩ
LS switch on resistance	R _{ON_LS}			55	85	mΩ
Switching frequency	f _{SW}	R _{FREQ} = 180kΩ or from sync clock	400	475	550	kHz
		R _{FREQ} = 82kΩ or from sync clock	850	1000	1150	kHz
		R _{FREQ} = 27kΩ or from sync clock	2250	2500	2750	kHz
Minimum on time ⁽⁶⁾	t _{ON_MIN}			80		ns
SYNC input low voltage	V _{SYNC_LOW}				0.4	V
SYNC input high voltage	V _{SYNC_HIGH}		1.8			V
Current limit	I _{LIMIT_HS}	Duty cycle = 40%	4.0	5.0	6.8	A
Low-side valley current limit	I _{LIMIT_LS}	V _{OUT} = 3.3V, L = 4.7μH	2.5	3.8	5.1	A
ZCD current	I _{ZCD}			0.1		A
Reverse current limit	I _{LIMIT_REVERSE}			3		A
Switch leakage current	I _{SW_LKG}			0.01	1	μA
Soft-start current	I _{SS}	V _{SS} = 0.8V	5	10	15	μA
VCC regulator	V _{CC}			5		V
VCC load regulation		I _{CC} = 5mA			3.5	%
Thermal shutdown ⁽⁶⁾	T _{SD}			170		°C
Thermal shutdown hysteresis ⁽⁶⁾	T _{SD_HYS}			20		°C

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{EN} = 2V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}C$.

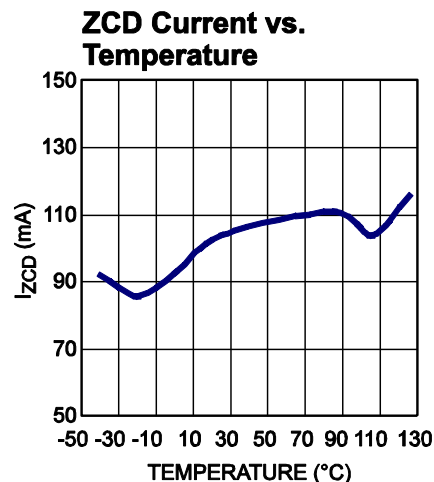
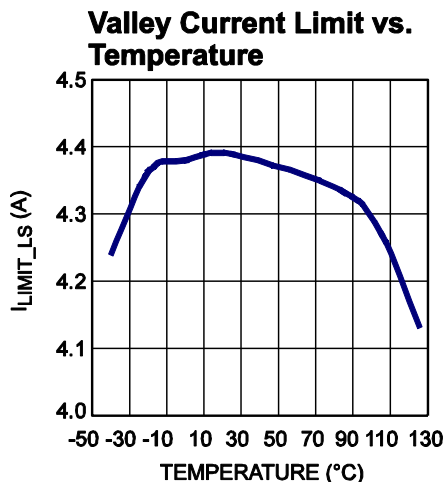
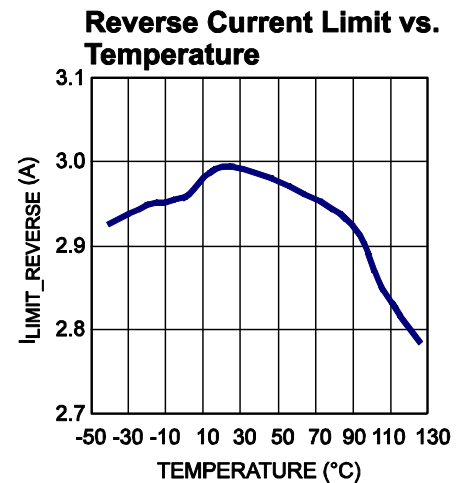
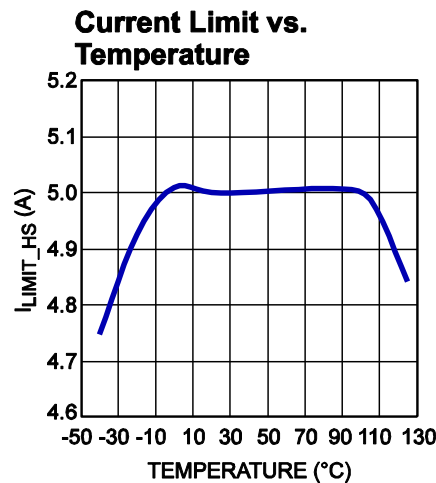
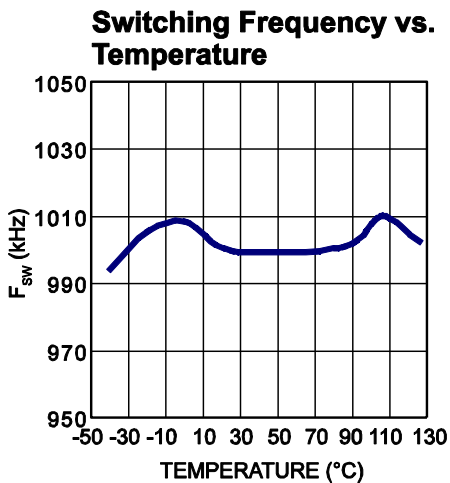
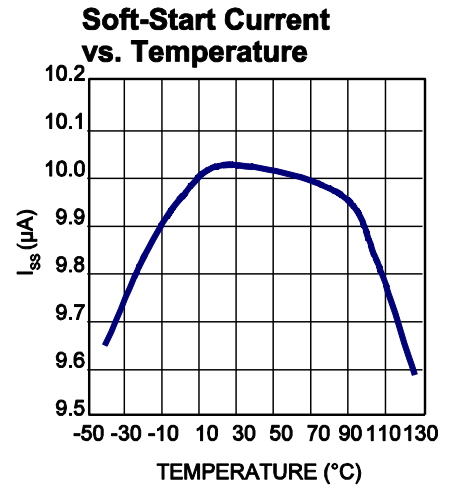
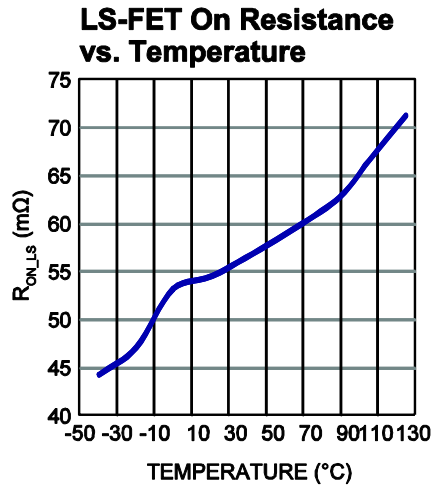
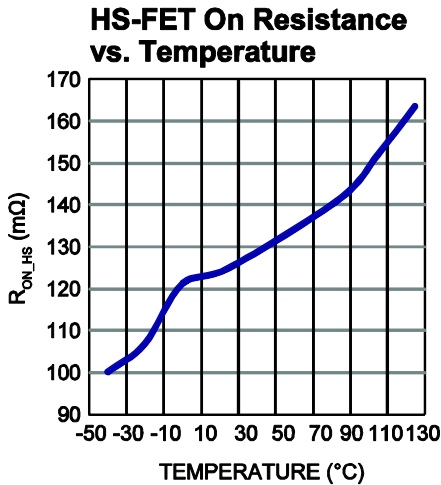
Parameter	Symbol	Condition	Min	Typ	Max	Units
PG rising threshold (V_{FB}/V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	
PG falling threshold (V_{FB}/V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	
PG deglitch timer	$t_{PG_DEGLITCH}$	PG from low to high		30		μs
		PG from high to low		50		μs
PG output voltage low	V_{PG_LOW}	$I_{SINK} = 2mA$		0.2	0.4	V

NOTE:

6) Not tested in production, guaranteed by design and characterization.

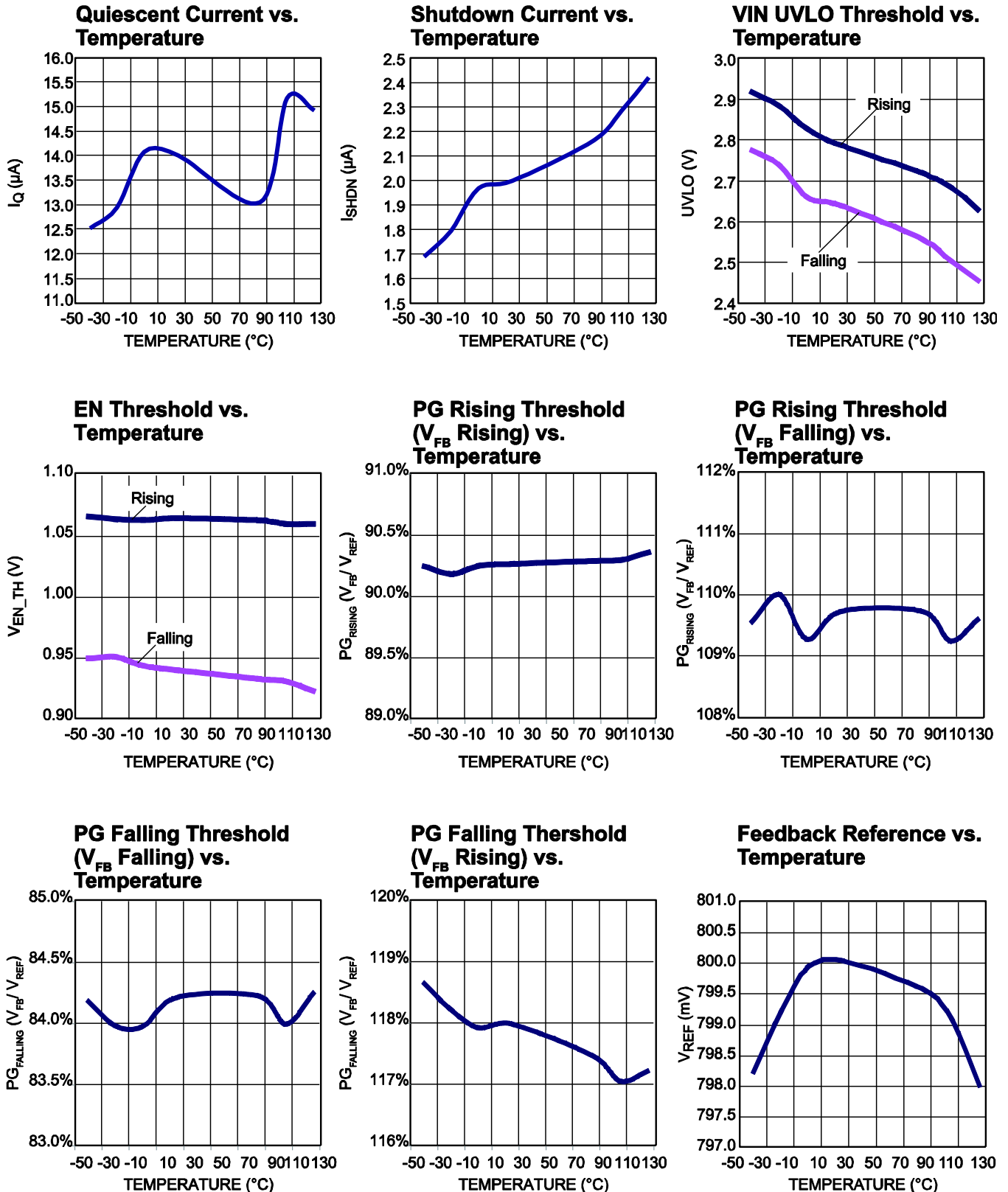
TYPICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

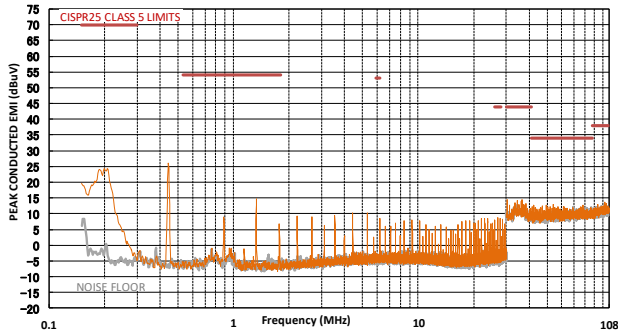
VIN = 12V, TJ = -40°C to +125°C, unless otherwise noted.



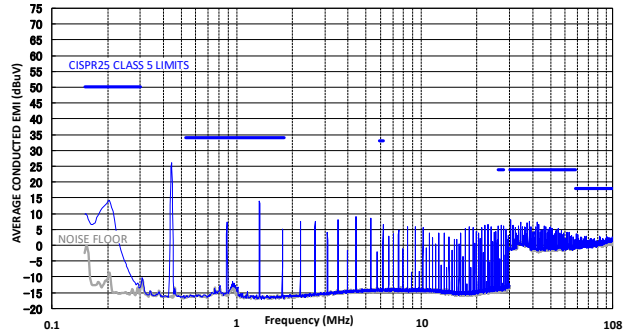
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, I_o=2A, L = 4.7μH, f_{sw} = 450kHz, with EMI filters, T_A = +25°C, unless otherwise noted. (7)

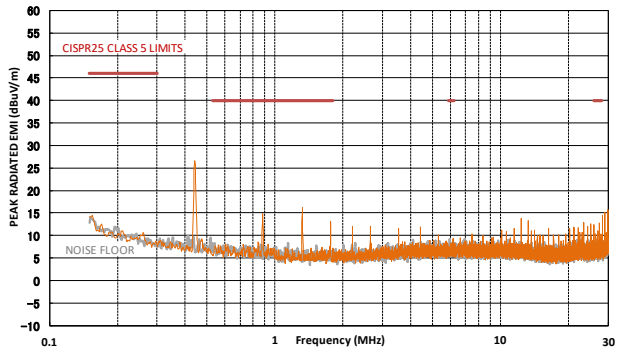
CISPR25 Class 5 Peak Conducted Emissions
150kHz -108MHz



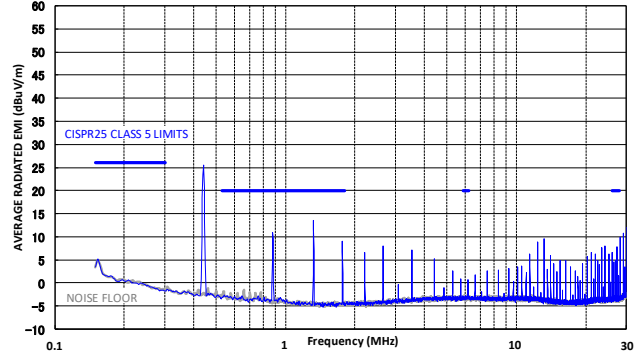
CISPR25 Class 5 Average Conducted Emissions
150kHz - 108MHz



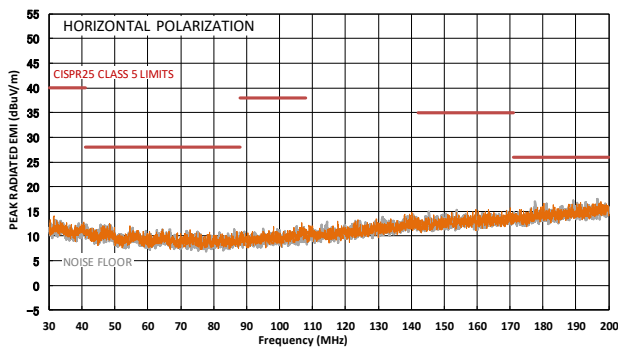
CISPR25 Class 5 Peak Radiated Emissions
150kHz-30MHz



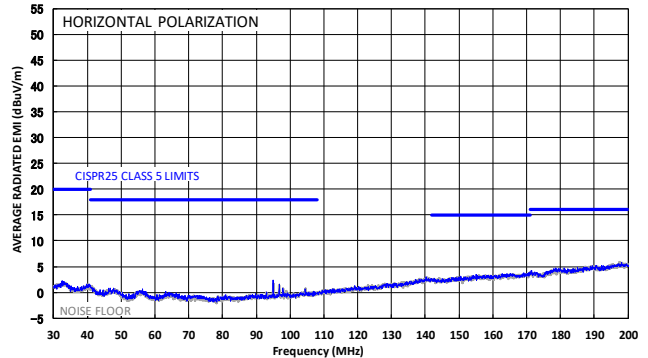
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150kHz-30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz-200MHz



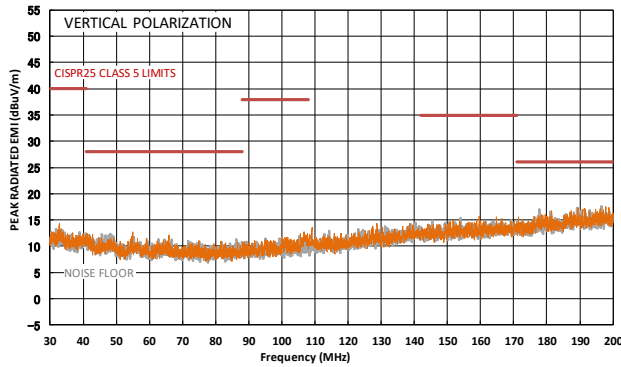
CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz-200MHz



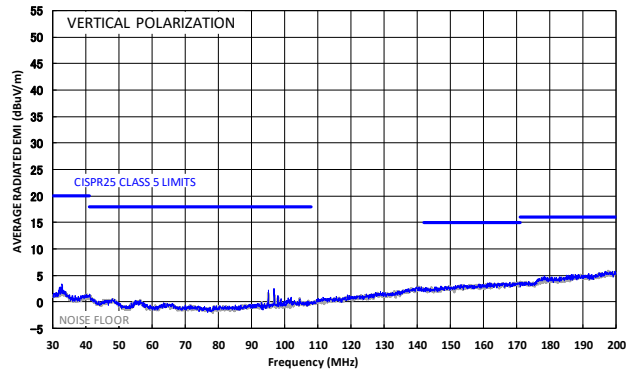
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_o=2A, L = 4.7μH, f_{sw} = 450kHz, with EMI filters, T_A = +25°C, unless otherwise noted. ⁽⁷⁾

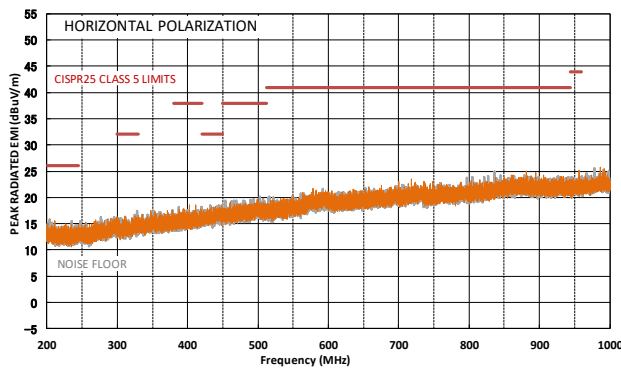
CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz-200MHz



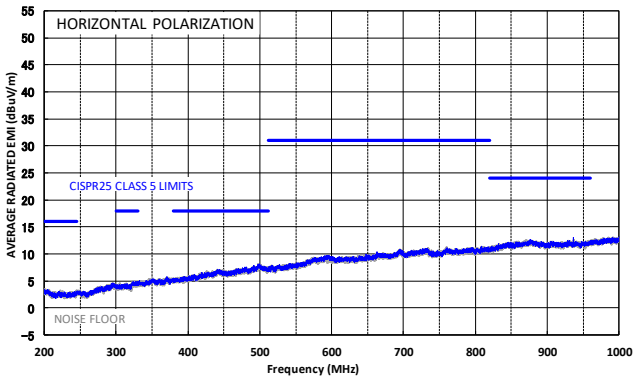
CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz-200MHz



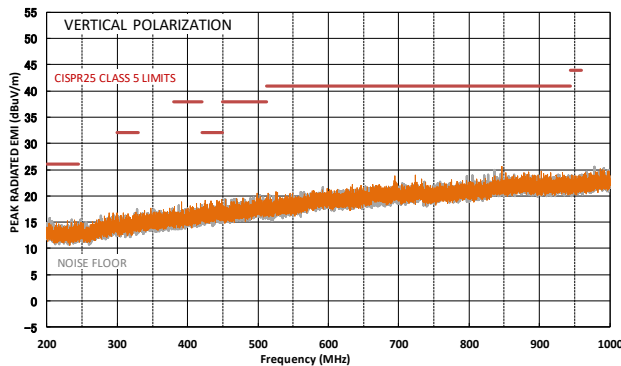
CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 200MHz-1GHz



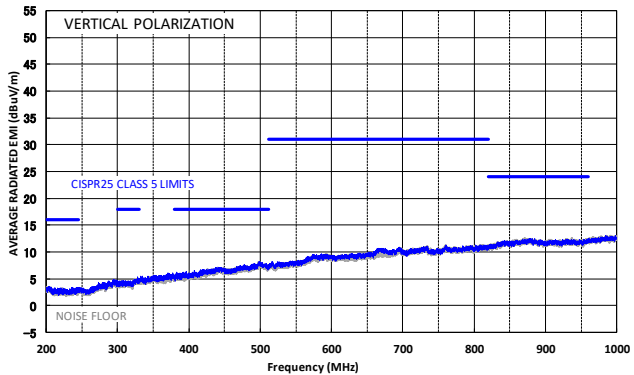
CISPR25 Class 5 Average Radiated Emissions
Horizontal, 200MHz-1GHz



CISPR25 Class 5 Peak Radiated Emissions
Vertical, 200MHz-1GHz



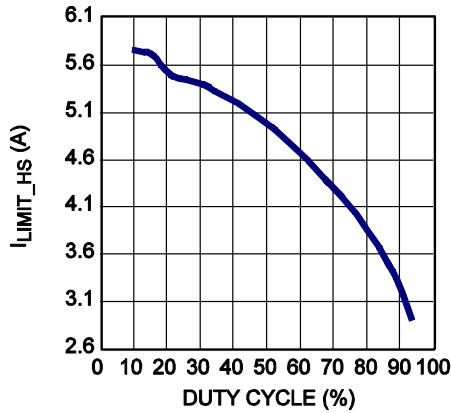
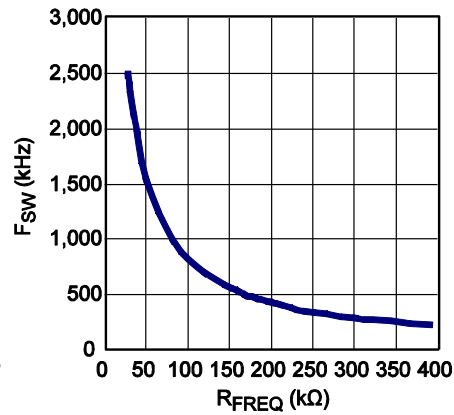
CISPR25 Class 5 Average Radiated Emissions
Vertical, 200MHz-1GHz



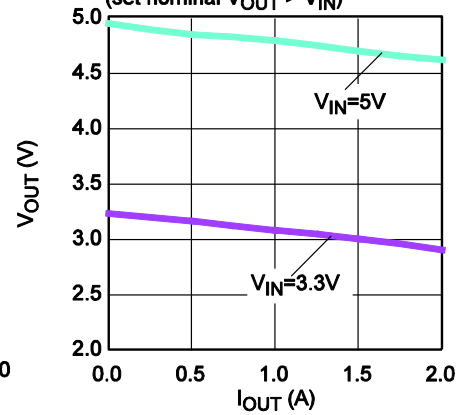
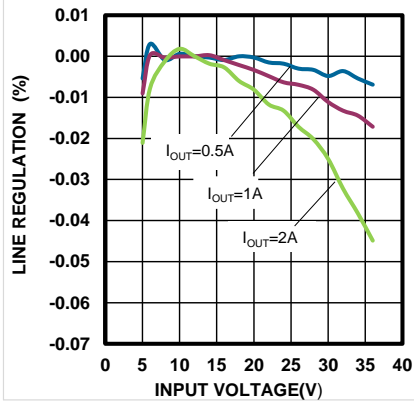
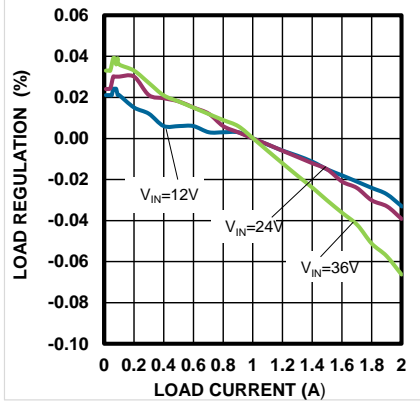
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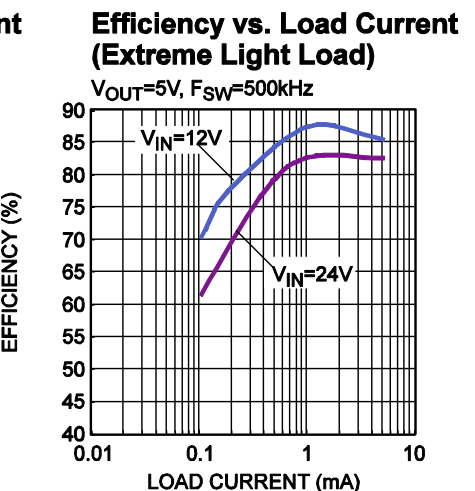
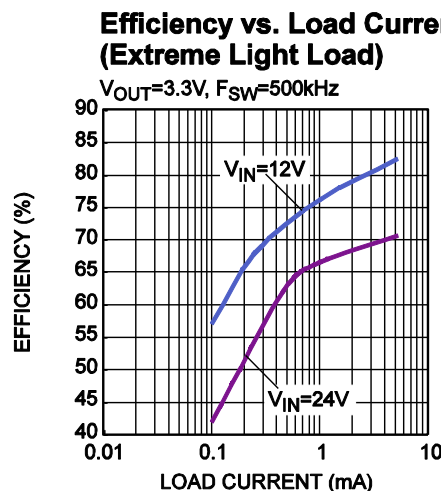
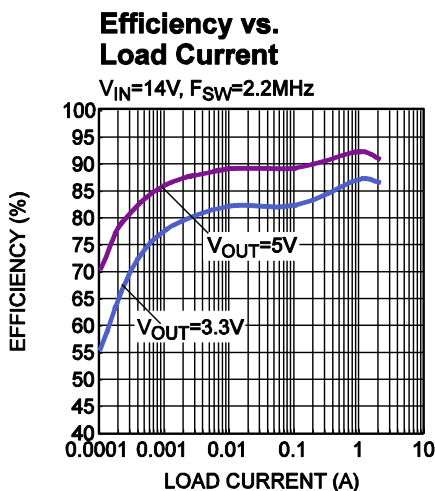
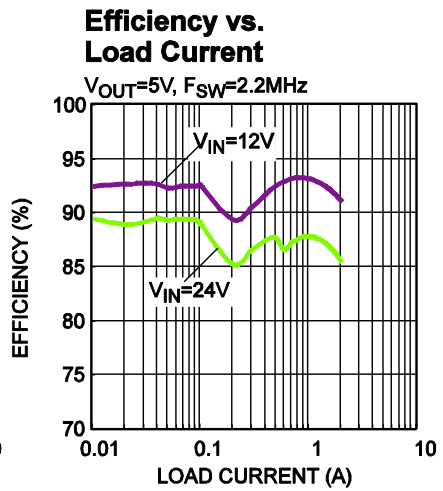
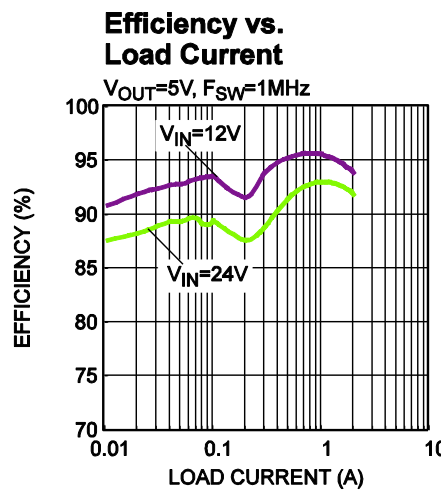
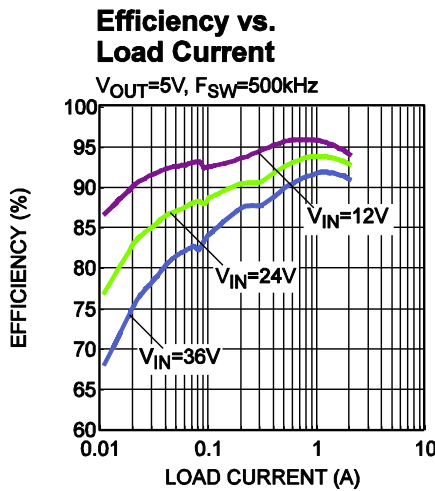
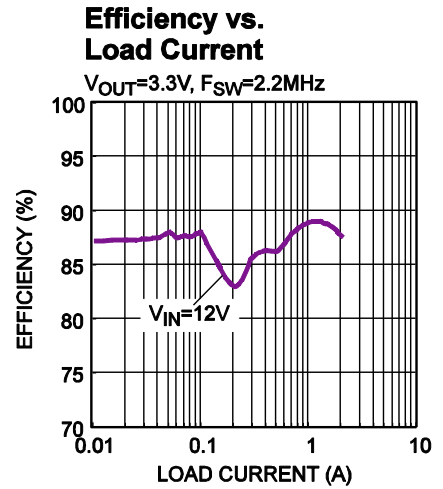
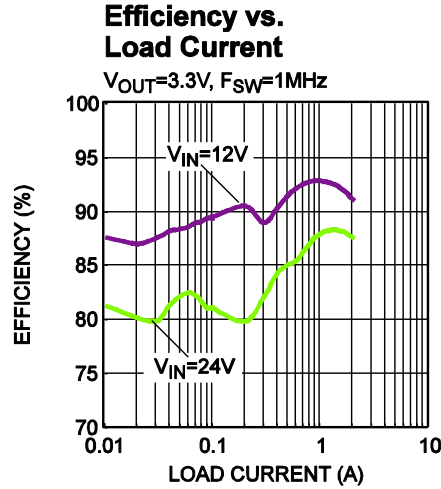
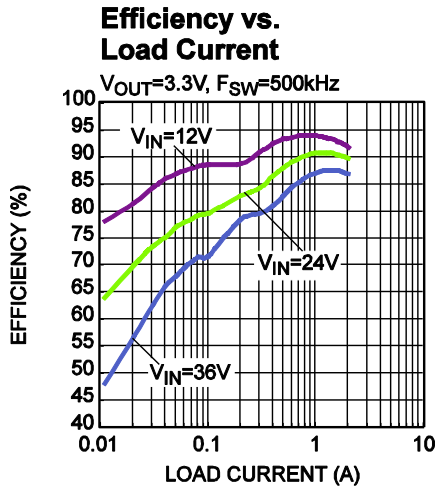
7) The EMC test results are based on the application circuit with EMI filters as shown in Figure14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.

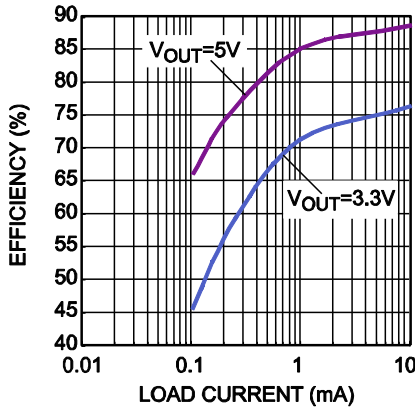
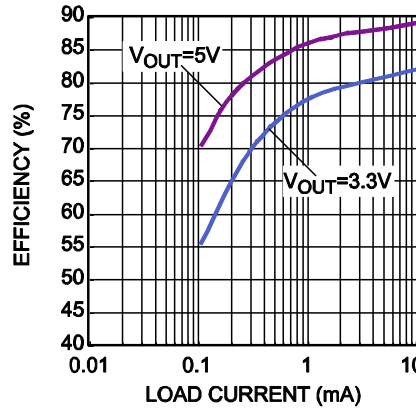
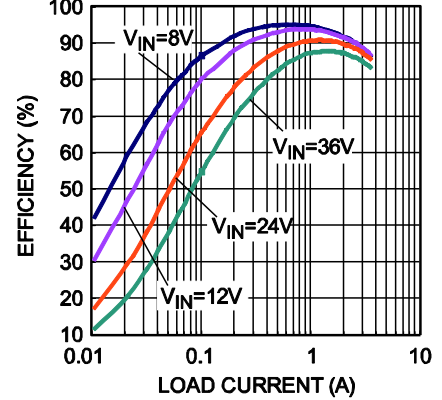
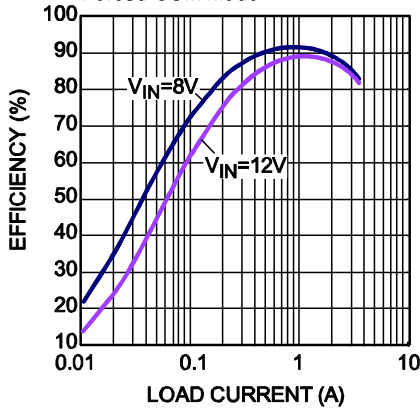
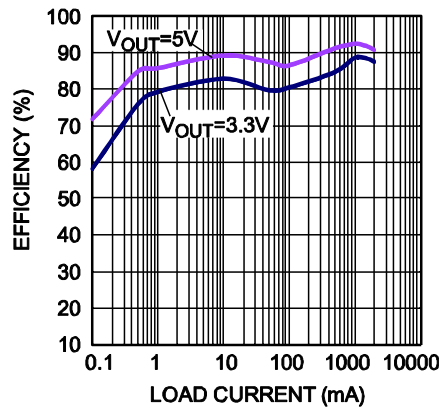
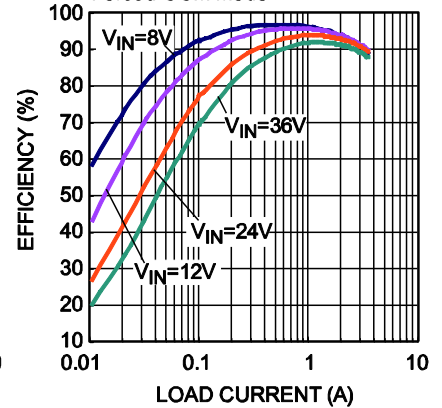
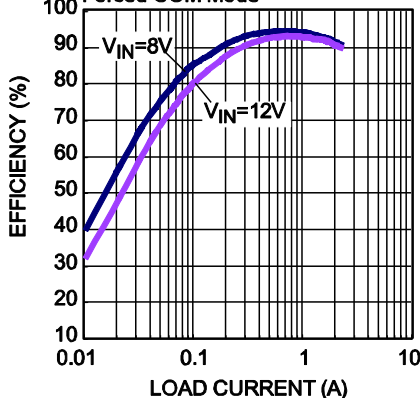
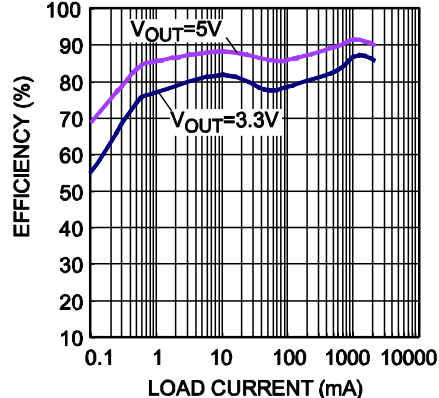
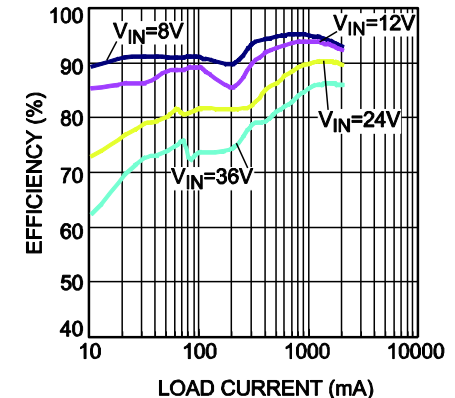
Current Limit vs. Duty Cycle

F_{SW} vs. R_{FREQ}

Output Voltage vs. Load Current

Dropout Performance

 (set nominal $V_{OUT} > V_{IN}$)

Line Regulation

Load Regulation


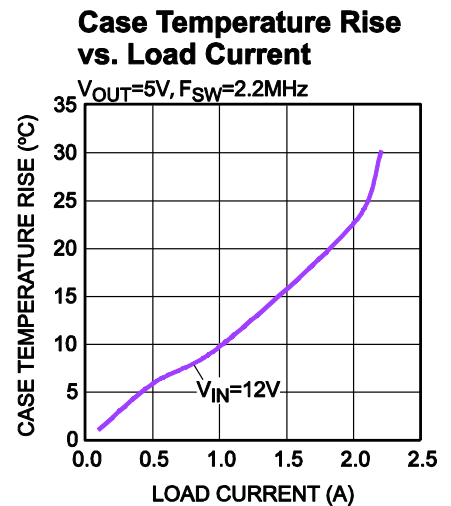
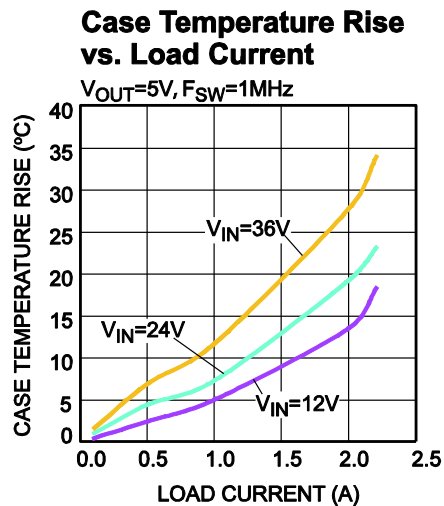
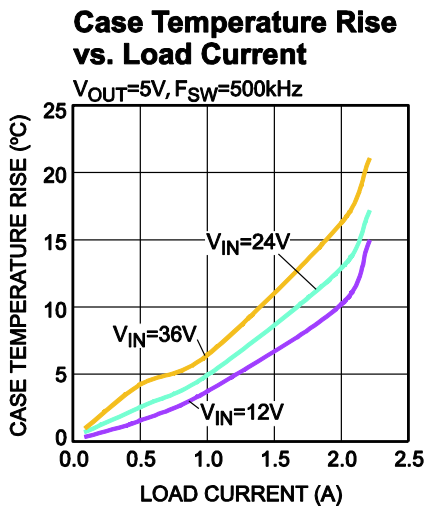
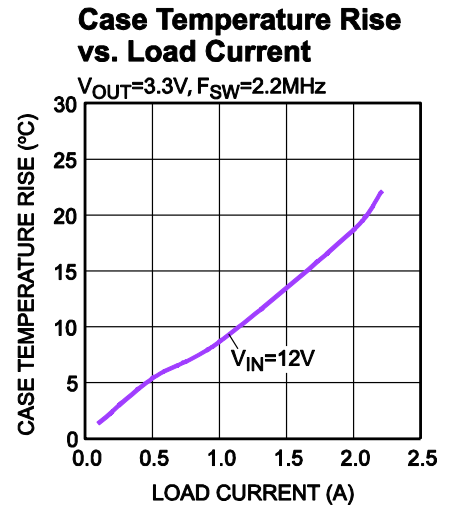
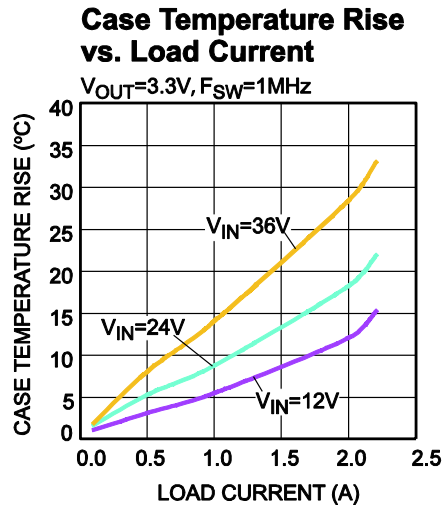
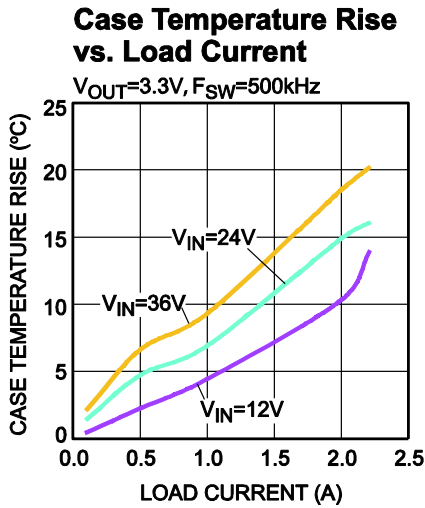
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.


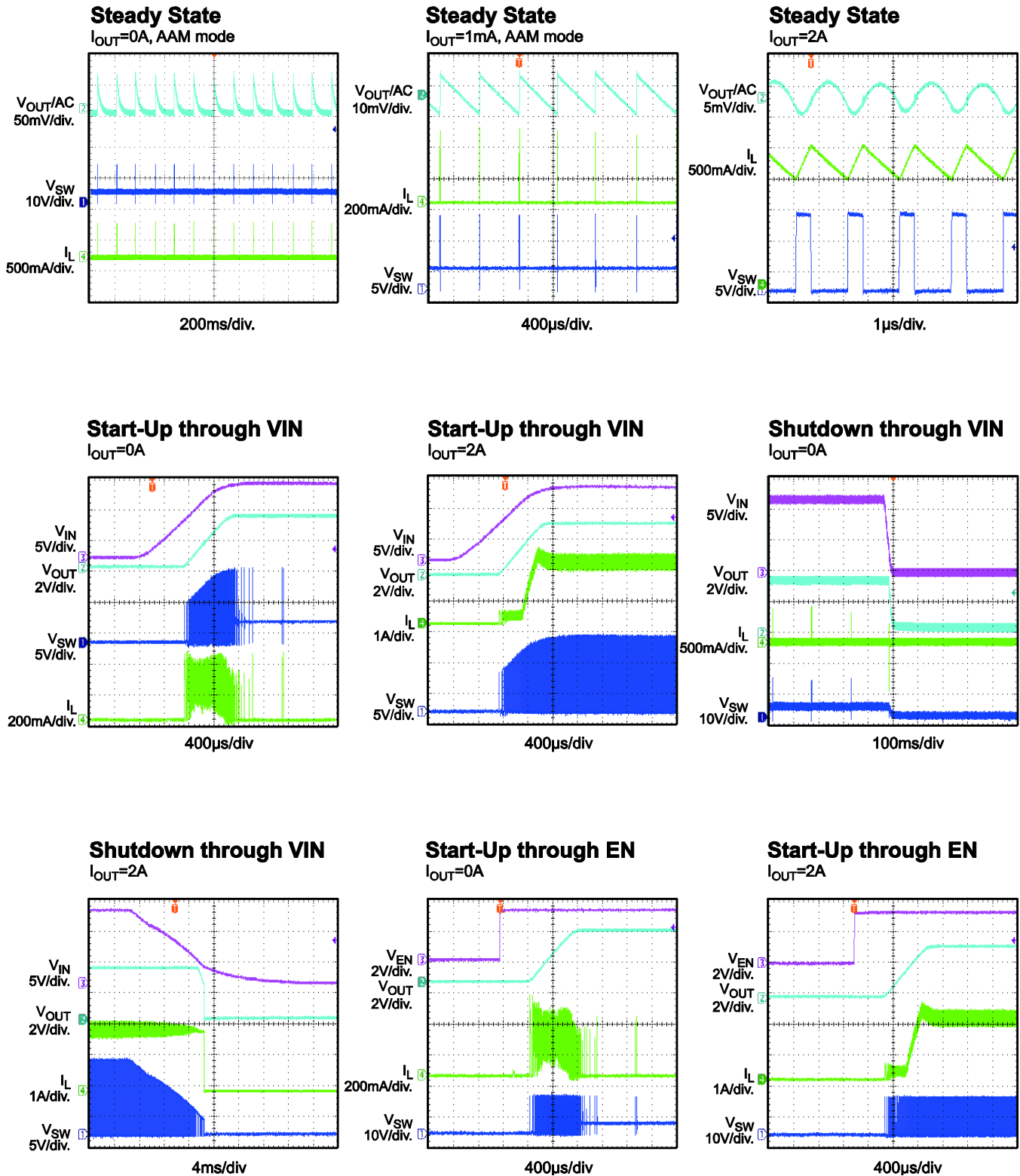
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.

Efficiency vs. Load Current (Extreme Light Load)
 $V_{IN}=14V$, $F_{SW}=400kHz$

Efficiency vs. Load Current (Extreme Light Load)
 $V_{IN}=14V$, $F_{SW}=2.2MHz$

Efficiency vs. Load Current
 $V_{OUT}=3.3V$, $F_{SW}=500kHz$, Forced CCM Mode

Efficiency vs. Load Current
 $V_{OUT}=3.3V$, $F_{SW}=2.2MHz$, Forced CCM Mode

Efficiency vs. Load Current
 $V_{IN}=12V$, $F_{SW}=2.2MHz$, $L=2.2\mu H$

Efficiency vs. Load Current
 $V_{OUT}=5V$, $F_{SW}=500kHz$, Forced CCM Mode

Efficiency vs. Load Current
 $V_{OUT}=5V$, $F_{SW}=2.2MHz$, Forced CCM Mode

Efficiency vs. Load Current
 $V_{IN}=14V$, $F_{SW}=2.2MHz$, $L=2.2\mu H$

Efficiency vs. Load Current
 $V_{OUT}=3.3V$, $F_{SW}=800kHz$, $L=10\mu H$


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.

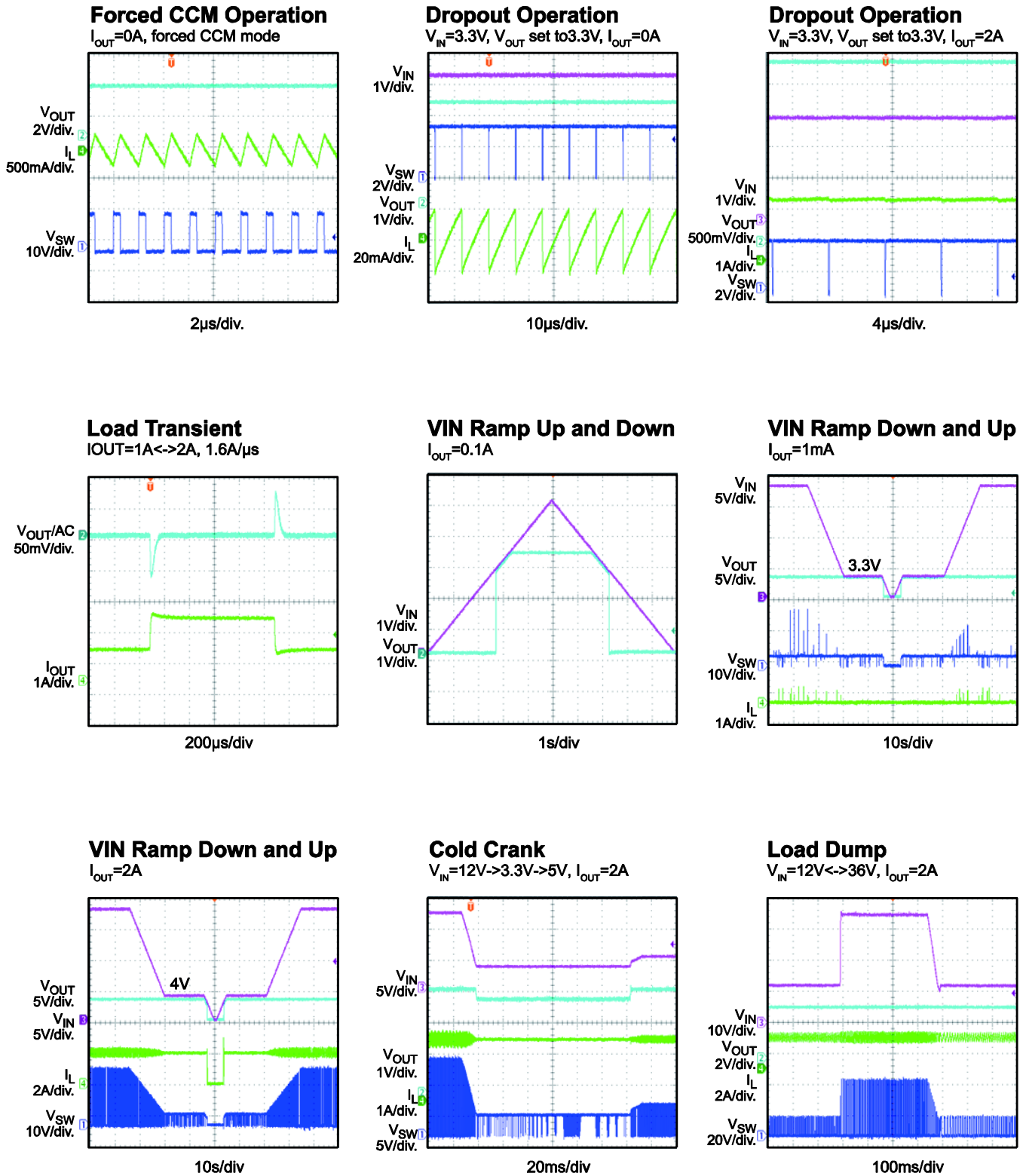


TYPICAL PERFORMANCE CHARACTERISTICS (continued)
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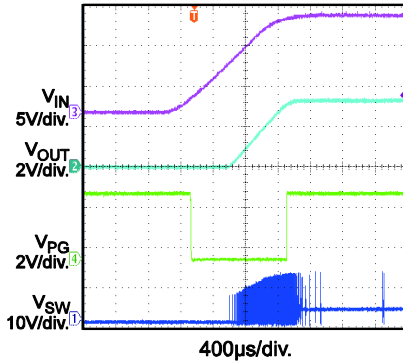
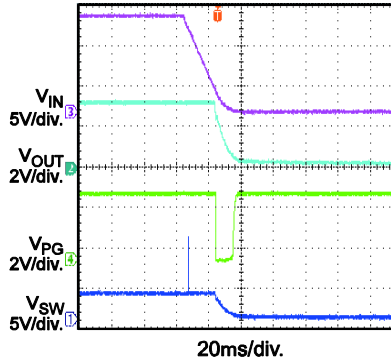
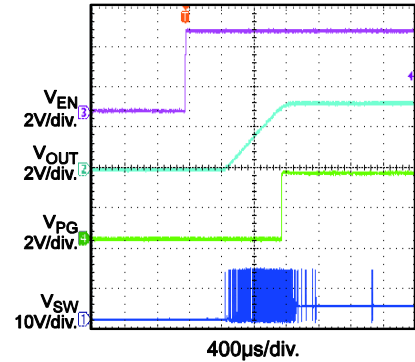
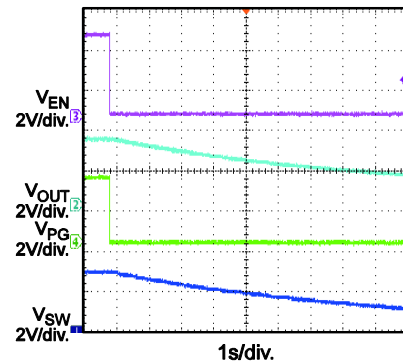
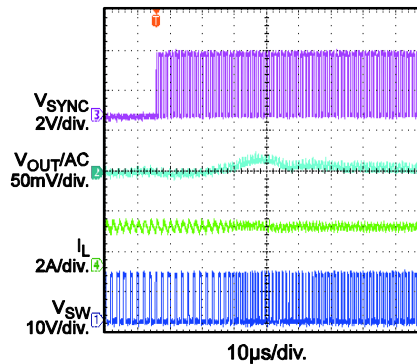
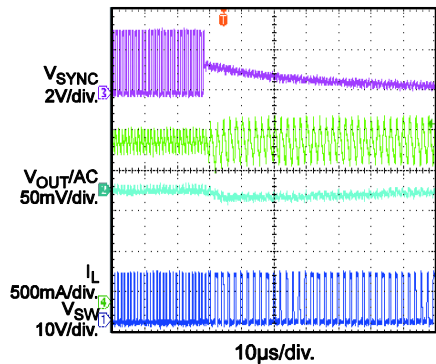
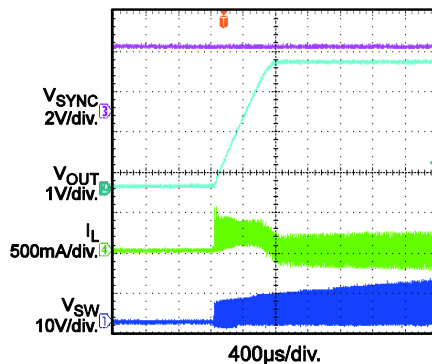
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.



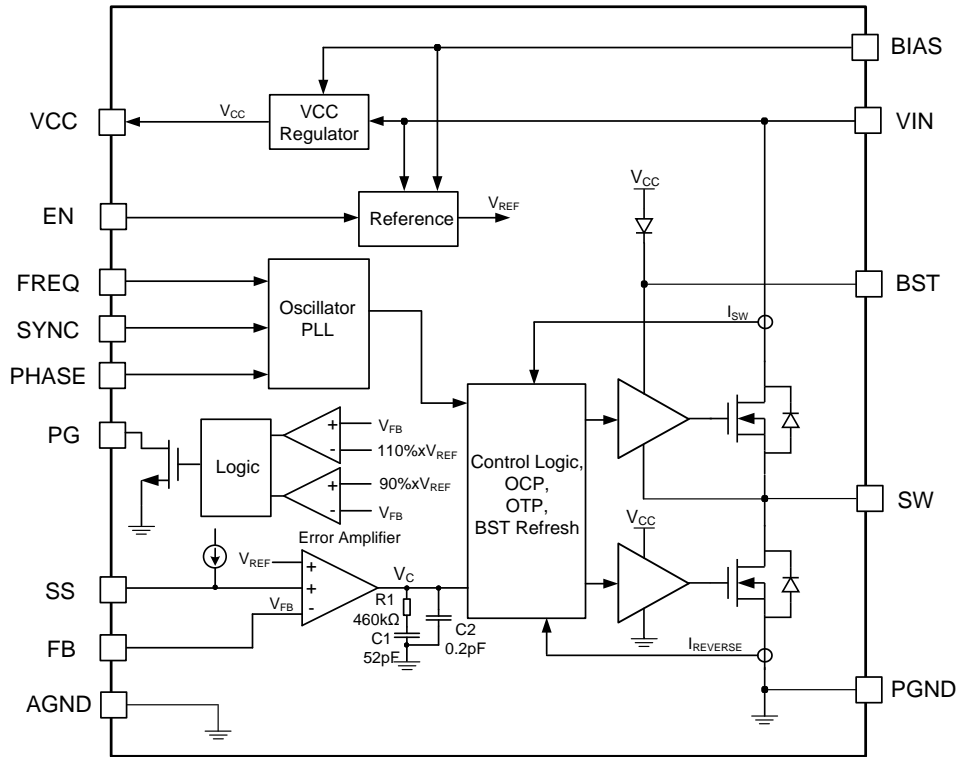
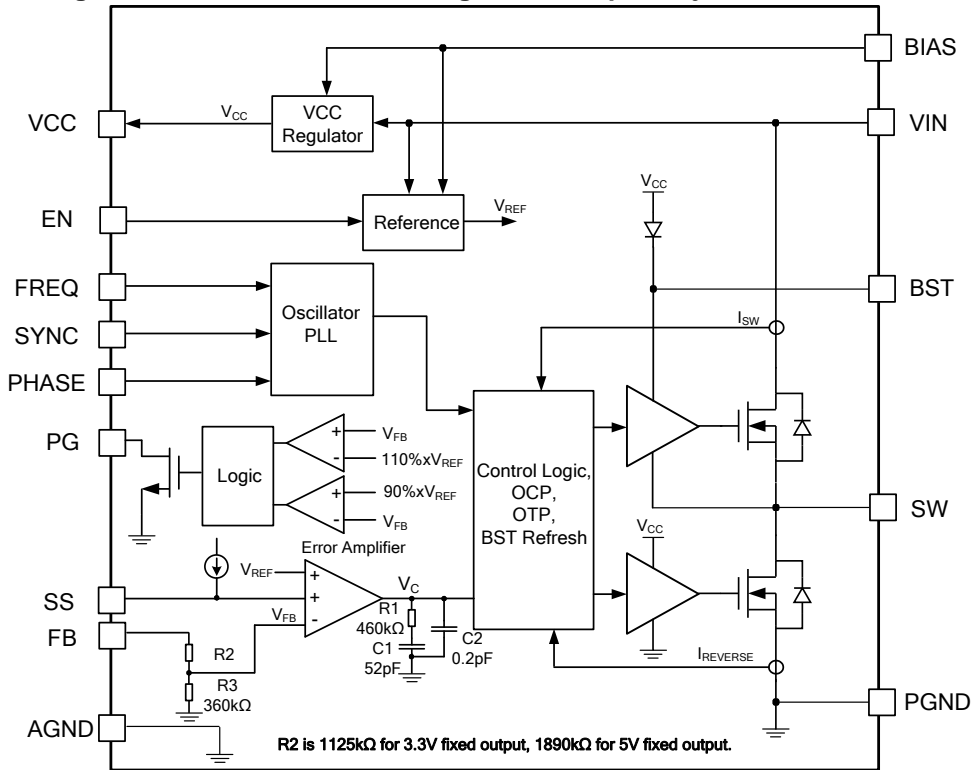
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.


TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM, $T_A = +25^\circ C$, unless otherwise noted.

PG in Start-Up through VIN
 $I_{OUT} = 0A$, PG is Pulled to 3.3V through 100k Resistor

PG in Shutdown through VIN
 $I_{OUT} = 0A$, PG is Pulled to 3.3V through 100k Resistor

PG in Start-Up through EN
 $I_{OUT} = 0A$, PG is Pulled to 3.3V through 100k Resistor

PG in Shutdown through EN
 $I_{OUT} = 0A$, PG is Pulled to 3.3V through 100k Resistor

Sync In Transient
 $I_{OUT} = 2A$, SYNC = 1MHz

Sync Out Transient
 $I_{OUT} = 2A$, SYNC = 1MHz

Forced CCM Entry
 $I_{OUT} = 0A$, Pull Sync High before Startup


PIN FUNCTIONS

Pin # QFN-16 (3mmx4mm)	Name	Description
1	PHASE	Selectable in-phase or 180° out-of-phase of the SYNC input. Pull PHASE high to be in-phase. Pull PHASE low to be 180° out-of-phase. Recommend to connect this pin to GND if not used.
2	VIN	Input supply. VIN supplies power to all of the internal control circuitries and the power switch connected to SW. Place a decoupling capacitor to ground close to VIN to minimize switching spikes.
3, 10	SW	Switch node. SW is the output of the internal power switch. Pin 3 and Pin 10 are internally connected.
4, 9	PGND	Power ground. PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.
5	EN	Enable. Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip.
6	SYNC	Synchronize. Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. SYNC can also be used to select forced continuous conduction mode (CCM) or advanced asynchronous mode (AAM). Before the chip starts up, drive SYNC low or leave SYNC floating to choose AAM, and drive SYNC high to external power source or pull up SYNC to VCC directly to set the part forced CCM mode.
7	PG	Power good output. The output of PG is an open drain. Float PG if not used.
8	BIAS	Bias input. Connect BIAS to an external power supply ($5V \leq V_{BIAS} \leq 18V$) to reduce power dissipation and increase efficiency. Float BIAS or connect BIAS to ground if not used.
11	BST	Bootstrap. BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
12	VCC	Bias supply. VCC supplies power to the internal control circuit and gate drivers. Place a decoupling capacitor ($\geq 1\mu F$) to ground close to VCC.
13	AGND	Analog ground. AGND is the reference ground of the logic circuit.
14	SS	Soft-start input. Place a capacitor from SS to AGND to set the soft-start period. The MPQ9842 sources $10\mu A$ from SS to the soft-start capacitor during start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up. There is an internal 0.7ms soft-start setting, the final SS time is determined by the longer time between 0.7ms and external SS setting time.
15	FB	Feedback input. For adjustable output version, connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For fixed output version, connect FB pin to the output directly.
16	FREQ	Switching frequency program. Connect a resistor from FREQ to ground to set the switching frequency.

BLOCK DIAGRAM

Figure 1-1: Functional Block Diagram of Output Adjustable Version

Figure 1-2: Functional Block Diagram of Fixed Output Version

OPERATION

The MPQ9842 is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. The MPQ9842 provides 2A of highly efficient output current with current mode control. The MPQ9842 features a wide input voltage range, switching frequency programmable from 350kHz to 2.5MHz, external soft start, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the MPQ9842 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}).

If the current in the HS-FET does not reach V_{COMP} in one PWM period, the HS-FET remains on, saving a turn-off operation.

When the high-side power switch is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next cycle begins.

For each turn-on and -off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

Advanced Asynchronous Mode (AAM)

The MPQ9842 employs advanced asynchronous mode (AAM) functionality to optimize efficiency during light-load or no-load conditions. AAM can be enabled by connecting SYNC to a low level (<0.4V) before start-up; CCM can be able when connecting SYNC to a high level (>1.8V) before start-up. SYNC can be used to synchronize switching again after start-up.

If continuous conduction mode (CCM) is enabled, the MPQ9842 is forced to work with a fixed frequency regardless of the output load current. The advantage of CCM is the controllable frequency and smaller output ripple, but it also has low efficiency at light load (see Figure 2).

If AAM is enabled, the MPQ9842 first enters non-synchronous operation for as long as the inductor current is approaching zero at light load. If the load is further decreased or is at no load, V_{COMP} drops below the AAM voltage (V_{AAM}). The MPQ9842 enters power-save mode (PSM), putting the chip into sleep mode, which consumes very low quiescent current to further improve light-load efficiency.

In PSM, the internal clock is reset whenever V_{COMP} crosses over V_{AAM} , and the crossover time is taken as the benchmark of the next clock. When the load increases, and the DC value of V_{COMP} is higher than V_{AAM} , the operation mode is discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency.

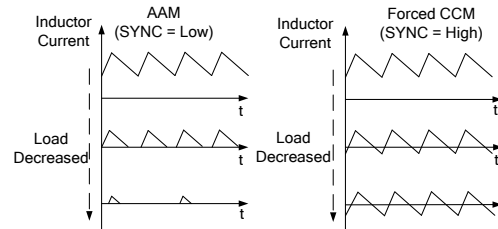


Figure 2 : AAM and Forced CCM

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference (0.8V) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form V_{COMP} , which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Bootstrap Charging

The bootstrap capacitor (0.1 μ F to 1 μ F) is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is lower than its regulation, a PMOS pass transistor connected from VIN to BST is turned on. The charging current path is from VIN to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. When the HS-FET is on, VIN is about equal to SW, so the bootstrap capacitor cannot be charged.

At a higher duty cycle operation condition, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

Low Dropout Operation (BST Refresh)

To improve dropout, the MPQ9842 is designed to operate at close to 100% duty cycle for as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In PSM or DCM, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, making the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and printed circuit board resistance.

Internal Regulator

Most of the internal circuitry is powered on by the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5V, the output of the regulator is in full regulation. When VIN is lower than 5V, the output degrades.

For better thermal performance, connect BIAS to an external 5V source. VCC and the internal circuit are then powered by BIAS. Since there is an internal diode between BIAS and the internal circuit, float BIAS or connect BIAS to GND if not being used.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip is put into the lowest shutdown current mode. Pulling EN

above its threshold voltage turns on the part. Do not float EN.

Frequency Programmable (FREQ)

The MPQ9842 oscillating frequency is programmed by either an external resistor (R_{FREQ}) from FREQ to ground or by a logic level SYNC signal.

The value of R_{FREQ} can be calculated with Equation (1):

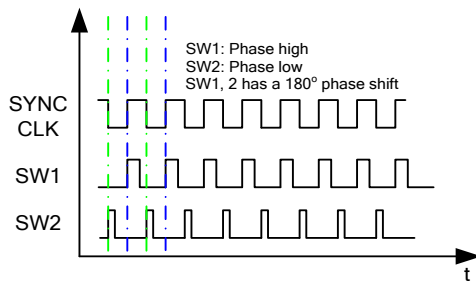
$$R_{FREQ}(\text{k}\Omega) = \frac{170000}{f_s^{1.11}(\text{kHz})} \quad (1)$$

The chip can be synchronized to an external clock range from 350kHz up to 2.5MHz through FREQ/SYNC.

SYNC and PHASE

The internal oscillator frequency can also be synchronized to an external clock ranging from 350kHz to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V, and low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. The pulse should be longer than 100ns in application.

PHASE is used when two or more MPQ9842 devices are in parallel with the same SYNC clock. Pulling PHASE high forces the device to operate in-phase of the SYNC clock. Pulling PHASE low forces the device to be 180° out-of-phase of the SYNC clock. By setting different voltages for PHASE, two devices can operate in 180° out-of-phase to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 3). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.


Figure 3: In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor. The internal SS voltage (V_{SSI}) rises with the soft-start voltage (V_{SS}), but V_{SSI} differs from V_{SS} in that it has a 0.5V offset and some delay. When V_{SS} is below 0.5V, V_{SSI} is 0V. V_{SSI} rises from 0V to 0.8V while V_{SS} rises from 0.5V to 1.6V. At this time, the error amplifier uses V_{SSI} as the reference, and the output voltage ramps up from 0V to the regulated value following V_{SSI} rising. When V_{SS} reaches 1.6V, V_{SSI} is 0.8V and overrides the internal V_{REF} , so the error amplifier uses the internal V_{REF} as the reference.

The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times 1.1\text{V}}{I_{SS}(\mu\text{A})} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 10 μA SS charge current. There is also an internal 0.7ms soft start when the SS pin is floating. The final SS time is determined by the longer time between 0.7ms and the external SS set time.

SS can be used for tracking and sequencing.

Pre-Bias Start-Up

During start-up, if $V_{FB} > V_{SSI} - 150\text{mV}$, then the output has a pre-bias voltage, and neither the HS-FET or LS-FET turn on until $V_{SSI} - 150\text{mV}$ is higher than V_{FB} .

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than its upper

threshold, the power MOSFETs are shut down. When the temperature is lower than its lower threshold, thermal shutdown is removed, and the MPQ9842 is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current sense MOSFET. The current is then fed to the high-speed current comparator for current-mode control purposes. The current comparator takes this sensed current as one of its inputs. When the HS-FET is turned on, the comparator is first blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power switch current with V_{COMP} . When the sensed current is higher than V_{COMP} , the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is limited cycle-by-cycle internally.

Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, the IC shuts down momentarily and begins discharging the soft-start capacitor. The IC restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Start-Up and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50 μs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure that the rest of the circuitries are ready before ramping up slowly.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this

shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ9842 has a power good (PG) indicator. PG is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.: 100k Ω). In the presence of an input voltage, the MOSFET turns on so that PG is pulled low before SS is ready. When the regulator output

is within $\pm 10\%$ of its nominal output, the PG output is pulled high after a delay, typically 30 μ s. When the output voltage moves outside of this range with a hysteresis, the PG output is pulled low with a 50 μ s delay to indicate a failure output status.

APPLICATION INFORMATION

Setting the Output Voltage

For adjustable output version, the external resistor divider connected to FB sets the output voltage (see Figure 4).

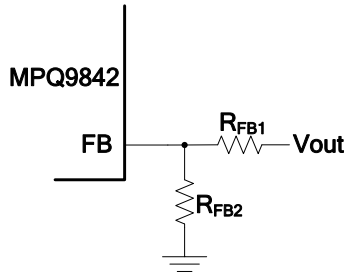


Figure 4: Feedback Network

Choose R_{FB1} first, then R_{FB2} can be calculated with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V _{OUT} (V)	R _{FB1} (kΩ)	R _{FB2} (kΩ)
3.3	41.2 (1%)	13 (1%)
5	68.1 (1%)	13 (1%)

For fixed output version, connect FB pin to the output directly.

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. An inductor with a larger value results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 10μF capacitor. It is strongly recommended to use another lower-value capacitor (e.g.: 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors,

ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}\right) \quad (9)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ9842 can be optimized for a wide range of capacitance and ESR values.

VIN UVLO Setting

The MPQ9842 has an internal, fixed, UVLO threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For applications that need a higher UVLO point, the

external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 5).

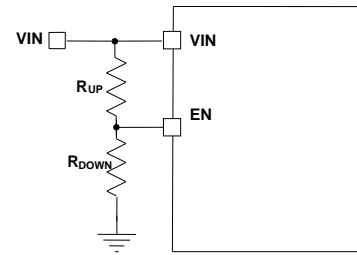


Figure 5: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (12) and Equation (13):

$$INUV_{RISING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN_RISING} \quad (12)$$

$$INUV_{FALLING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN_FALLING} \quad (13)$$

Where V_{EN_RISING} is 1.05V, and $V_{EN_FALLING}$ is 0.93V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended to be this power supply in the circuit (see Figure 6).

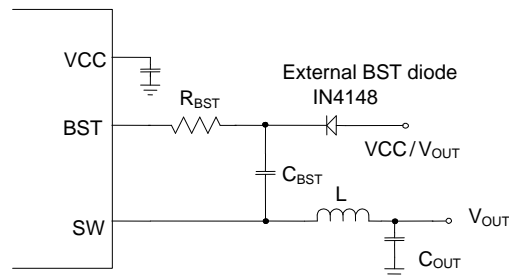


Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1μF to 1μF.

A resistor in series with BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high VIN. A higher resistance is better for SW spike reduction but compromises efficiency. To make

a tradeoff between EMI and efficiency, a $\leq 20\Omega$ R_{BST} is recommended.

Hot-Plug Application

In a hot-plug application, the VIN pin may turn on and off frequently before the power supply can establish a connection with the IC. In applications where the input power turns on and off frequently, the BST capacitor may have a residual voltage when the IC turns on. This may turn on the high-side MOSFET (HS-FET) for a short time before V_{CC} can rise sufficiently high, which can cause an unexpected overshoot on VOUT.

To protect the IC, hot-plug applications are not recommended. If a hot-plug application must be initiated, use a small BST capacitor (e.g. 47nF), a large VCC capacitor (e.g. 4.7 μ F), and a large PG resistor (e.g. 1M Ω) to reduce the overshoot risk. Contact an MPS FAE to confirm the design.

PCB Layout Guidelines ⁽⁸⁾

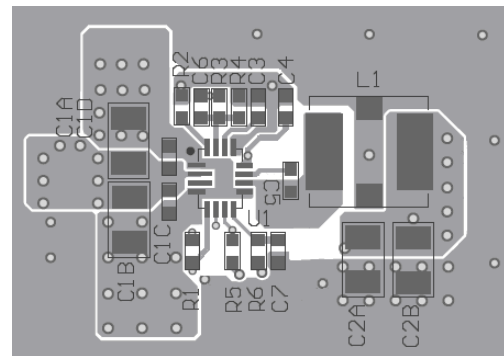
Efficient PCB layout, especially for the input capacitor placement, is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 7 and follow the guidelines below.

1. Place symmetric input capacitors as close to VIN and GND as possible. Recommend to connect pin1 to GND for symmetric input structure if in-phase not used. Pin3 and pin10 are internally connected. Connecting together on layout or not are both OK. Recommend to leave pin3 floating for shorter pin4 and pin1 trace and smaller input hot loop.
2. Use a large ground plane to connect to PGND directly.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.

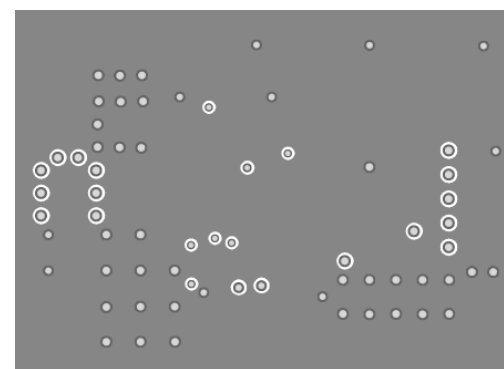
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
10. Use multiple vias to connect the power planes to internal layers.

NOTE:

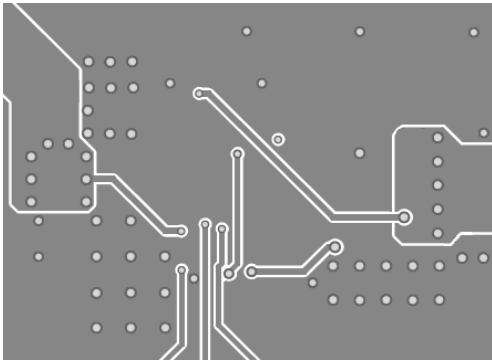
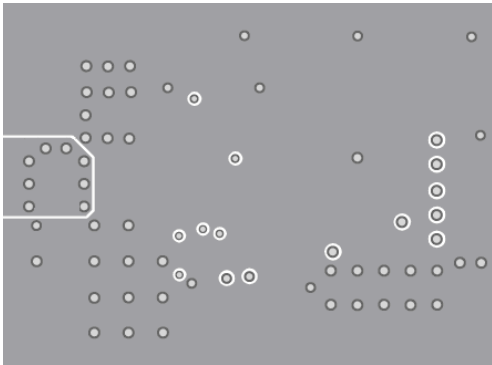
- 8) The recommended PCB layout is based on Figure 8.

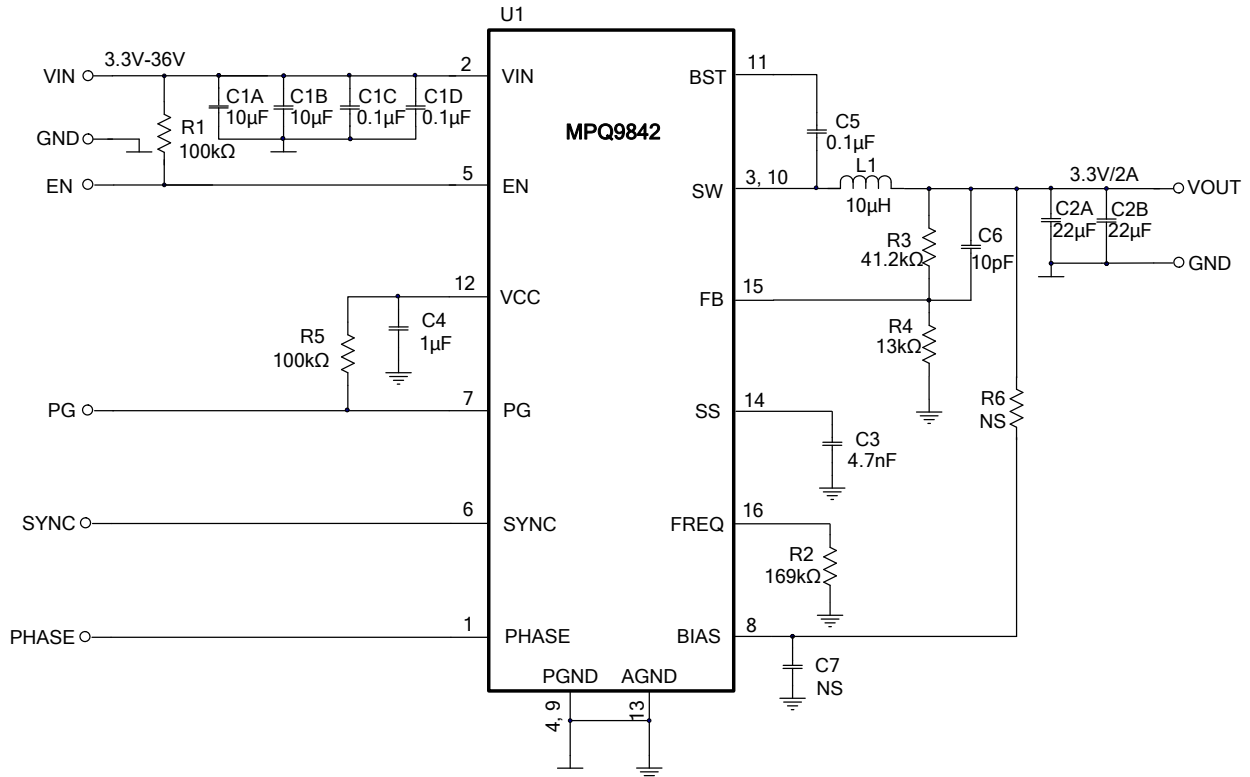
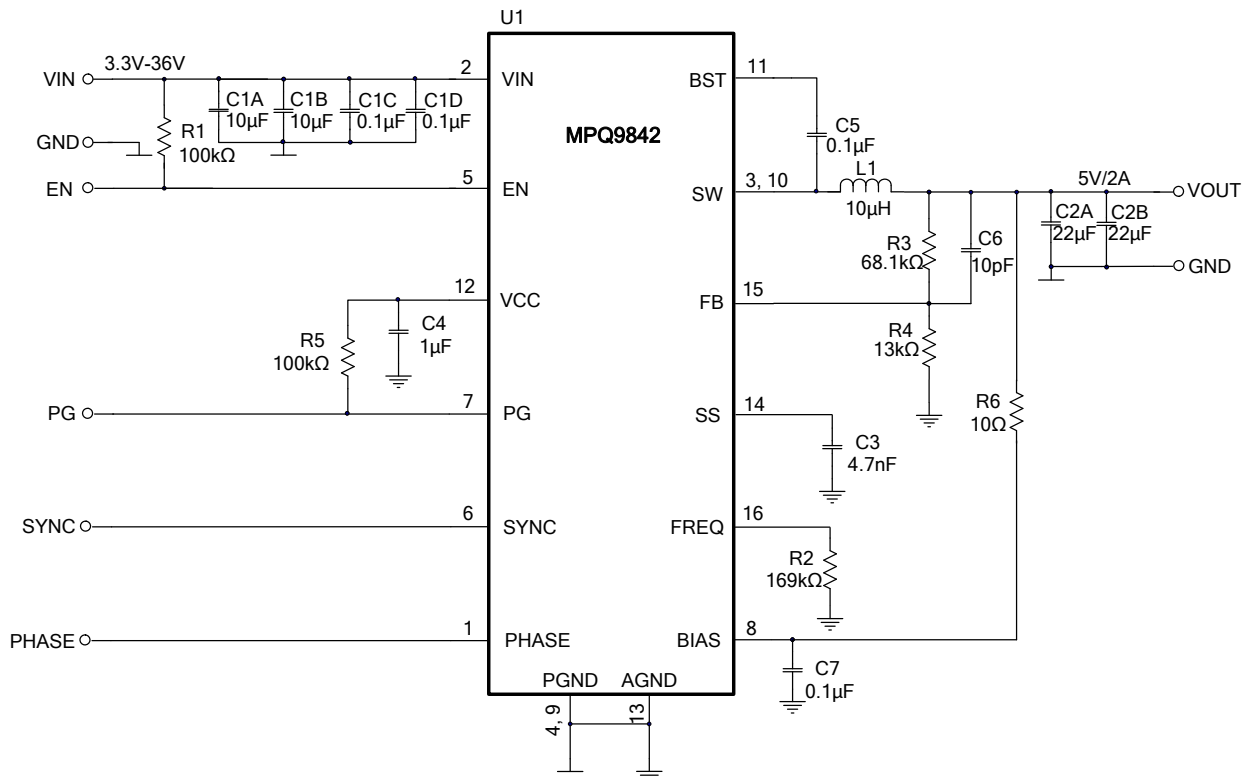


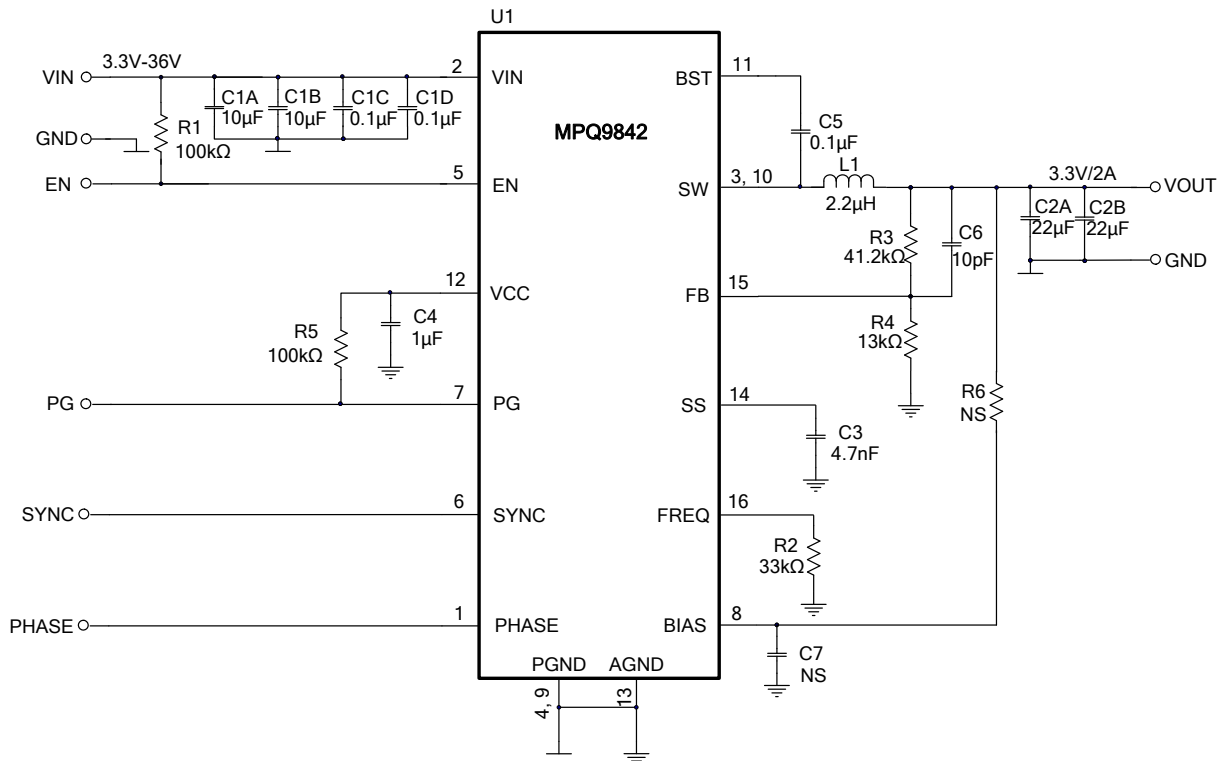
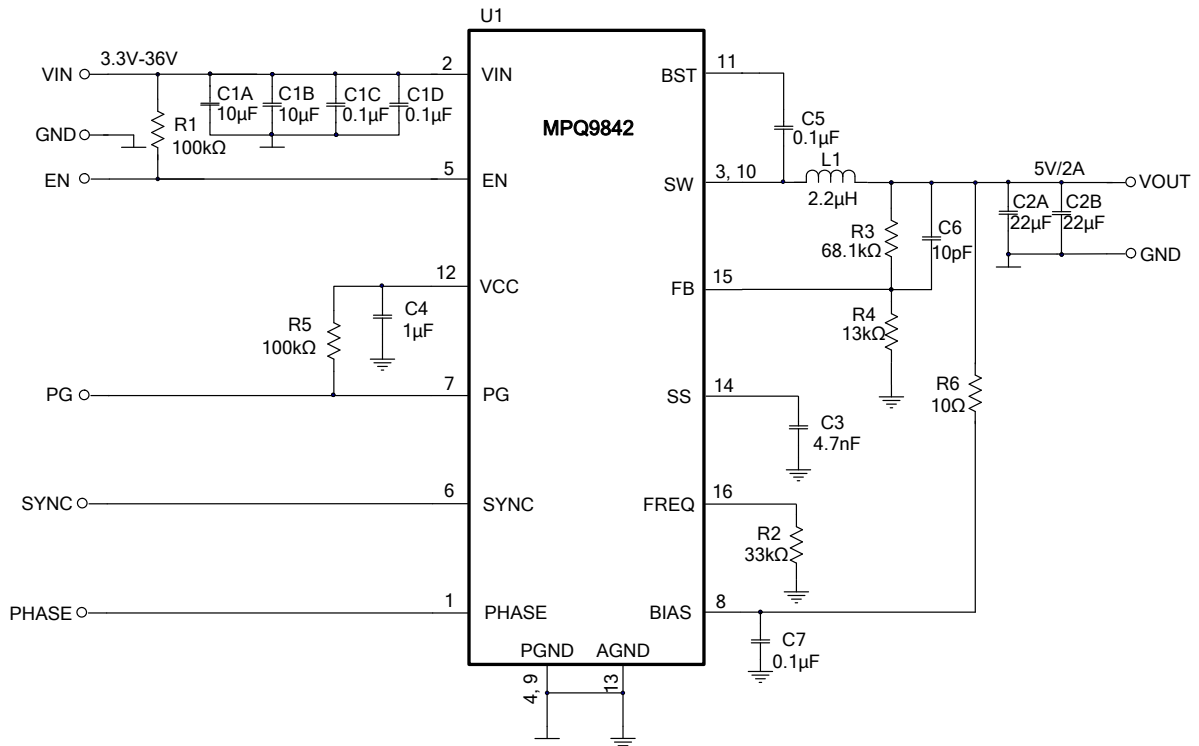
Top Layer

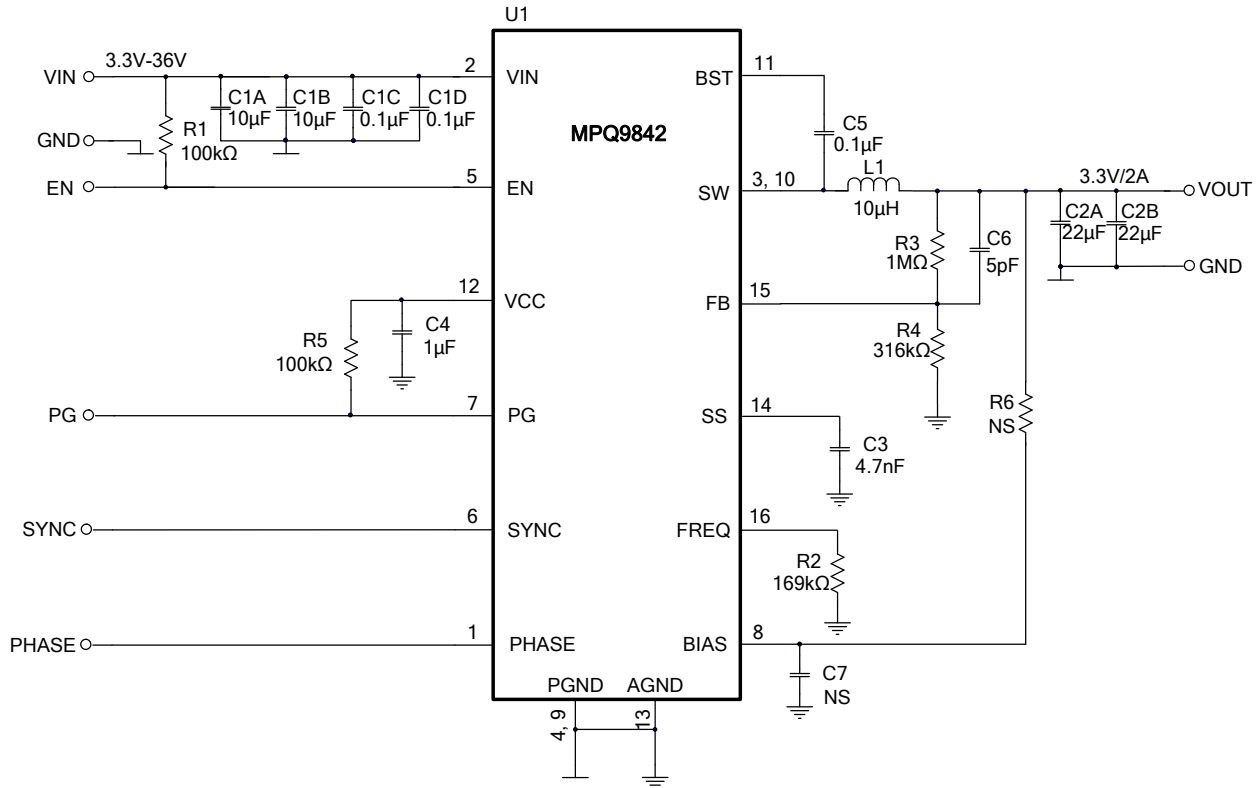
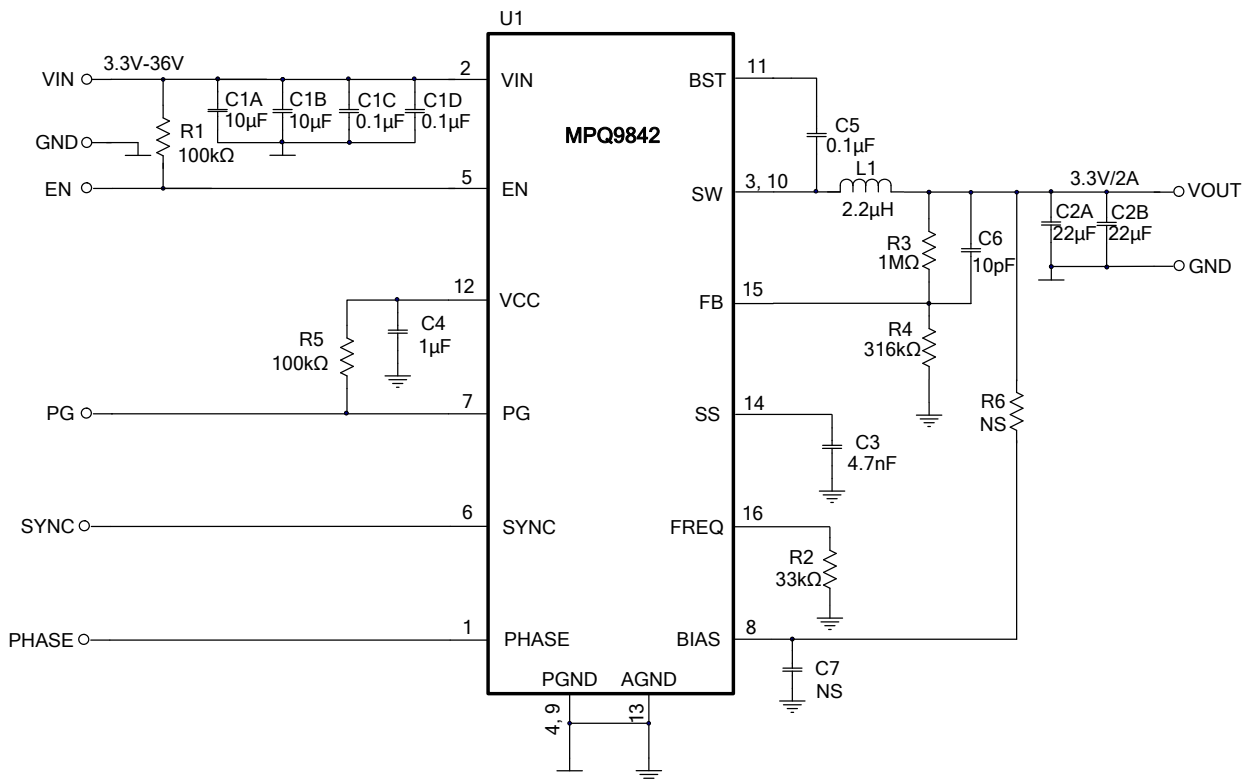


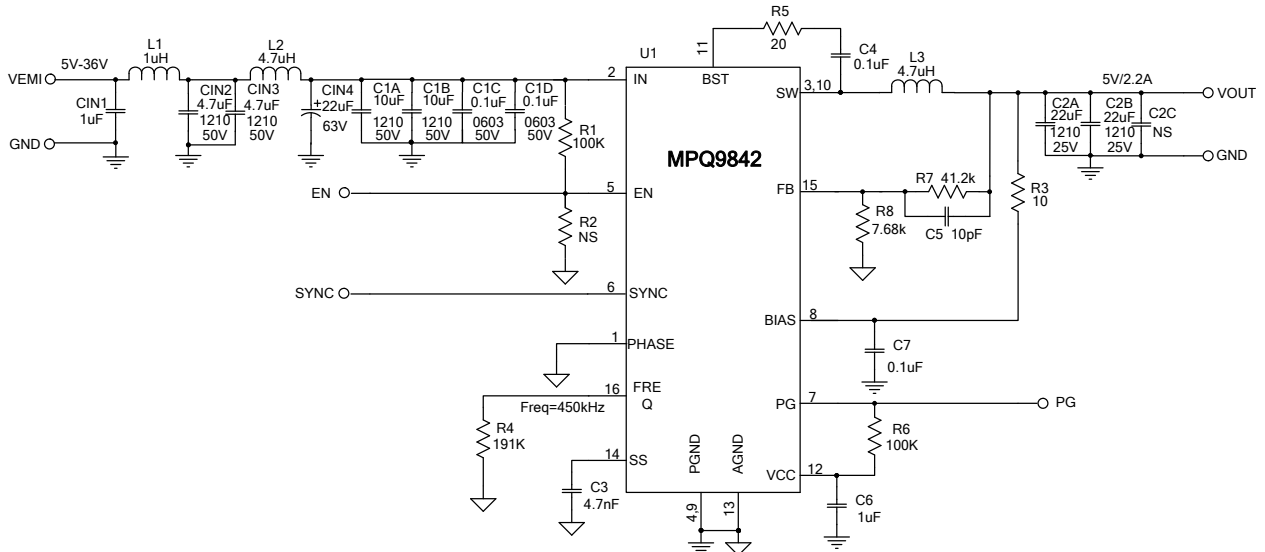
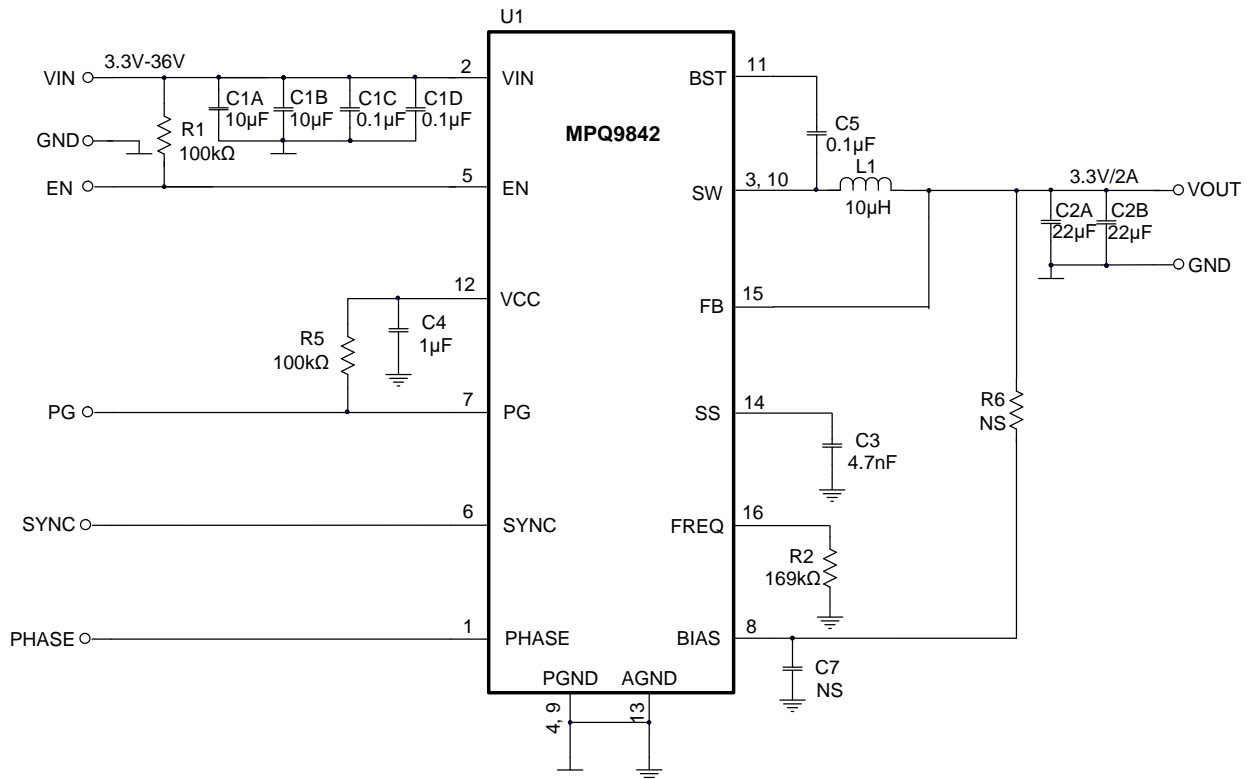
Inner Layer 1

**Inner Layer 2****Bottom Layer****Figure 7: Recommended PCB Layout**

TYPICAL APPLICATION CIRCUITS

Figure 8: $V_{OUT} = 3.3V$, $f_{sw} = 500kHz$

Figure 9: $V_{OUT} = 5V$, $f_{sw} = 500kHz$

TYPICAL APPLICATION CIRCUITS (continued)

Figure 10: $V_{OUT} = 3.3V$, $f_{sw} = 2.2MHz$

Figure 11: $V_{OUT} = 5V$, $f_{sw} = 2.2MHz$

TYPICAL APPLICATION CIRCUITS (continued)

Figure 12: $V_{OUT} = 3.3V$, $f_{sw}=500kHz$ for Big FB Resistor Divider Application

Figure 13: $V_{OUT} = 3.3V$, $f_{sw} = 2.2MHz$ for Big FB Resistor Divider Application


Figure 14: Application Circuit with EMI Filter @ $V_{OUT} = 5V/2A$, $f_{sw} = 450kHz$

Figure 15: 3.3V Fixed Output, $f_{sw} = 500kHz$

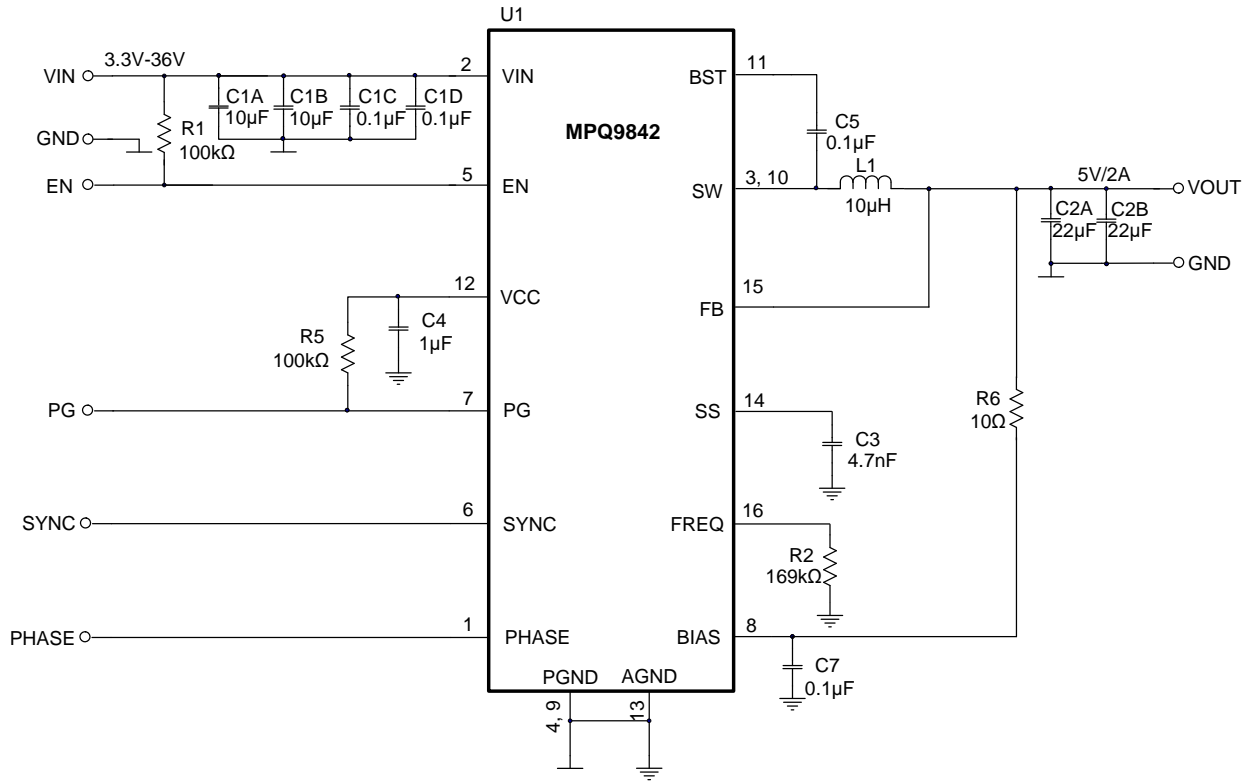
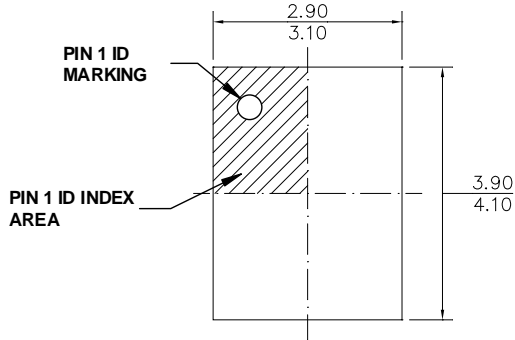


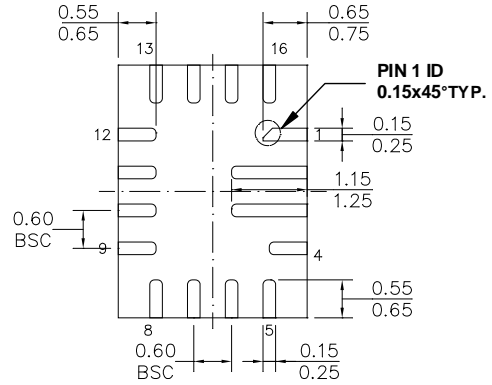
Figure 16: 5V Fixed Output, $f_{sw} = 500\text{kHz}$

PACKAGE INFORMATION

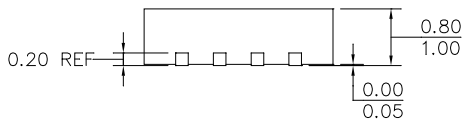
QFN-16 (3mmx4mm) Non-Wettable Flank



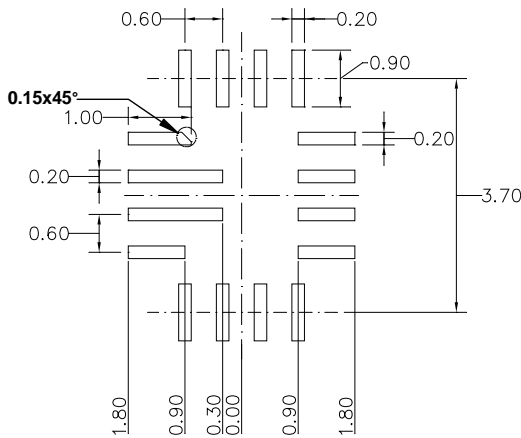
TOP VIEW



BOTTOM VIEW



SIDE VIEW



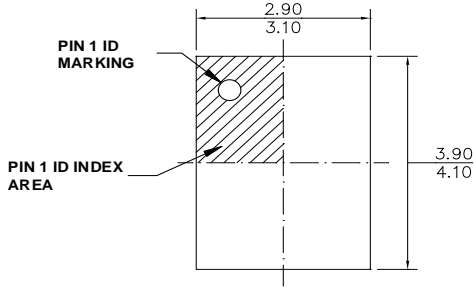
RECOMMENDED LAND PATTERN

NOTE:

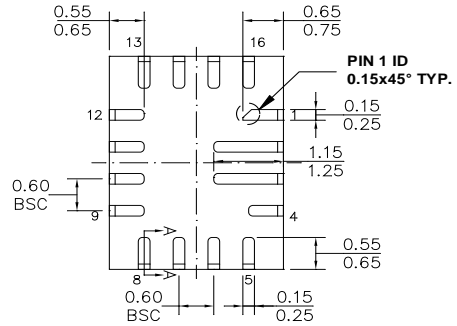
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION (continued)

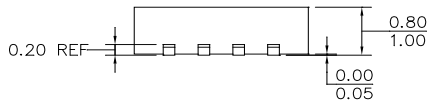
QFN-16 (3mmx4mm)
Wettable Flank



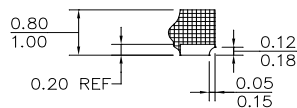
TOP VIEW



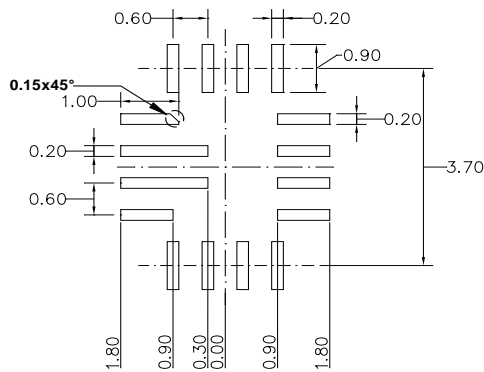
BOTTOM VIEW



SIDE VIEW



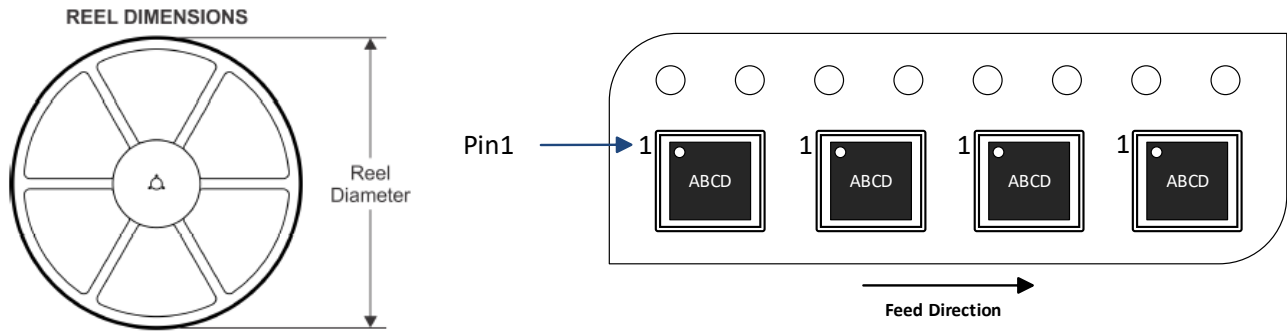
SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION


Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ9842GL-Z	QFN-16 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ9842GL-AEC1-Z							
MPQ9842GLE-AEC1-Z							
MPQ9842GLE-33-AEC1-Z							
MPQ9842GLE-5-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/3/2017	Initial Release	-
1.01	10/23/2017	Updated the Recommended Operating Conditions	4
1.02	4/19/2019	Added the MPQ9842-5/33 order package information	1, 2, 3, 20
		Updated the Recommended Operating Conditions	4
		Added the EMC result of CISPR 25 class 5	9, 10
		Added the PHASE and PG pin connection when not used in pin description	19
		Added the force CCM setting when starting up in the pin description	19
1.1	7/29/2022	Added the MSL rating	2
		Deleted "Under Qualification" in the Ordering Information section	2
		Added the ESD ratings	4
		Updated the thermal resistance description for θ_{JA} and θ_{JC} , based on the EVB and the continuous power dissipation	4
		Added the 3.3V and 5V fixed output accuracy	5
		Updated the load and line regulation curves	11
		Updated the Soft Start (SS) section	23
		Added the Hot-Plug Application section	27
		Modified the POD error for the wettable flank	35
		Added the Carrier information section	36

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