

# BGA7M1N6

Silicon Germanium Low Noise Amplifier for LTE

## Data Sheet

Revision 3.1 (Min/Max), 2014-02-11

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**Revision History**

Page or Item	Subjects (major changes since previous revision)
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10-15	Min/max values added
<b>Revision 3.0, 2014-02-10</b>	
7	Marking added
10-15	Footnotes updated

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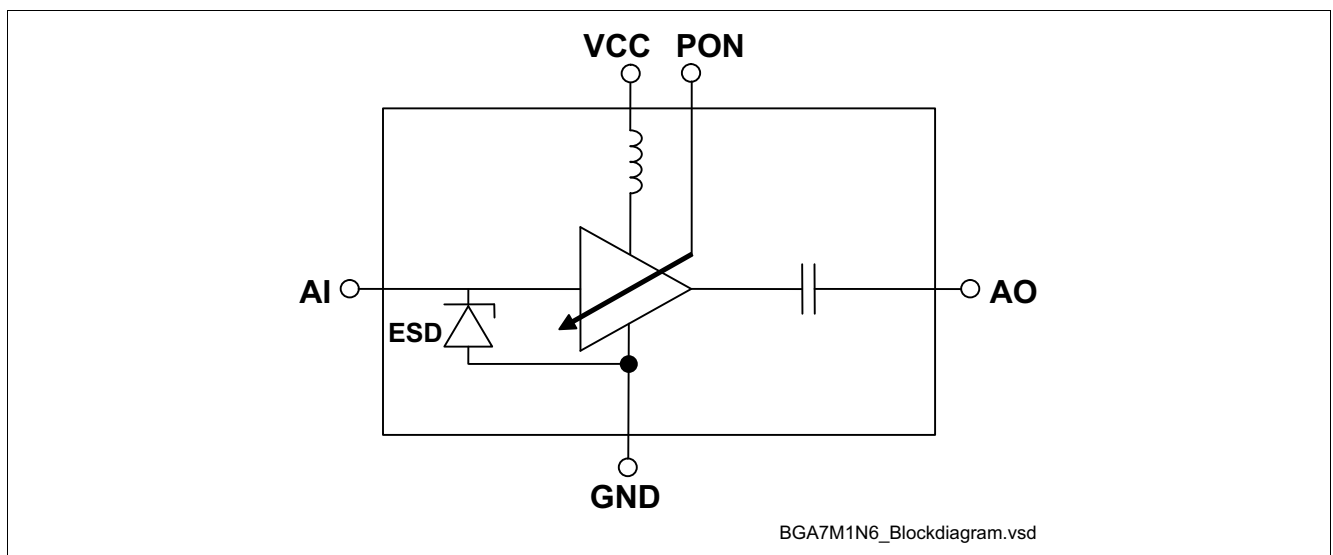
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**Features**

- Insertion power gain: 13.0 dB
- Low noise figure: 0.60 dB
- Low current consumption: 4.4 mA
- Operating frequencies: 1805 - 2200 MHz
- Supply voltage: 1.5 V to 3.3 V
- Digital on/off switch (1V logic high level)
- Ultra small TSNP-6-2 leadless package (footprint: 0.7 x 1.1 mm<sup>2</sup>)
- B7HF Silicon Germanium technology
- RF output internally matched to 50 Ω
- Only 1 external SMD component necessary
- 2kV HBM ESD protection (including AI-pin)
- Pb-free (RoHS compliant) package



**Figure 1 Block Diagram**

Product Name	Marking	Package
BGA7M1N6	B	TSNP-6-2

**Description**

The BGA7M1N6 is a front-end low noise amplifier for LTE which covers a wide frequency range from 1805 MHz to 2200 MHz. The LNA provides 13.0 dB gain and 0.60 dB noise figure at a current consumption of 4.4 mA in the application configuration described in [Chapter 3](#). The BGA7M1N6 is based upon Infineon Technologies' B7HF Silicon Germanium technology. It operates from 1.5 V to 3.3 V supply voltage.

**Pin Definition and Function****Table 1 Pin Definition and Function**

Pin No.	Name	Function
1	GND	Ground
2	VCC	DC supply
3	AO	LNA output
4	GND	Ground
5	AI	LNA input
6	PON	Power on control



## 1 Maximum Ratings

**Table 2 Maximum Ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	$V_{CC}$	-0.3	–	3.6	V	1)
Voltage at pin AI	$V_{AI}$	-0.3	–	0.9	V	–
Voltage at pin AO	$V_{AO}$	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin PON	$V_{PON}$	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin GNDRF	$V_{GNDRF}$	-0.3	–	0.3	V	–
Current into pin VCC	$I_{CC}$	–	–	16	mA	–
RF input power	$P_{IN}$	–	–	0	dBm	–
Total power dissipation, $T_S < \text{tbd. } ^\circ\text{C}^2)$	$P_{tot}$	–	–	60	mW	–
Junction temperature	$T_J$	–	–	150	$^\circ\text{C}$	–
Ambient temperature range	$T_A$	-40	–	85	$^\circ\text{C}$	–
Storage temperature range	$T_{STG}$	-65	–	150	$^\circ\text{C}$	–
ESD capability all pins	$V_{ESD\_HBM}$	–	–	2000	V	according to JESD22A-114

1) All voltages refer to GND-Node unless otherwise noted

2)  $T_S$  is measured on the ground lead at the soldering point

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

### Thermal Resistance

**Table 3 Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$	tbd.	K/W

1) For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

## 2 Electrical Characteristics

### 2.1 Measured RF Characteristics Band 1

**Table 4** Electrical Characteristics:<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 1.8\text{ V}$ ,  $V_{PON,ON} = 1.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 2110 - 2170\text{ MHz}$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.4	5.4	mA	ON-mode
		–	0.2	3	$\mu\text{A}$	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{CC}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	5	10	$\mu\text{A}$	ON-mode
		–	–	1	$\mu\text{A}$	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.1	12.6	14.1	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.65	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	7	10	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	10	16	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	15	19	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	4	7	$\mu\text{s}$	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-7	-3	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	+2	+7	–	dBm	$f_1 = 2140\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

**Table 5 Electrical Characteristics:**<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 2.8\text{ V}$ ,  $V_{PON,ON} = 2.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 2110 - 2170\text{ MHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.5	5.5	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{cc}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	10	15	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.2	12.7	14.2	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.65	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	7	10	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	10	15	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	15	19	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	3	6	μs	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-4	0	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	+3	+8	–	dBm	$f_1 = 2140\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

**2.2 Measured RF Characteristics Band 2**
**Table 6 Electrical Characteristics:**<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 1.8\text{ V}$ ,  $V_{PON,ON} = 1.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 1930 - 1990\text{ MHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.4	5.4	mA	ON-mode
		–	0.2	3	$\mu\text{A}$	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{CC}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	5	10	$\mu\text{A}$	ON-mode
		–	–	1	$\mu\text{A}$	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.2	12.7	14.2	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.6	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	6	8	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	8	11	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	17	21	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	4	7	$\mu\text{s}$	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-7	-3	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	+1	+6	–	dBm	$f_1 = 1960\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

**Table 7 Electrical Characteristics:**<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 2.8\text{ V}$ ,  $V_{PON,ON} = 2.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 1930 - 1990\text{ MHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.5	5.5	mA	ON-mode
		–	0.2	3	$\mu\text{A}$	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{cc}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	10	15	$\mu\text{A}$	ON-mode
		–	–	1	$\mu\text{A}$	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.3	12.8	14.3	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.6	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	6	9	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	8	11	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	17	21	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	3	6	$\mu\text{s}$	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-4	0	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	+3	+8	–	dBm	$f_1 = 1960\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

**2.3 Measured RF Characteristics Band 3**
**Table 8 Electrical Characteristics:**<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 1.8\text{ V}$ ,  $V_{PON,ON} = 1.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 1805 - 1880\text{ MHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.4	5.4	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{CC}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	5	10	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.5	13.0	14.5	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.65	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	6	8	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	6	9	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	17	21	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	4	7	μs	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-8	-4	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	-1	+4	–	dBm	$f_1 = 1840\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

**Table 9 Electrical Characteristics:**<sup>1)</sup>  $T_A = 25\text{ °C}$ ,  $V_{CC} = 2.8\text{ V}$ ,  $V_{PON,ON} = 2.8\text{ V}$ ,  $V_{PON,OFF} = 0\text{ V}$ ,  
 $f = 1805 - 1880\text{ MHz}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	1.5	–	3.3	V	–
Supply current	$I_{CC}$	–	4.5	5.5	mA	ON-mode
		–	0.2	3	$\mu\text{A}$	OFF-mode
Power On voltage	$V_{pon}$	1.0	–	$V_{CC}$	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	$I_{pon}$	–	10	15	$\mu\text{A}$	ON-mode
		–	–	1	$\mu\text{A}$	OFF-mode
Insertion power gain	$ S_{21} ^2$	11.6	13.1	14.6	dB	–
Noise figure <sup>2)</sup>	$NF$	–	0.65	1.2	dB	$Z_S = 50\ \Omega$
Input return loss <sup>3)</sup>	$RL_{in}$	6	8	–	dB	–
Output return loss <sup>3)</sup>	$RL_{out}$	6	9	–	dB	–
Reverse isolation <sup>3)</sup>	$1/ S_{12} ^2$	17	21	–	dB	–
Power gain settling time <sup>4)5)</sup>	$t_S$	–	3	6	$\mu\text{s}$	OFF- to ON-mode
Inband input 1dB-compression point <sup>3)</sup>	$IP_{1dB}$	-5	-1	–	dBm	–
Inband input 3 <sup>rd</sup> -order intercept point <sup>6)3)</sup>	$IIP_3$	+1	+6	–	dBm	$f_1 = 1840\text{ MHz}$ $f_2 = f_1 \pm 10\text{ MHz}$
Stability <sup>5)</sup>	$k$	–	> 1	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain

5) Guaranteed by device design; not tested in production

6) Input power = -30 dBm for each tone

### 3 Application Information

#### 3.1 Application Circuit Schematic Band 1

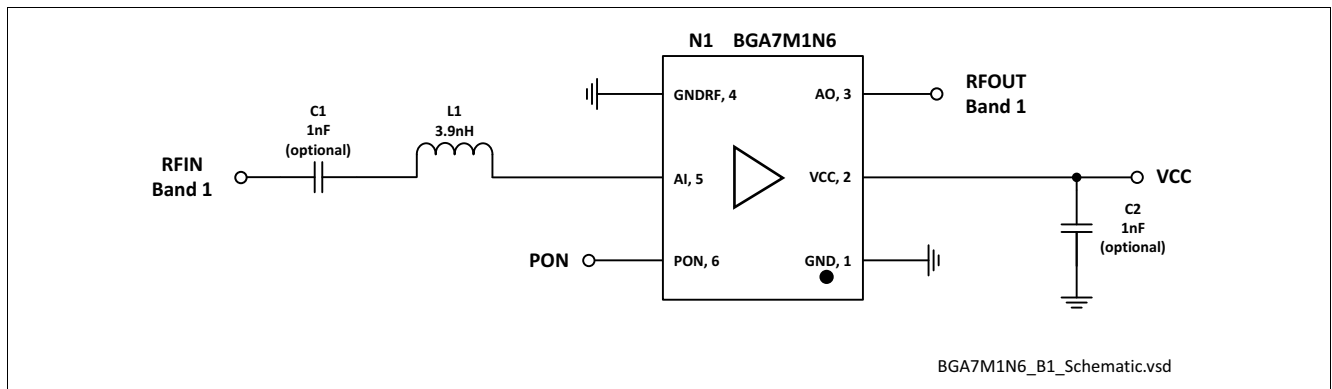


Figure 2 Application Schematic BGA7M1N6

Table 10 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block <sup>1)</sup>
C2 (optional)	$\geq 1\text{nF}^2$	0402	Various	RF bypass <sup>3)</sup>
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7M1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications

2) For data sheet characteristics 1nF used

3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/gpslna.appnotes>.



### 3.2 Application Circuit Schematic Band 2

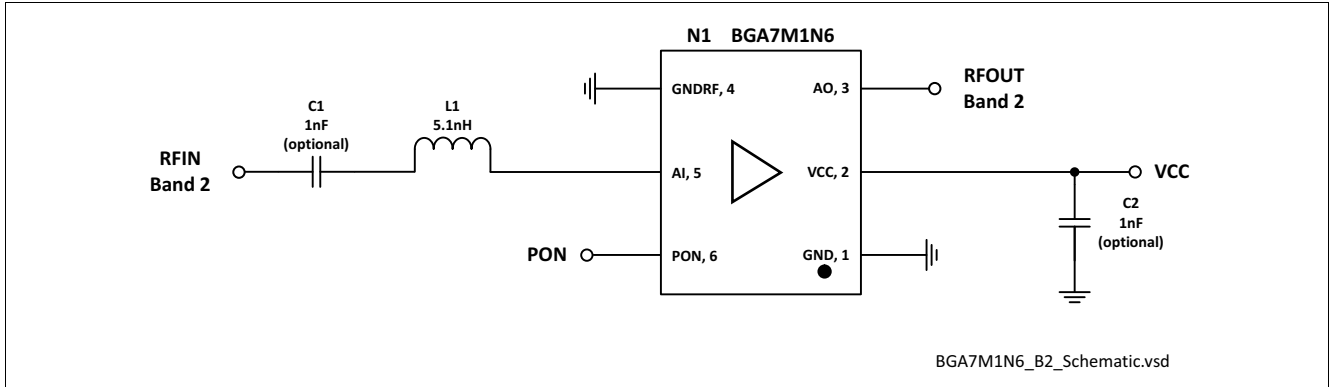


Figure 3 Application Schematic BGA7M1N6

Table 11 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block <sup>1)</sup>
C2 (optional)	$\geq 1\text{nF}^2)$	0402	Various	RF bypass <sup>3)</sup>
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7M1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications

2) For data sheet characteristics 1nF used

3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/gpslna.appnotes>.

### 3.3 Application Circuit Schematic Band 3

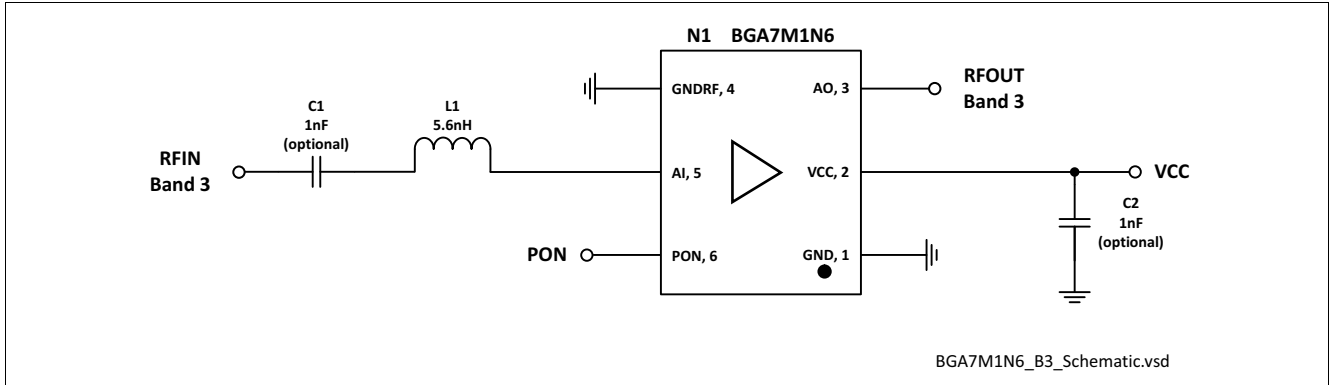


Figure 4 Application Schematic BGA7M1N6

Table 12 Bill of Materials

Name	Part Type	Package	Manufacturer	Function
C1 (optional)	Chip capacitor	0402	Various	DC block <sup>1)</sup>
C2 (optional)	$\geq 1\text{nF}^2)$	0402	Various	RF bypass <sup>3)</sup>
L1	Chip inductor	0402	Murata LQW type	Input matching
N1	BGA7M1N6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in LTE applications

2) For data sheet characteristics 1nF used

3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/gpslna.appnotes>.

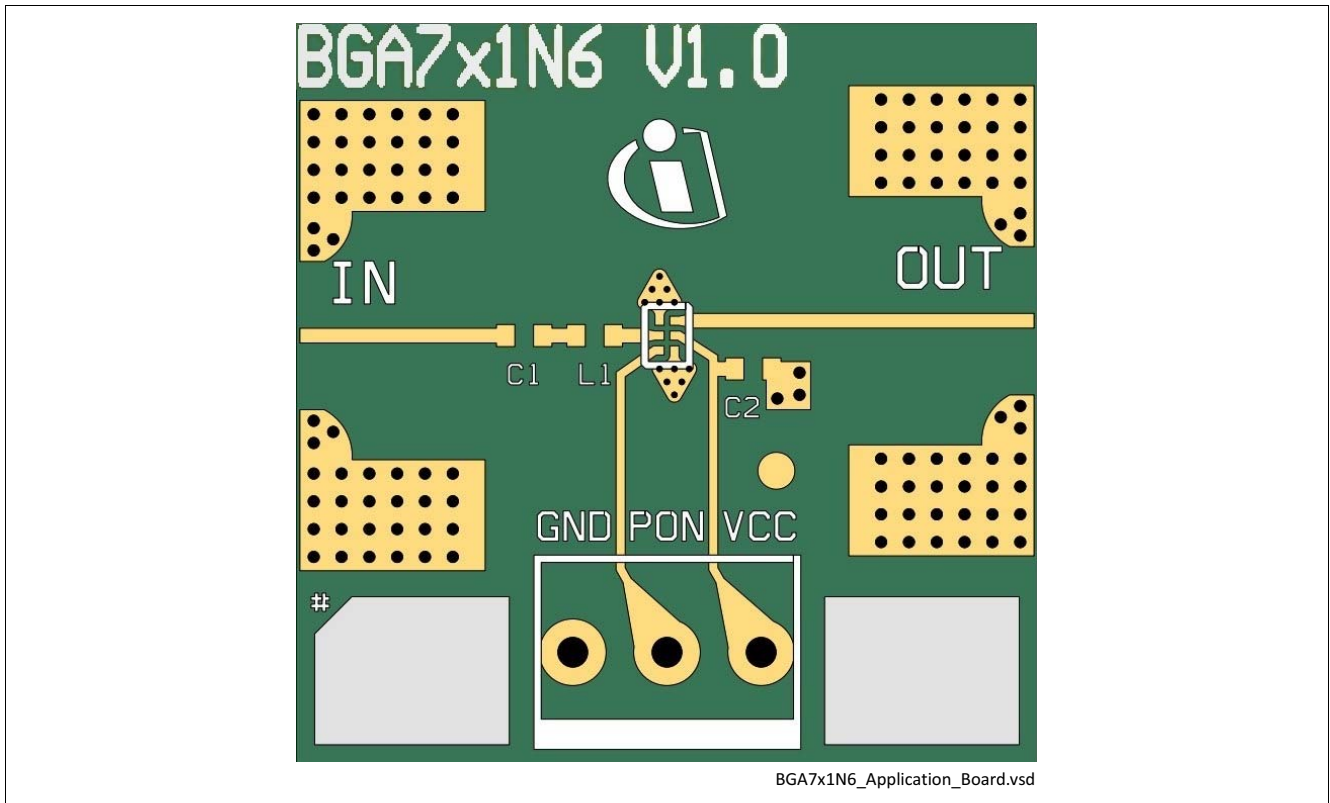


Figure 5 Drawing of Application Board

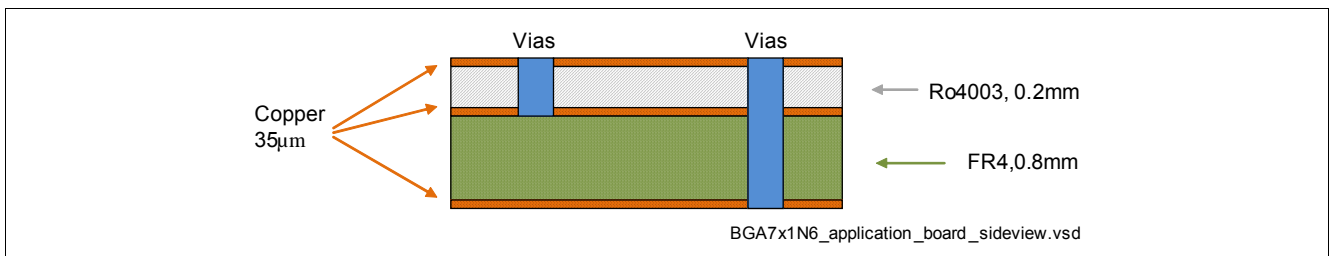


Figure 6 Application Board Cross-Section

## 4 Package Information

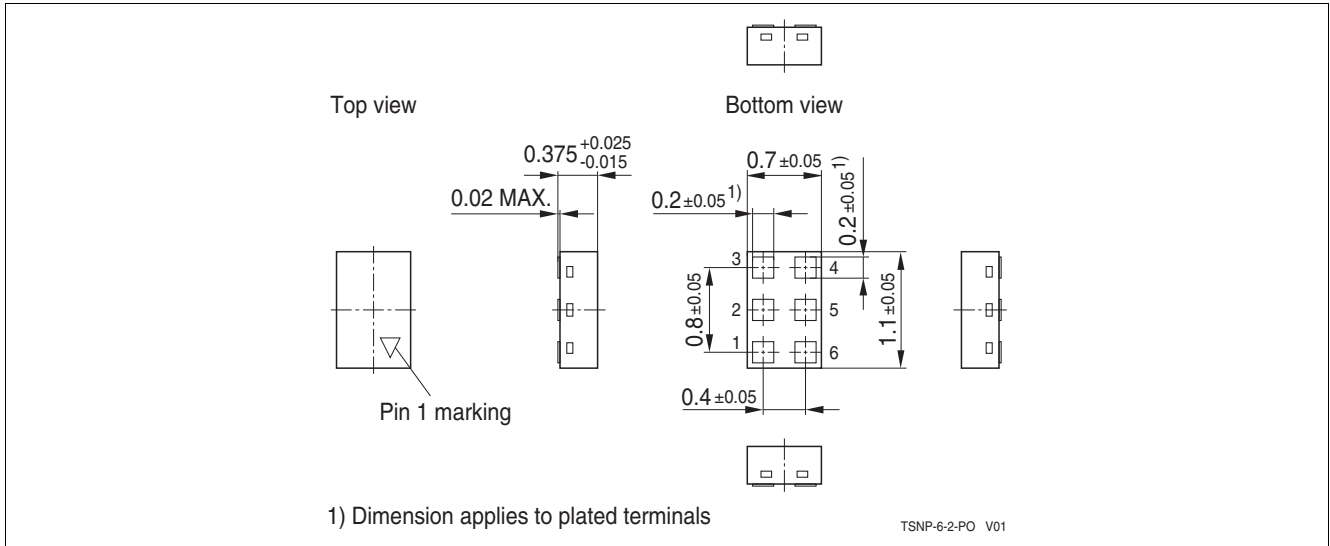


Figure 7 TSNP-6-2 Package Outline (top, side and bottom views)

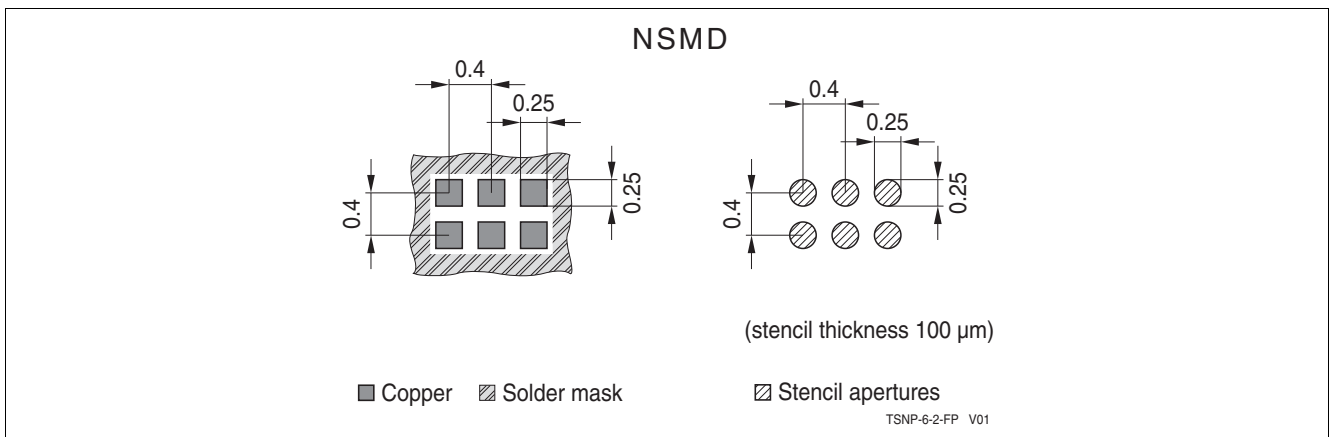


Figure 8 Footprint Recommendation TSNP-6-2

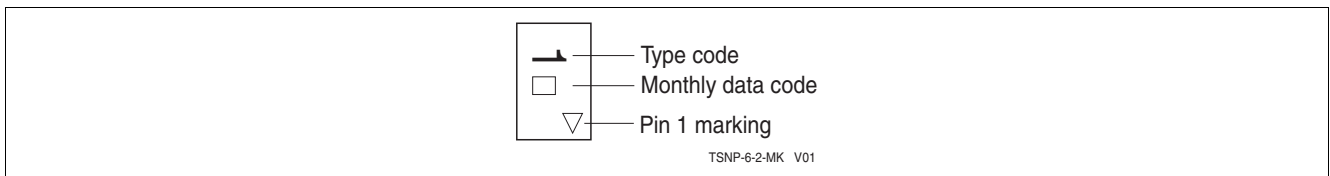


Figure 9 Marking Layout (top view)

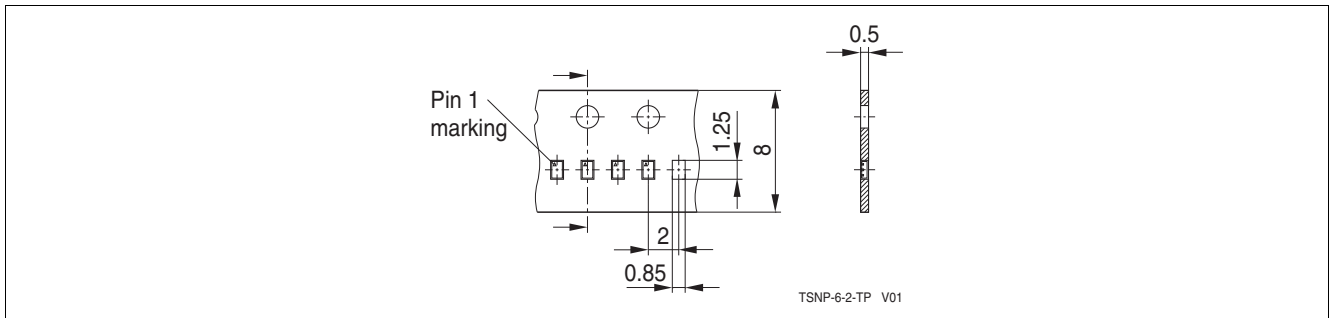


Figure 10 Tape & Reel Dimensions (reel diameter 180 mm, pieces/reel 15000)

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