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AN-1903 LM20136 Evaluation Board

1   Introduction

The LM20136 is a full-featured synchronous buck switching regulator capable of driving up to 6A of load current. This device features a clock synchronization input that allows the switching frequency to be synchronized to an external clock source. The ability to adjust the operating frequency from 500kHz to 1.5MHz gives the designer flexibility in component selection. The LM20136 is capable of converting an input voltage between 2.95V and 5.5V down to an output voltage as low as 0.8V. Fault protection features include cycle-by-cycle current limit, output power good, and output over-voltage protection. The dual function soft-start/tracking pin can be used to control the startup response of the LM20136, and the precision enable pin can be used to easily sequence the LM20136 in sequence-critical applications. The LM20136 is available in a 16-pin HTSSOP package with an exposed pad for enhanced thermal performance.

The LM20136 evaluation board is designed to balance overall solution size and efficiency. The evaluation board measures 1.5" × 1.5" on a two layer PCB with all components placed on the top layer. The power stage and compensation components of the LM20136 evaluation board have been optimized for an input voltage of 5V. The output voltage is nominally 3.3V, but this voltage can be easily changed by replacing one of the feedback resistors (R_{FB1} or R_{FB2}). The control loop compensation of the LM20136 evaluation board has been designed to provide a stable solution over the entire input and output voltage range with a reasonable transient response. The EN pin must be above 1.18V (typ) on the board to initiate switching. The EN pin is tied to V_{IN} with a 10kΩ resistor and can be toggled directly through the enable test point.
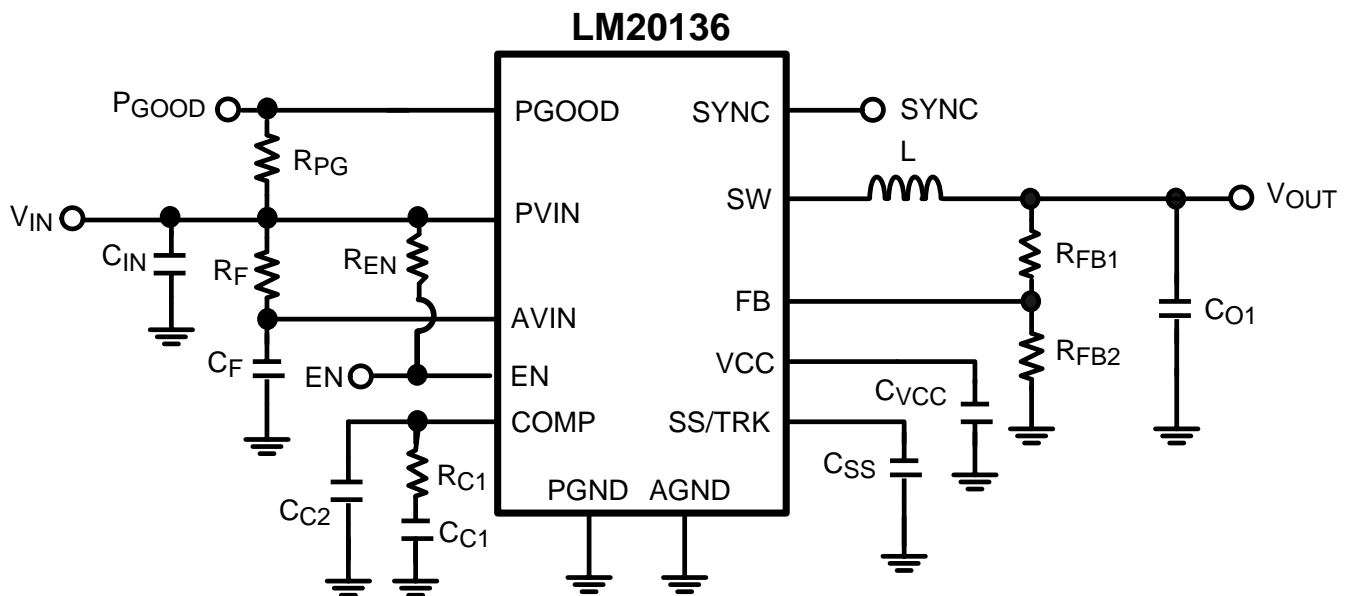

Figure 1. Evaluation Board Schematic

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2 Connection Descriptions

Terminal Silkscreen	Description
VIN	This terminal is the input voltage to the device. The device will operate over the input voltage range of 2.95V to 5.5V. The absolute maximum voltage rating for this pin is 6V.
GND	This terminal is the ground connection to the device. There are two different GND connections on the PCB. One should be used for the input supply and the other for the load.
VOUT	This terminal connects to the output voltage of the power supply and should be connected to the load.
EN	This terminal connects to the enable pin of the device. This terminal should be connected to V_{IN} or driven externally. If driven externally, a voltage typically greater than 1.18V will enable the device. The operating voltage for this pin should not exceed 5.5V. The absolute maximum voltage rating on this pin is 6V.
SS/TRACK	This terminal provides access to the SS/TRK pin of the device. Connections to this terminal are not needed for most applications. The feedback pin of the device will track the voltage on the SS/TRK pin if it is driven with an external voltage source that is below the 0.8V reference. The voltage on this pin should not exceed 5.5V during normal operation. The absolute maximum voltage rating on this pin is 6V.
PGOOD	This terminal connects to the power good output of the device. There is a 10kΩ pull-up resistor from this pin to the input voltage. The voltage on this pin should not exceed 5.5V during normal operation and has an absolute maximum voltage rating of 6V.
SYNC	This terminal connects to the SYNC pin of the device. If this pin is left open the switching frequency will default to approximately 400kHz. The voltage on this pin should not exceed 5.5V during normal operation and has an absolute maximum voltage rating of 6V.
SW	This point allows a scope probe to be connected to observe the switch node voltage.
VOUT TP	This terminal provides an oscilloscope probe connection directly to VOUT to probe the transient response and output voltage ripple.

3 Component Selection

This section provides a walk-through of the design process for the LM20136 evaluation board. Unless otherwise indicated all equations assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, and Volts (V) for voltage.

3.1 Input Capacitor

The required RMS current rating of the input capacitor for a buck regulator can be estimated by the following equation:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D(1 - D)}$$

(1)

The variable D refers to the duty cycle and can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}}$$

(2)

From this equation, it follows that the maximum $I_{CIN(RMS)}$ requirement will occur at a full 6A load current with the system operating at 50% duty cycle. Under this condition, the maximum $I_{CIN(RMS)}$ is given by:

$$I_{CIN(RMS)} = 6A \sqrt{0.66 \times 0.34} = 2.8A$$

(3)

Ceramic capacitors feature a very large I_{RMS} rating in a small footprint, making a ceramic capacitor ideal for this application. A 100μF X5R ceramic capacitor from TDK provides the necessary input capacitance for the evaluation board.

3.2 AVIN Filter

An RC filter should be added to prevent any switching noise on PVIN from interfering with the internal analog circuitry connected to AVIN. This can be seen on the schematic as components R_F and C_F. There is a practical limit to the value of resistor R_F as the AVIN pin will draw a short 60mA burst of current during startup. If R_F is too large the resulting voltage drop can trigger the UVLO comparator. For the evaluation board a 1.0Ω resistor is used for R_F ensuring that UVLO will not be triggered after the part is enabled. A 1.0μF capacitor in conjunction with the 1.0Ω resistor is recommended to filter the input to AVIN.

3.3 Inductor

As per the datasheet recommendations, the inductor value should initially be chosen to give a peak to peak ripple current equal to roughly 30% of the maximum output current. The peak to peak inductor ripple current can be calculated by the equation:

$$\Delta I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

(4)

Rearranging this equation and solving for the inductance reveals that for this application (V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 500kHz, and I_{OUT} = 6A) the nominal inductance value is roughly 1.25μH. However, to allow evaluation of the LM20136 over the full frequency range of operation, a final inductance of 1μH was selected. This results in a peak-to-peak ripple current of 2.2A when the converter is operating from 5V and 500kHz . Once an inductance value is calculated, an actual inductor needs to be selected based on a tradeoff between physical size, efficiency, and current carrying capability. For the LM20136 evaluation board, a TDK SPM6530T-1R0M120 inductor offers a good balance between efficiency (7.8mΩ DCR), size (7.1mm × 6.5mm), and saturation current rating (12A I_{SAT}).

3.4 Output Capacitor

The value of the output capacitor in a buck regulator influences the voltage ripple that will be present on the output voltage, as well as the large signal output voltage response to a load transient. Given the peak-to-peak inductor current ripple ($\Delta I_{P\text{-}P}$) the output voltage ripple can be approximated by the equation:

$$\Delta V_{OUT} = \Delta I_{P\text{-}P} \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

(5)

The variable R_{ESR} above refers to the ESR (Effective Series Resistance) of the output capacitor. As can be seen in the above equation, the ripple voltage on the output can be divided in two parts. One part is attributed to the AC ripple current flowing through the ESR of the output capacitor. The other part is due to the AC ripple current charging and discharging the output capacitor. The output capacitor also has an affect on the amount of droop that is seen on the output voltage in response to a load transient event.

For the evaluation board, a TDK 100μF ceramic capacitor is selected for the output capacitor to provide good transient and DC performance in a relatively small package. From the technical specifications of this capacitor, the ESR is roughly 3mΩ and the effective in-circuit capacitance is approximately 35μF (reduced from 100μF due to the 3.3V DC bias and worse case tolerance). With these values, the peak to peak voltage ripple on the output when operating from a 5V input can be calculated to be about 20mV.

3.5 C_{SS}

A soft-start capacitor can be used to control the startup time of the LM20136. The startup time when using a soft-start capacitor can be estimated by the following equation:

$$t_{SS} = \frac{0.8V \times C_{SS}}{I_{SS}}$$

(6)

For the LM20136, I_{SS} is nominally 5μA. For the evaluation board, the soft-start time has been designed to be roughly 5 ms, resulting in a C_{SS} capacitor value of 33nF.

3.6 C_{VCC}

The C_{VCC} capacitor is necessary to bypass an internal 2.7V subregulator. This capacitor should be sized equal to or greater than 1µF, but less than 10µF. A value of 1µF is sufficient for most applications.

3.7 C_{C1}

The capacitor C_{C1} is used to set the crossover frequency of the LM20136 control loop. Since this board was optimized to work well over the full input voltage, output voltage, and frequency range, the value of C_{C1} was selected to be 1nF. Once the operating conditions for the device are known, the transient response can be optimized by reducing the value of C_{C1} and calculating the value for R_{C1} as outlined in the next section.

3.8 R_{C1}

Once the value of C_{C1} is known, resistor R_{C1} is used to place a zero in the control loop to cancel the output filter pole. This resistor can be sized according to the equation:

$$R_{C1} = \left[\frac{C_{C1}}{C_{OUT}} \times \left[\frac{I_{OUT}}{V_{OUT}} + \frac{1-D}{f_{SW} \times L} + \frac{D \times f_{SW}}{48750 \times V_{IN}} - \frac{1}{2 \times f_{SW} \times L} \right] \right]^{-1}$$

(7)

For stability purposes the device should be compensated for the maximum output current expected in the application.

3.9 C_{C2}

A second compensation capacitor C_{C2} can be used in some designs to provide a high frequency pole, useful for cancelling a possible zero introduced by the ESR of the output capacitor. For the LM20136 evaluation board, the C_{C2} footprint is unpopulated because the low ESR ceramic capacitor used on the output does not contribute a zero to the control loop before the crossover frequency. If the ceramic capacitor on the evaluation board is replaced with a different capacitor having significant ESR, the required value of the capacitor C_{C2} can be estimated by the equation:

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}}$$

(8)

3.10 R_{FB1} and R_{FB2}

The resistors labeled R_{FB1} and R_{FB2} create a voltage divider from V_{OUT} to the feedback pin that is used to set the output of the voltage regulator. Nominally, the output of the LM20136 evaluation board is set to 3.3V, giving resistor values of $R_{FB1} = 30.9$kΩ and $R_{FB2} = 10.0$kΩ. If a different output voltage is required, the value of R_{FB1} can be adjusted according to the equation:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.8} - 1 \right) \times R_{FB2}$$

(9)

R_{FB2} does not need to be changed from its value of 10.0kΩ.

4 Bill of Materials

Table 1. Bill of Materials

| Designator	Description	Part Number	Qty	Manufacturer
U1	Synchronous Buck Regulator	LM20136	1	Texas Instruments
C_{IN}	100µF, 1210, X5R, 6.3V	C3225X5ROJ107M	1	TDK
C_{O1}	100µF, 1210, X5R, 6.3V	C3225X5ROJ107M	1	TDK
C_{O2}	OPEN	N/A	N/A	N/A
L	1.0µH, 7.8 mΩ	SPM6530T-1R0M120	1	TDK
R_F	1.0Ω, 0603	CRCW06031R0J-e3	1	Vishay-Dale
C_F	1.0µF, 0603, X5R, 6.3V	GRM188R60J105KA01	1	Murata
C_{VCC}	1.0µF, 0603, X5R, 6.3V	GRM188R60J105KA01	1	Murata
R_{PG}	10.0kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
R_{C1}	14.3kΩ, 0603	CRCW06031432F-e3	1	Vishay-Dale
C_{C1}	1.0nF, 0603, COG, 50V	GRM1885C1H102JA01	1	Murata
C_{C2}	OPEN	N/A	N/A	N/A
C_{SS}	33.0nF, 0603, X7R, 50V	GRM188R71H333kA61	1	Murata
R_{FB1}	30.9kΩ, 0603	CRCW060330921F-e3	1	Vishay-Dale
R_{FB2}	10.0kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
R_{EN}	10.0kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
VOUT TP	Test Point	131503100	1	Tektronix
EN, PGOOD, SW, SS/RK	Test Points	52F7279	4	Keystone
P1,P2,P3,P4	POWER I/O	160-1026-02-01-00	4	Cambion

5   Performance Characteristics
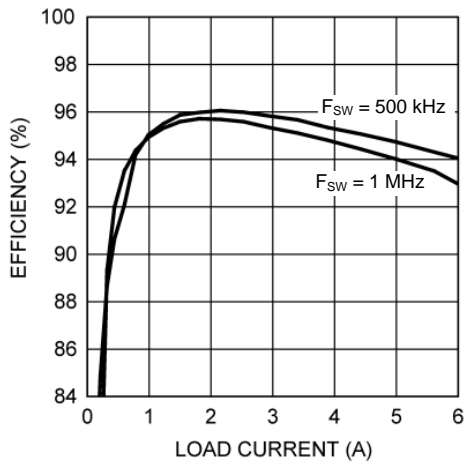
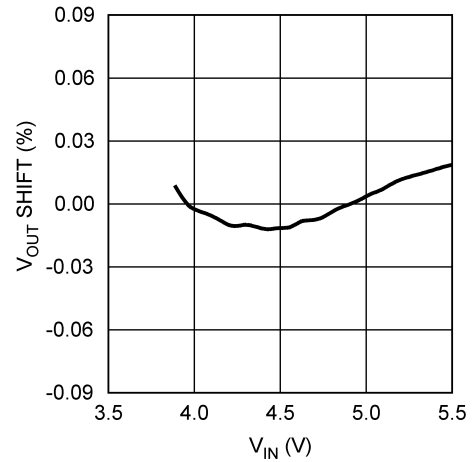**Figure 2. Efficiency vs Load**

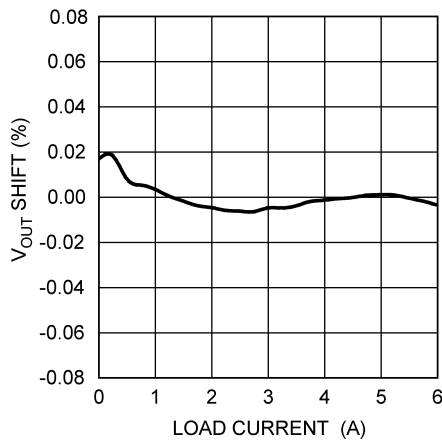**Figure 3. Line Regulation (I$_{LOAD}$ = 6A)**

Figure 4. Load Regulation (V$_{IN}$ = 5V)
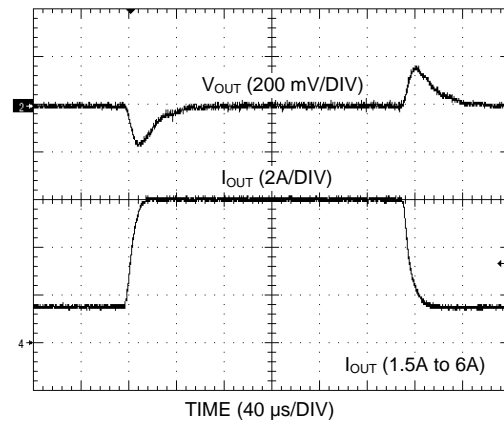
Figure 5. 1.5A to 6A Load Transient Response

Figure 6. Startup Waveform

6   PCB Layout

Figure 7. Top Layer

Figure 8. MidLayer 1
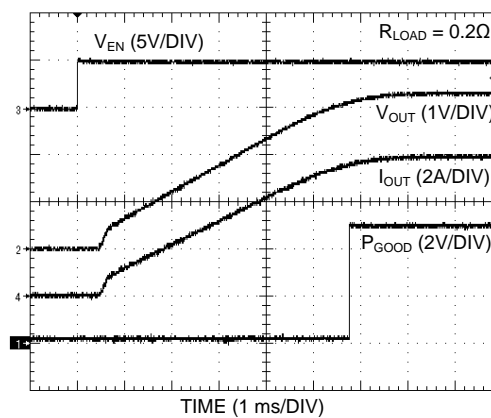

Figure 9. MidLayer 2

Figure 10. Bottom Layer

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