DAC9881 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC9881 Evaluation Module (EVM). It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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1 EVM Overview

This section gives a general overview of the DAC9881 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

1.1 Features

This EVM features the DAC9881 digital-to-analog converter (DAC). The DAC9881EVM is a simple evaluation module designed for quick and easy evaluation of the functionality and performance of the 18-bit, high-resolution, voltage-output, single-channel, and serial input DAC. This EVM features a high-speed serial interface of up to 50 MHz to communicate with any host microprocessor or DSP-based system.

The DAC9881 is designed to work by default for unipolar output range, but it can also be configured for bipolar output range with the addition of an external amplifier and some resistors. The option for bipolar mode of operation is included in the EVM with some minor jumper configuration.

A +5-V precision voltage reference is provided on the board via U3 (REF5050) to supply the necessary external reference voltage to set the DAC9881 output range. The footprint of U3 is compatible with many SO-8 package type reference devices. The user has the flexibility to select the reference supply to set the output range of the DAC9881 differently than what is provided on the board. The family of REF50xx precision reference sources work well with this EVM. In addition, the provision of test points TP1 and TP8, allow users to use their own external reference supply. Typically, TP1 ($V_{REF}L$) must be connected to ground, but it can accept up to ±0.2 V, if necessary. The test point, TP8 ($V_{REF}H$), is typically set to +5 V, but can accept a minimum of +1.25 V and up to a maximum of +5.5 V.

The voltage reference configuration implemented on this EVM uses the Kelvin connection feature of the DAC9881 device. This connection helps minimize the internal errors caused by the changing reference current and its associated circuit impedances.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply requirement for this DAC9881EVM (AVDD and DV_{DD}) is selectable between +3.3 VA and +5 VA via W1 jumper header. The +3.3 VA comes from J6-8, and the +5 VA comes from J6-3. These power supply voltages are referenced to analog ground through J6-5 and J6-6.

The logic voltage, IOV_{DD}, is selectable between +1.8 VD, +3.3 VD and +5 VD via the J3 jumper.

The V_{CC} and V_{SS} that ranges from +15-V to –15-V maximum connect through J6-1 and J6-2 terminals, respectively. All the analog power supplies are referenced to analog ground through J3-6.

CAUTION

To avoid potential damage to the EVM board, ensure that the proper voltages are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

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1.2.2 Reference Voltage

The DAC9881 requires an external reference source to set the DAC's operating voltage output range. Applying the desired voltage between the ranges of 1.25 V to AV_{DD} into the $V_{REF}H$ pin sets the positive range of the DAC9881 output. Also, applying the desired voltage between the range of -0.2 V to +0.2 V into the $V_{REF}L$ pin sets the negative range of the DAC9881 output, although the $V_{REF}L$ pin must nominally be set to zero volts. The voltages applied into the $V_{REF}H$ and $V_{REF}L$ pins set the DAC9881's full output voltage swing.

For optimum performance, the DAC9881 supports a set Kelvin connection to the external reference via $V_{REFH}F$ and $V_{REFH}S$ pins, as well as $V_{REFL}F$ and $V_{REFL}S$ pins. This option for reference configuration minimizes the internal errors caused by the changing reference current and its associated circuit impedances.

A +5-V precision voltage reference is provided for the external reference source of the DAC through REF5050, U3. The power supply for the reference device, U3, is selectable between V_{CC} and +5 VA via W11 to ensure that the correct voltage range of U3 can be set. As mentioned earlier, the family of REF50xx reference devices may be used and the installed device on the EVM changed to provide the desired voltage range required.

The reference voltages, $V_{REF}H$ and $V_{REF}L$ are selectable via jumpers W8 and W4. When shorting pins 1 and 2 of both jumpers, the onboard +5-V reference via REF5050 is selected. Shorting pins 2 and 3 of both jumpers selects the reference voltages that are applied via J4 pins 18 and 20, respectively. These voltages normally come from the host platform that is used to interface with the DAC9881EVM.

The test points TP1 and TP8 are also provided to allow the user to connect other external reference sources if the onboard reference circuit is not desired. The external voltage reference must not exceed the applied power supplies, AV_{DD} and DV_{DD} of the DAC.

CAUTION

When applying an external voltage reference through TP8 or J4-20, ensure that it does not exceed the applied AVDD. This can permanently damage the DAC9881, U1.

1.3 EVM Basic Functions

This EVM is designed as a functional evaluation platform to test certain characteristics of the DAC9881 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, DSP, or a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC9881 EVM. All signals are routed through except SDI because of daisy-chain capability. SDI to the DAC9881 enters the P2 connector (located on the bottom side of the board) at pin 11 and is viewable on TP7. SDO from the DAC9881 exits the board at J1 pin 11 and is viewable on TP6.

An adapter interface card (5–6K Interface Board) is also available to fit and mate with TI's C5000™ and C6000™ DSP Starter Kit (DSK). This alleviates the building of a custom cable. In addition, the Precision Analog Application group of Texas Instruments has other interface boards that are designed to connect to and interface with this EVM as well. For more details or information regarding the 5-6K Interface Board, call Texas Instruments Incorporated or visit the product folder for the tool here: 5-6K Interface Board.

The DAC output can be monitored through pins 2 and 6 of the J4 connector. The DAC output can be switched through W2 for stacking the EVM for daisy-chaining purposes.

A block diagram of the EVM is shown in Figure 1.

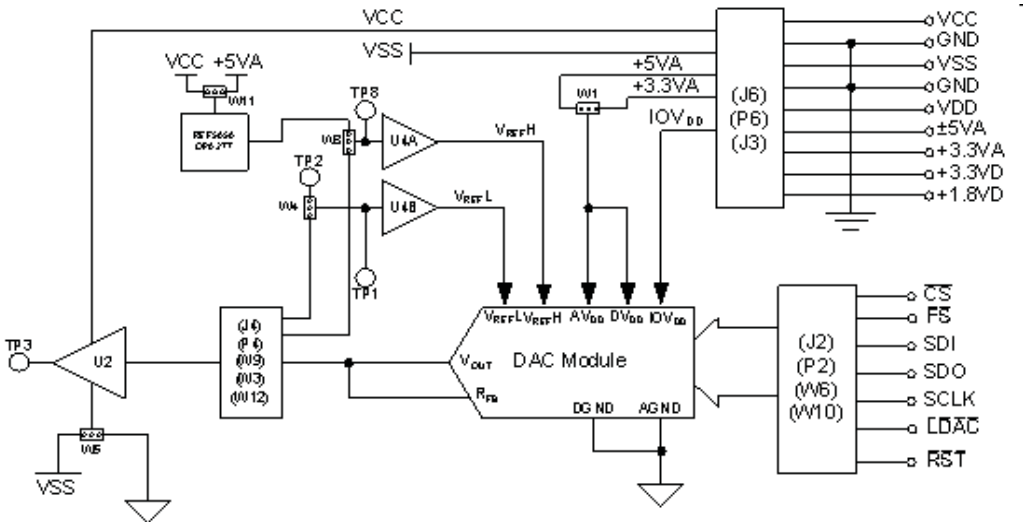


Figure 1. Block Diagram

2 PCB Design and Performance

This section discusses the layout design of the printed-circuit board (PCB), the physical and mechanical characteristics of the EVM, and a brief description of the EVM test performance procedure. The list of components used on this evaluation module also is included in this section.

2.1 PCB Layout

The DAC9881EVM is designed to preserve the performance quality of the DAC as specified in the data sheet. To take full advantage of the EVM's capabilities, use care during the schematic design phase to properly select the right components and to build the circuit correctly. The circuit must include adequate bypassing, identifying, and managing the analog and digital signals, and understanding the components electrical and mechanical attributes.

The main design concern during the layout process is the optimal placement of components and the proper routing of signals. Place the bypass capacitors as close as possible to the pins and be sure to route the analog and digital signals away from each other. A solid ground plane is preferred. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the DUT. The ground plane plays an important role in reducing noise that contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the largest possible trace width allowable in the design. These design practices were applied to the DAC9881EVM PCB.

The DAC9881EVM board is constructed on a four-layer PCB using a copper-clad FR-4 laminate material. The PCB has a dimension of 43,18 mm (1.70 inch) × 82,55 mm (3.25 inch), and the board thickness is 1,57 mm (0.062 inch). Figure 2 through Figure 7 show the individual artwork layers.

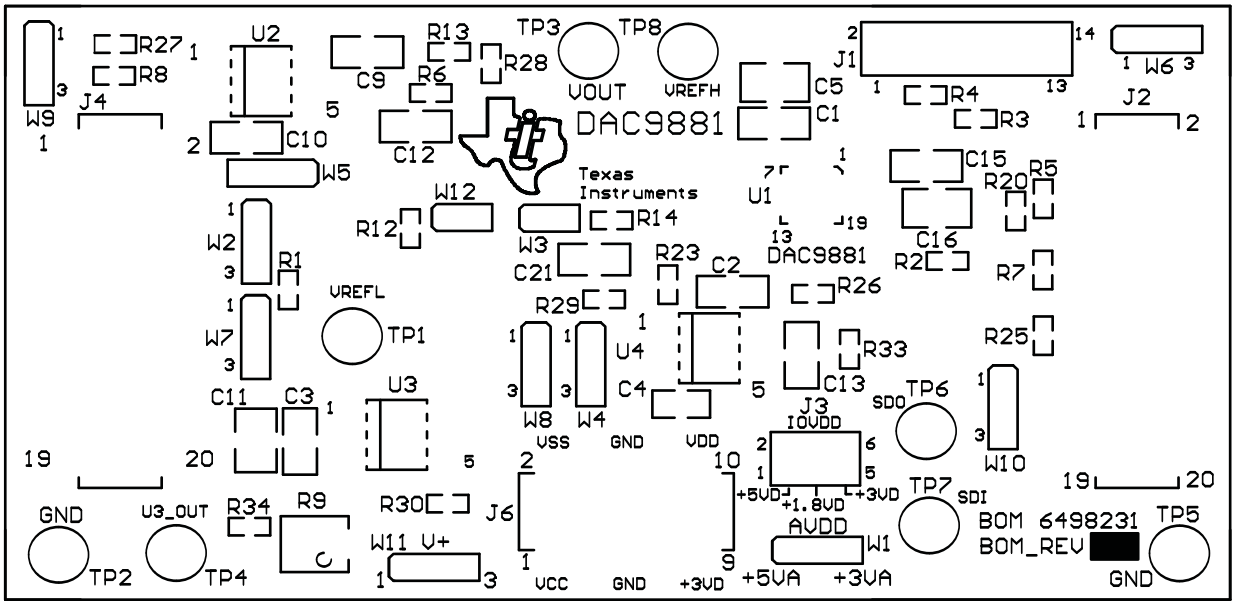


Figure 2. Top Silkscreen

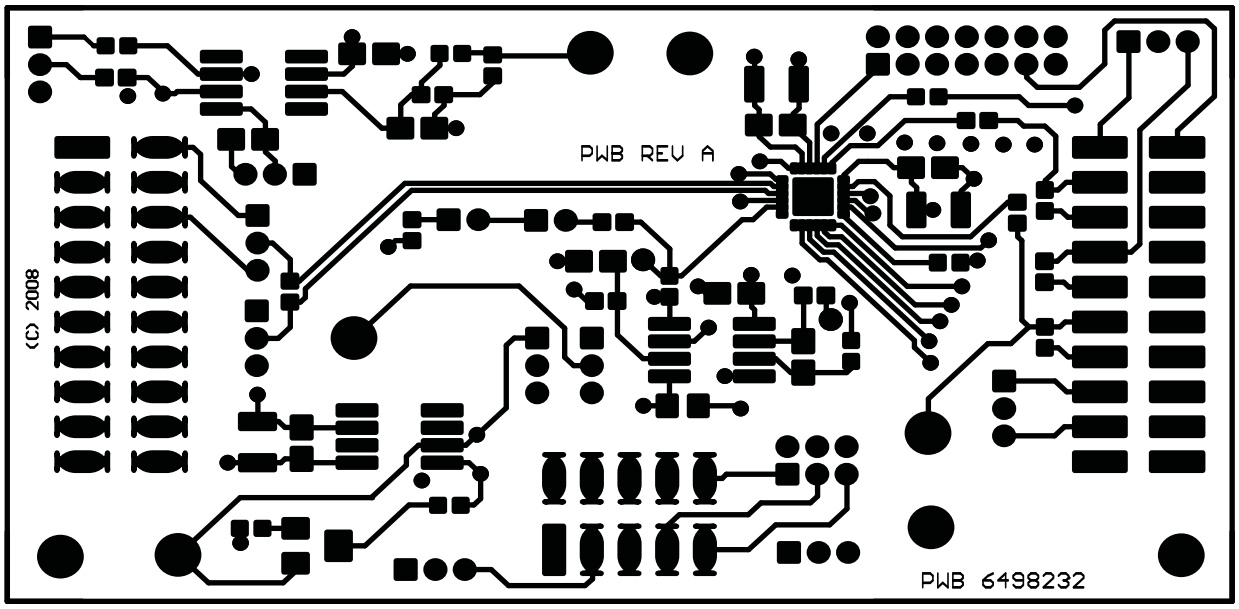


Figure 3. Layer 1, Top Signal Plane

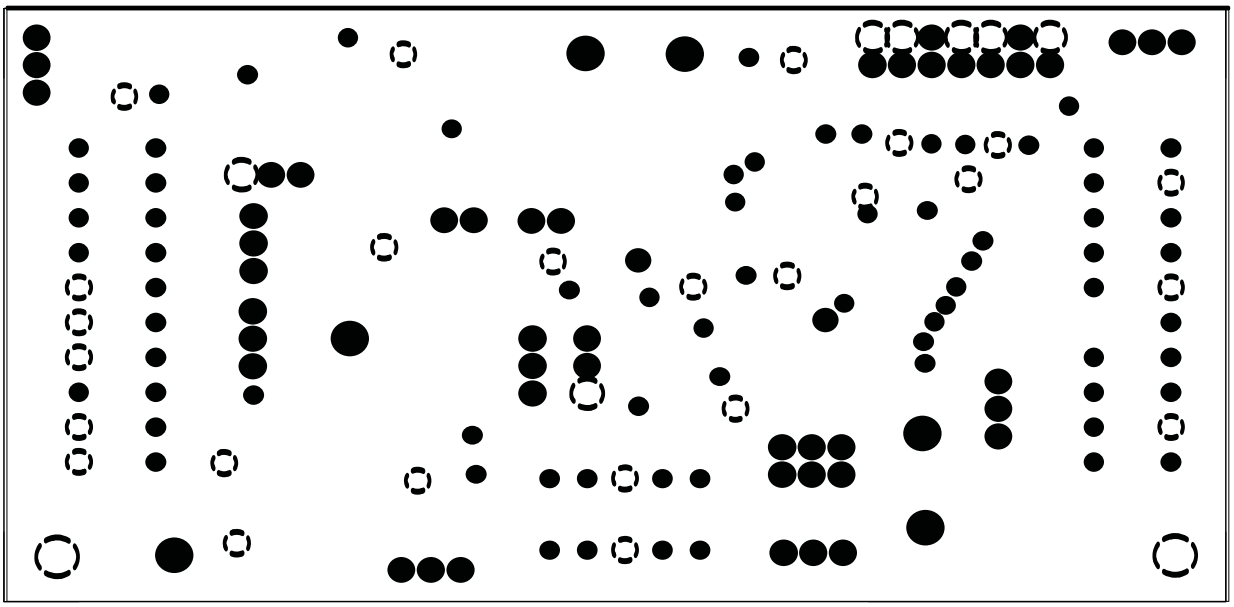


Figure 4. Layer 2, Ground Plane

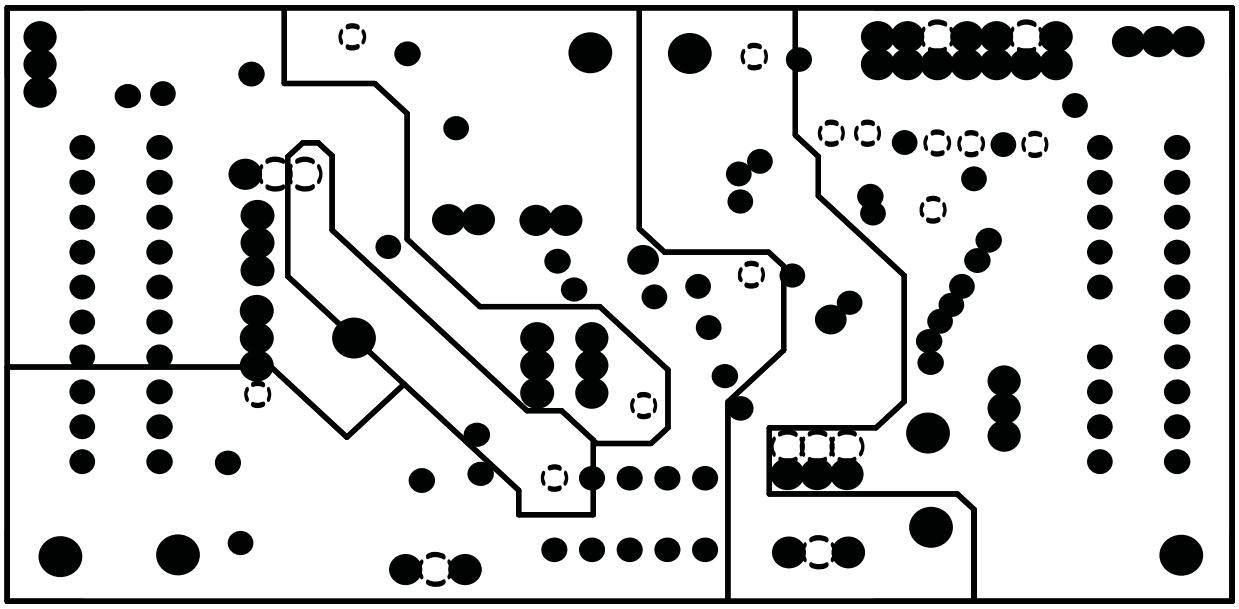


Figure 5. Layer 3, Power Plane

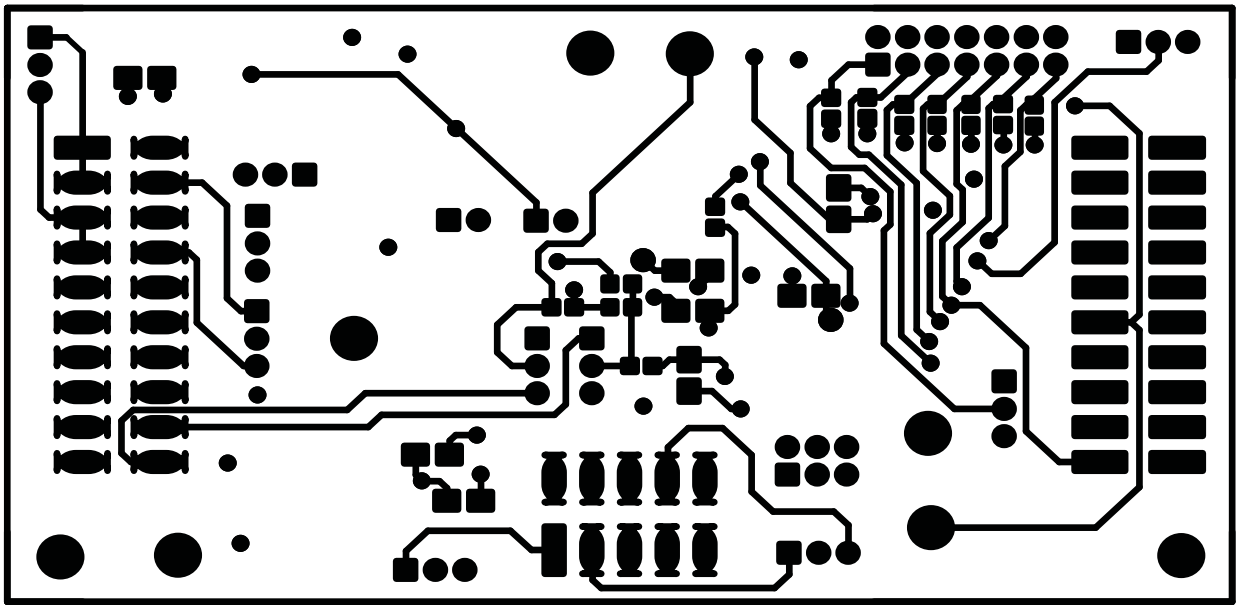


Figure 6. Layer 4, Bottom Signal Plane

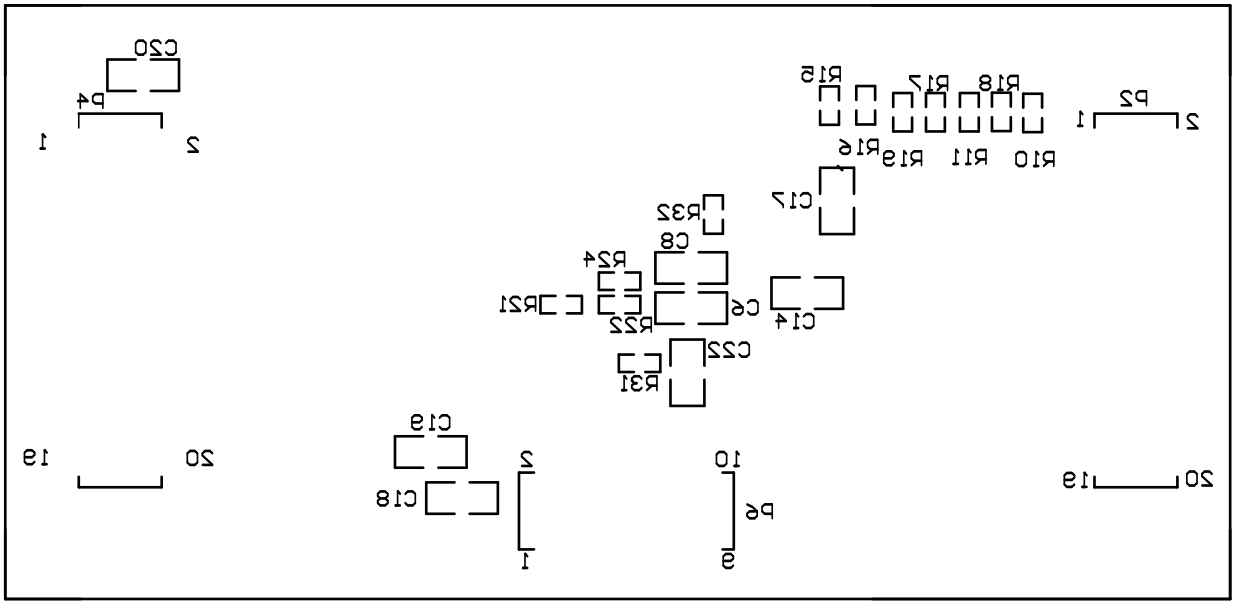


Figure 7. Bottom Silkscreen

3 EVM Performance

The DAC9881 is optimized for DC performance; total harmonic distortion (THD) is typically at -80 dB. The EVM INL and DNL testing is performed using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a personal computer (PC) running LabVIEW™ software. The EVM board is tested for all codes of 262,144 × 8 bits organization and the DAC is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 8 shows the INL and DNL characteristic plots.

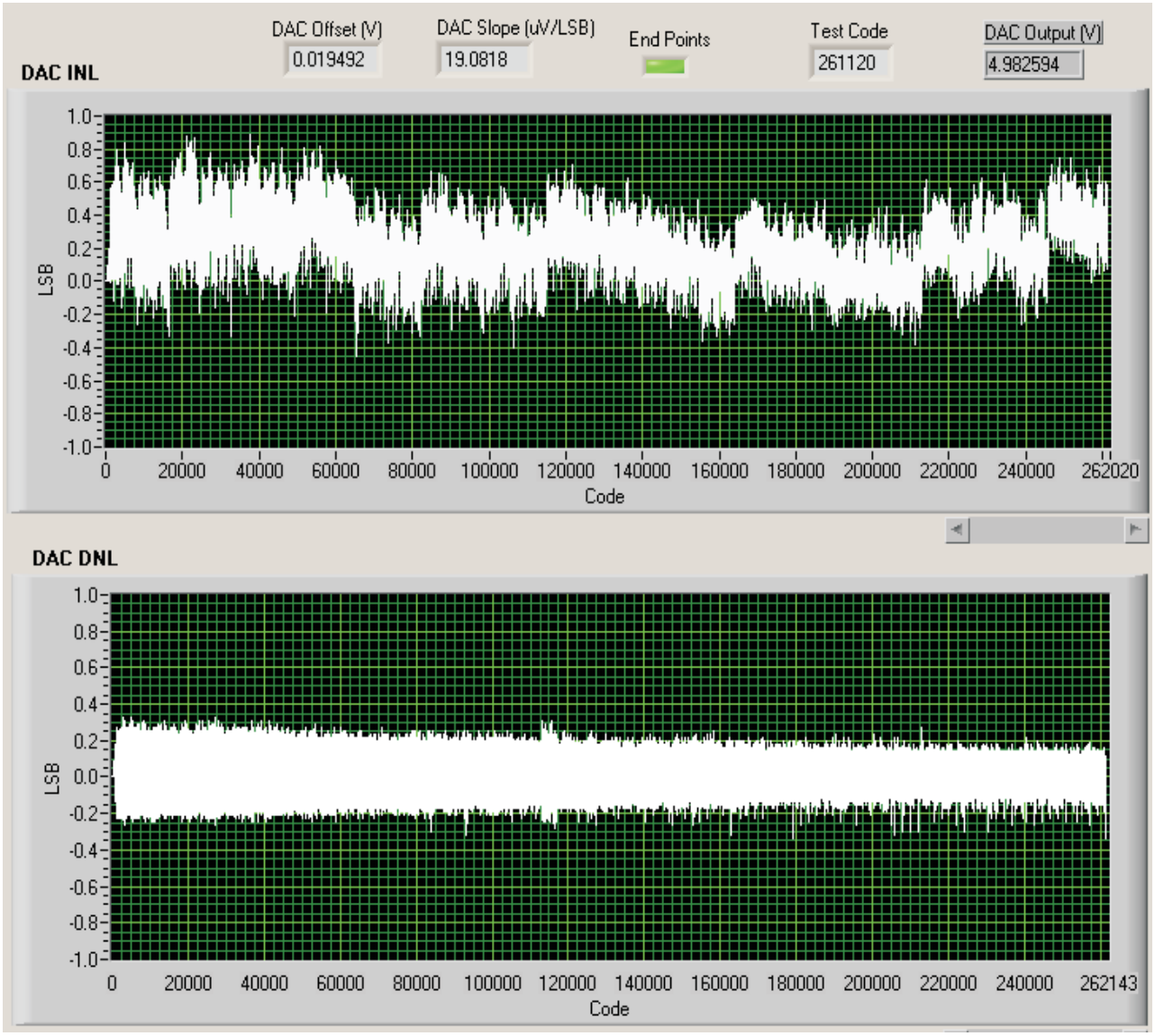


Figure 8. INL and DNL Characteristic Plot

4 Bill of Materials

Table 1. Parts Lists

Qty.	Designators	Description	Manufacturer	Mfg. Part Number
1	N/A	Printed Wiring Board	TI	6498232
6	C1–C4, C15, C17	0.1 µF, 0805, Ceramic, X7R, 50V, 10%	TDK	C2012X7R1H104K
3	C5, C11, C16	10 µF, 1210, Ceramic, X7R, 25V, 20%	TDK	C3225X7R1E106M
2	C6, C13	2200 pF, 0805, Ceramic, C0G, 50V, 5%	TDK	C2012C0G1H222J
3	C8, C12, C14	1000 pF, 0805, Ceramic, C0G, 50V, 5%	TDK	C2012C0G1H102J
4	C9, C10, C18, C19	1 µF, 0805, Ceramic, X7R, 25V, 10%	TDK	C2012X7R1E105K
0	C20	DNP		
2	C21, C22	2.2 µF, 0805, Ceramic, X7R, 16V, 10%	TDK	C2012X7R1C225K
1	J1	7 × 2 × 2 mm Terminal Strip	Samtec	TMM-107-01-T-D
2	J2, J4 (top side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
1	J3	3 × 2 × 2mm Terminal Strip	Samtec	TMM-103-01-T-D
1	J6 (top side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
2	P2, P4 (bottom side)	10 Pin, Dual Row, TH Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
1	P6 (bottom side)	5 Pin, Dual Row, TH Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
6	R1–R4, R8, R20	0.0 Ω 1/10W, 5%, 0603, SMD	Yageo	RC0603JR-070RL
0	R5, R7, R25, R27, R28	DNP		
2	R6, R12	6.04 kΩ, 1/10W, 0.1%, 0603, SMD	BCC	2312-201-76042
1	R9	10 kΩ 4MM TOP ADJ SMD	Bourns	3214W-1-103E
7	R10, R11, R15–R19	10.0 kΩ, 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-0710KL
1	R13	100 Ω, 1/10W, 0.1%, 0603, SMD	BCC	2312-201-71001
1	R14	3.01 kΩ, 1/10W, 0.1%, 0603, SMD	BCC	2312-201-73012
2	R21, R24	2.00 kΩ,1/10W, 0.1%, 0603, SMD	BCC	2312-201-72002
1	R22	95.3 kΩ, 1/10W, 0.1%, 0603, SMD	KOA	RN731JTTDK9532B25
2	R23, R26	49.9 Ω, 1/10W, 0.1%, 0603,	SMD KOA	RN731JTTDK49R9B25
4	R29, R31, R32, R33	10.0 kΩ, 1/10W, 0.1%, 0603,	SMD KOA	RN731JTTDK1002B25
1	R30	470 kΩ, 1/10W, 1%, 0603,	SMD Yageo	RC0603FR-07470KL
1	R34	1.00 kΩ, 1/10W, 1%, 0603,	SMD Yageo	RC0603FR-071KL
8	TP1–TP8	Test Point Turret	Mill-Max	2348-2-00-44-00-00-07-0
1	U1	18-Bit, Buffered Voltage Output DAC	TI	DAC9881SBRGET
1	U2	High Precision Op-Amp	TI	OPA211AIDR
1	U3	5V Precision Voltage Reference	TI	REF5050AID
1	U4	High Precision Dual Operational Amplifier	TI	OPA2277UA
10	W1, W2, W4–W11	3 Pin Mini Header	Samtec	TMM-103-01-T-T
2	W3, W12	2 Pin Mini Header Components	Samtec	TMM-102-01-T-T
ADDITIONAL COMPONENTS				
9	Shunt for items 33 and 34	2mm Shunt – Black	Samtec	2SN-BK-G
1	Shunt for J4	0.100 Shunt – Black (J4 Pins 1 and 2)	Samtec	SNT-100-BK-T
Notes: 1.	P2, P4 and P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.			

5 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

For information about the serial interface and other related topics, see the DAC9881 data sheet (SBAS438).

The EVM board is factory tested and configured to operate in the unipolar output mode.

5.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in the Table 2 to operate in unipolar +5V mode of operation. Figure 9 shows the default jumper configuration as described in table 2.

Table 2. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	The +5VA is used for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC9881.
W2	1-2	Routes V_{OUT} of the DAC9881 to J4-2 for analog output monitoring.
W3	OPEN	Disconnects $V_{REF}H$ from the inverting input of U2 to allow other output mode of configuration.
W4	2-3	Connects the $V_{REF}L$ pin of the DAC9881 to ground.
W5	1-2	Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
W6	2-3	FS signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC9881.
W7	OPEN	Leave this jumper open because R1 is installed. This is the default mode of the EVM when it leaves the factory.
W8	1-2	Routes the onboard +5-V voltage reference, $V_{REF}H$ for the DAC.
W9	1-2	Routes V_{OUT} and R_{FB} from J4-2 and J4-4 (if they are shunted) to the noninverting input of U2 operational amplifier.
W10	OPEN	The $\overline{LDAC}$ signal of the DAC9881 is tied to ground for synchronous update of the DAC9881 output.
W11	1-2	Routes V_{CC} to power the analog supply of the U3 reference device.
W12	OPEN	Disconnects the inverting input of U2 from R12 gain resistor to allow other output mode of configuration.
J1	1-2	The LDAC signal of the DAC9881 is tied to ground for synchronous DAC update operation.
J3	5-6	The DAC9881's IOV_{DD} is powered with +3.3 VD.

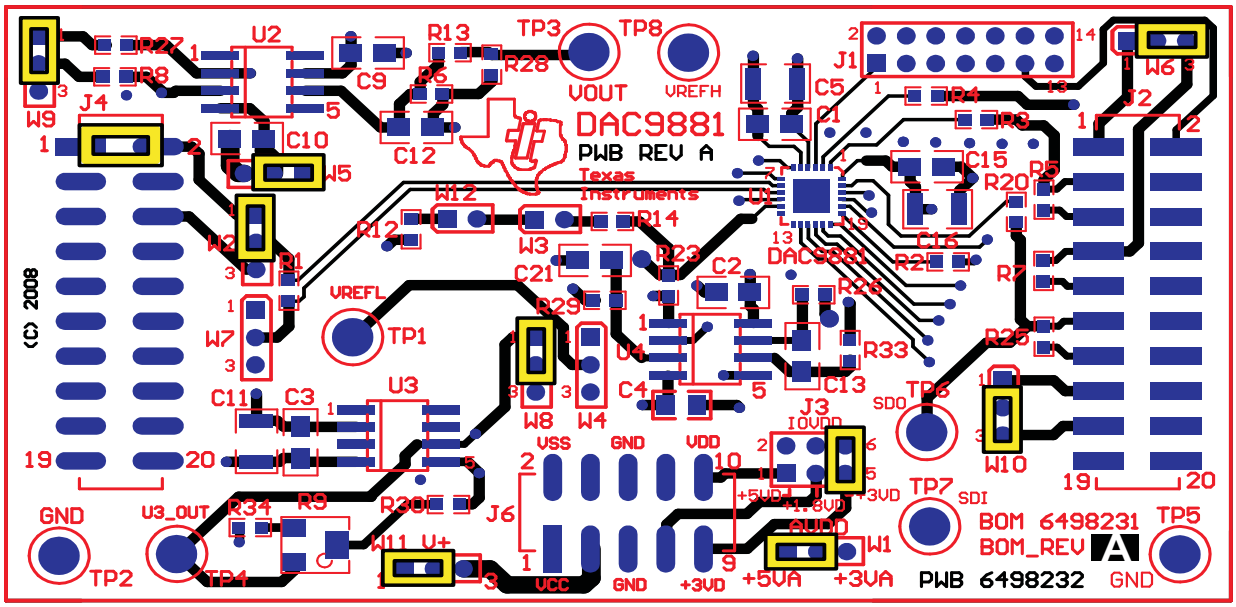


Figure 9. DAC9881 EVM Default Jumper Configuration

5.2 Host Processor Interface

The DAC9881 supports high-speed serial peripheral interface (SPI) to communicate with gate arrays, microprocessors or DSP devices. The user supplied host processor drives the serial communication to the DAC9881EVM. The DAC9881EVM provides the necessary connections to the host processor through connector P2 (located on the bottom side of the board). Proper operation of the DAC9881 depends on the successful communication between the host processor and the EVM. Communication is based on an SPI where CPOL = 0 and CPHA = 0. This means the serial clock dwells low in its inactive state and the input data considered valid on the rising edge of the serial clock.

The following sections describe the basic operation of the digital control inputs to the DAC9881. For more detailed information regarding the DAC9881 digital interface, see the data sheet (SBAS438).

5.3 Digital Control Interface

The DAC9881 can be considered a 3-wire SPI slave device. The host processor must provide a chip select ($\overline{CS}$), the serial data input (SDI) and the serial clock (SCLK) necessary to control the operation of the DAC9881. A fourth control line called load dac ($\overline{LDAC}$) can be used to control the point in time at which the DAC output data is updated. This is useful in applications where multiple DAC9881's need to be updated simultaneously. With the exception of the serial data input (SDI) and the serial data output (SDO) to and from the DAC9881, the EVM incorporates a pass-through connector arrangement to accommodate the digital control interface of the DAC9881 device via J2 (top side) or P2 (bottom side) connectors. The signals on these pass-through connectors are listed as shown in Table 3.

Table 3. Digital Control Interface Signal Mapping for J2/P2 Connectors

Pin Number	Signal	Function
J2.1/P2.1	$\overline{CS}$	Primary synchronization and device enable input for the DAC9881. Host microcontroller's STE signal for SPI interface.
J2.3/P2.3	SCLK	Serial interface clock.
J2.5/P2.5	CLKR	Unused.
J2.7/P2.7	FS	Secondary synchronization and device enable input for the DAC9881. Host microcontroller's STE signal for SPI interface or FS signal from DSP host system.
J2.9/P2/9	FSR	Unused.
J2.11	SDO	Serial Data Output.
P2.11	SDI	Serial Data Input.
J2.13/P2.13	DR	Unused.
J2.15/P2.15	$\overline{LDAC}$1	GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.17/P2.17	$\overline{LDAC}$2	Alternate GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.19/P2.19	$\overline{RST}$	GPIO signal to control $\overline{RST}$ for DAC reset function.
J2.2/P2.2	PDN	GPIO signal to control PDN for hardware power down.
J2.4/P2.4 J2.10/P2.10 J2.18/P2.18	GND	Signal Ground
J2.6/P2.6 J2.8/P2.8 J2.12/P2.12 J2.14/P2.14 J2.16/P2.16 J2.20/P2.20	GPIOs	Unused

5.3.1 $\overline{CS}$ Signal

The signals found on J2 pins 1 and 7 of the EVM are used to control the chip select input of the DAC9881. These signals are configurable via wire jumper W6. Either signal can be chosen to drive the DAC9881 $\overline{CS}$ pin. The basic function of the $\overline{CS}$ input signal is to enable serial communication with the DAC9881. This signal must be held low while the host processor is accessing the DAC serial shift register. The low-to-high transition of this signal transfers the content of the serial shift register to the DAC input register. The $\overline{CS}$ input can also be used to update the DAC output if the $\overline{LDAC}$ is tied to ground.

5.3.2 SDI Signal

The SDI signal is the serial data input that is loaded into the DAC's input register. The data frame sent to the DAC9881 is 24-bits wide. The first 6 bits are 'don't care', the seventh bit is the most-significant bit (MSB) of the DAC data and the 24th bit is the least significant bit (LSB) of the 18-bit DAC data. The serial data input is driven from the SPI master on the falling SCLK edge and sampled by the DAC9881 on the rising edge of the serial clock.

5.3.3 SCLK Signal

The host processor must provide an SCLK signal which is used to advance serial data through the DAC's serial shift register. The serial clock rate can operate at speeds up to 50 MHz. The 6 don't care bits plus 18-bit data is shifted out of the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the DAC's serial shift register. After 24-bits are transferred or 24 SCLK cycles are generated, the bus master must take the $\overline{CS}$ signal high. If the $\overline{CS}$ signal is held low and more than 24 SCLK cycles are applied, the last SCLK cycle is considered the least significant bit (LSB) of the 18-bit data stream loaded into the DAC's serial shift register.

5.3.4 $\overline{LDAC}$ Signal

The $\overline{LDAC}$ signal is a control input signal that can be used to update the DAC output at a specific point in time. This signal is active low and can be triggered synchronously or asynchronously. If $\overline{LDAC}$ is held low, the DAC9881 output updates with the rising edge of the $\overline{CS}$ input. If multiple DAC9881 devices share the databus in daisy-chain fashion, a common LDAC signal can be used to update multiple DAC outputs simultaneously.

5.3.5 $\overline{RST}$ Signal

The $\overline{RST}$ signal is the control input used to reset the DAC output to a known state which is determined by the logic level of the RSTSEL pin when the $\overline{RST}$ pin is asserted. If RSTSEL is tied to DGND, the DAC output latch is cleared (0 V) and V_{OUT} is minimum scale (i.e., $V_{REF}L$). If RSTSEL is tied to VDD, the DAC output latch is set to midscale and V_{OUT} is equal to ($V_{REF}H - V_{REF}L$)/2. This pin is an active low input.

5.3.6 PDN Signal

The PDN signal is the control input provided for hardware power-down function of the device. This signal is active high, so when the PDN pin is driven high, the device goes into power-down mode, which reduces its power consumption. The DAC9881 voltage output pin is connected to ground through an internal 10-kΩ resistor while in power-down mode.

5.4 Analog Output

The DAC9881 voltage output is buffered internally and offers a force and sense output configuration to allow the loop around the output amplifier to be closed as near to the load as possible. The EVM closes this loop by default with R1 installed, so if the loop at the load needs to be closed, R1 must be removed and jumpers W2 and W7 used to connect V_{OUT} and R_{FB} to the connector J4. The selected pins of the J4 connector, as dictated by the jumper positions of W2 and W7 jumpers, can then be connected to the load to close the loop.

The EVM includes an external operational amplifier, U2, as an option for other output signal-conditioning circuitry for the DAC output. Although the buffered output of the DAC9881 can be monitored through J4 pin 2, the optional external buffer output (if the DAC output is connected to it) can be monitored through the TP3 test point.

The external operational amplifier, U2, is set to unity gain configuration by default to maintain the DAC9881 unipolar output mode of operation. But it can be modified by simple jumper settings to achieve other modes of operation. The following sections describe the different configurations of the output amplifier, U2.

5.4.1 Bipolar Output Operation

Using the external $V_{REF}H$ to offset the DAC output and extend the range of operation to achieve a bipolar mode of operation is possible by properly configuring the output operational amplifier, U2. This configuration is described in Table 4.

Table 4. Bipolar Output Operation Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the noninverting input of the output operational amplifier, U2.
W3	CLOSE	Connect $V_{REF}H$ to the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.
W12	OPEN	Disconnect negative input of the operational amplifier from the gain resistor, R12.

5.4.2 Output Gain of Two Operation

The configuration as described on Table 5 yields a voltage output mode of operation that is gained by two.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the noninverting input of the output operational amplifier, U2.
W3	OPEN	Disconnect $V_{REF}H$ from the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.
W12	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R12.

5.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all operational amplifiers under certain conditions may become unstable depending on the operational amplifier configuration, gain, and load value. These are just a few factors that can affect operational amplifiers stability performance and must be considered when implementing.

In unity gain, the OPA211 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor even improves the capacitive load drive capability.

Table 6 shows the jumper setting configuration for a capacitive load drive.

Table 6. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the noninverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the noninverting input of the output operational amplifier, U2.
W3	OPEN	Disconnect $V_{REF}H$ to the inverting input of the operational amplifier, U2.
W5	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.
W12	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R12.

5.5 Jumper Setting

Table 7 shows the function of each specific jumper setting of the EVM.

Table 7. Jumper Setting Function

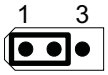
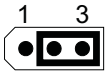
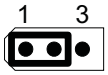
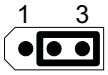
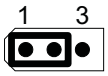
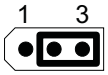
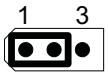
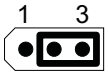
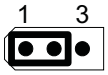
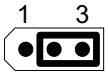
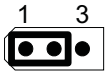
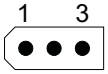
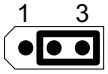
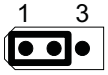
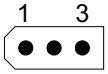
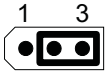
Reference	Jumper Setting	Function
W1		Routes +5VA for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC9881.
		Routes +3.3VA for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC9881.
W2		Routes V_{OUT} to J4-2.
		Routes V_{OUT} to J4-6.
W3		Connect $V_{REF}H$ to the inverting input of U2 for DAC9881's bipolar mode of operation.
		Disconnects $V_{REF}H$ from the inverting input of U2 to allow other output mode of configuration.
W4		Routes the reference voltage from J4 pin 18 for the $V_{REF}L$ pin of the DAC9881.
		Connects the $V_{REF}L$ pin of the DAC9881 to ground.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		$\overline{CS}$ signal from J2-1 is routed to drive the $\overline{CS}$ signal of the DAC9881.
		FS signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC9881.
W7		Routes the reference feedback, R_{FB}, pin of the DAC9881 to J4 pin 4 to provide the option to close the output operational amplifier, U2, loop as close as possible to the load.
		Leave this jumper open if R1 is installed. This is the default mode of the EVM when it comes out of the factory.
		Routes the reference feedback, R_{FB}, pin of the DAC9881 to J4 pin 8 to provide the option to close the output operational amplifier, U2, loop as close as possible to the load.
W8		Routes the onboard +5-V voltage reference, $V_{REF}H$ for the DAC.
		Disconnect onboard or external positive voltage reference, $V_{REF}H$ for the DAC via U5A or J1 pin 20. Allows user reference voltage to connect via TP1.
		Routes the external positive voltage reference, $V_{REF}H$ for the DAC via J1 pin 20.

Table 7. Jumper Setting Function (continued)

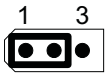
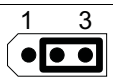
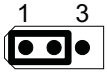
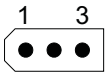
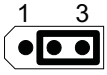
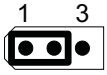
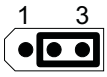
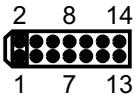
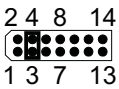
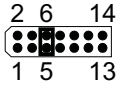
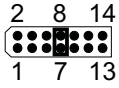
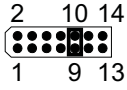
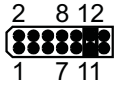
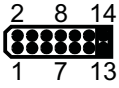
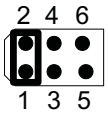
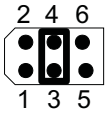
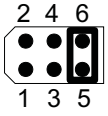
Reference	Jumper Setting	Function
W9		Routes V_{OUT} and R_{FB} from J4-2 and J4-4 to the noninverting input of U2 operational amplifier.
		Routes V_{OUT} and R_{FB} from J4-6 and J4-8 to the noninverting input of U2 operational amplifier.
W10		$\overline{\text{LDAC}}$1 signal from J2-15 is routed to drive the $\overline{\text{LDAC}}$ signal of the DAC9881.
		The $\overline{\text{LDAC}}$ signal of the DAC9881 is tied to ground for synchronous update of the DAC9881 output.
		$\overline{\text{LDAC}}$2 signal from J2-17 is routed to drive the $\overline{\text{LDAC}}$ signal of the DAC9881.
W11		Routes V_{CC} to power the analog supply of the U3 reference device.
		Routes +5VA to power the analog supply of the U3 reference device.
W12		Connect the inverting input of U2 to R12 gain resistor for DAC9881's 2x gain of operation.
		Disconnects the inverting input of U2 from R12 gain resistor to allow other output mode of configuration.
J1		If jumper is installed on pins 1 and 2, the $\overline{\text{LDAC}}$ signal of the DAC9881 is tied to ground for synchronous DAC update operation.
		If jumper is installed on pins 3 and 4, the RSTSEL pin of the DAC9881 is tied to ground so that the DAC output is at 0 V on power up or reset to the device is issued.
		If jumper is installed on pins 5 and 6, the GAIN pin of the DAC9881 is tied to IOV_{DD} so that the DAC output is set with a gain of two output.
		If jumper is installed on pins 7 and 8, the USB/$\overline{\text{BTC}}$ pin of the DAC9881 is tied to ground so that the DAC's input data format is set for 2s complement format.
		If jumper is installed on pins 9 and 10, the $\overline{\text{RST}}$ pin of the DAC9881 is tied to ground so that the DAC is forced into hardware reset mode.
		If jumper is installed on pins 11 and 12, the PDN pin of the DAC9881 is tied to IOV_{DD} so that the DAC is forced into power-down status.
		If jumper is installed on pins 13 and 14, the SDOSEL pin of the DAC9881 is tied to ground so that the DAC device can be operated in daisy-chain mode.

Table 7. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
J3		The DAC9881's IOV_{DD} is powered with +5VD.
		The DAC9881's IOV_{DD} is powered with +1.8VD.
		The DAC9881's IOV_{DD} is powered with +3.3VD.
Legend:  Indicates the corresponding pins that are shorted or closed.		

5.6 DAC9881EVM Schematic

The DAC9881EVM schematic appears as the last page of this manual.

6 Using the DAC9881EVM with DXP

The DAC9881EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary code required to output various signals and waveforms from the DAC9881EVM. The DAC9881EVM-DXP kit combines the DAC9881EVM board with the TMS320VC5509 DSP-based modular motherboard (MMB0), and includes DXP software for evaluation using any available USB port.

DXP is a program for controlling the digital input signals such as the clock, LDAC, $\overline{CS}$, and SDI. Wave tables are built into the DSP software to allow Sine, Ramp, Triangle, and Square wave signals to be generated by the DAC9881. Straight DC outputs also can be obtained.

The DAC9881EVM-PDK is controlled by loading a DAC EVM configuration into the MMB0. For complete information about installing and configuring DXP, see the *DXP User's Guide*, available for download from the TI Web site.

This section covers the specific operation of the DAC9881EVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DAC9881EVM.

6.1 Hardware

The hardware consists of two main components, the first is the DAC9881EVM itself and the other is a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507DSP which controls the DAC9881 serial interface.

The hardware needs to be configured such that the DAC9881EVM is plugged onto the board onto the MMB0 aligning female connectors P4, P2, and P6 (bottom side of the DAC9881EVM) with male connectors J4, J7, and J5 on the MMB0. Exercise caution when assembling the boards as it is possible to misalign the connectors. Do not connect the MMB0 to your PC before installing the DXP software. Installing the software ensures that the necessary drivers are properly loaded to run the hardware.

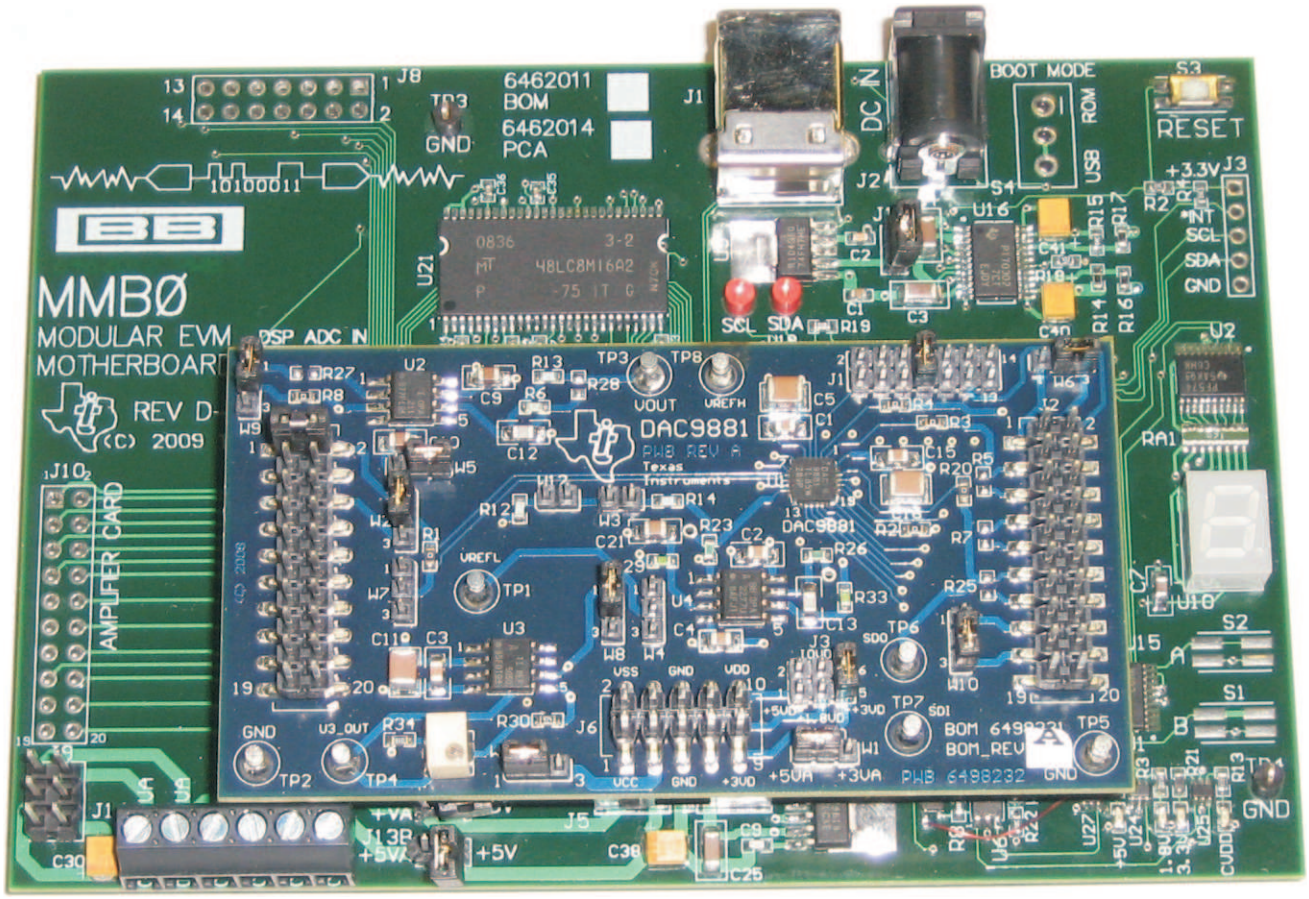


Figure 10. MMB0 with DAC9881EVM Installed

6.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6-V AC/DC converter is all that is necessary. Ensure that J12 on the MMB0 board is closed before connecting the AC/DC adapter to the DC In connector of the MMB0. This supply provides all power to the digital portion of the DAC9881EVM as well as all necessary power for the DSP. Analog power for the DAC9881EVM must be supplied externally via J14 – a 6-position screw terminal mounted in the lower left corner of the MMB0 board.

CAUTION

When using external power supplies applied to J14 on the MMB0, ensure that all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

From left to right, the screw terminal connections of J14 are –VA, +VA, +5VA, –5VA, +5VD, and GND. The DAC9881 board has power requirements as described in Section 1.2. The analog power for Vcc (+VA), Vss (-VA), and +5VA may be applied directly to the screw terminals at J14 on the MMB0 (referenced to the GND terminal).

Connect the MMB0 power supply to DC IN connector (J2) on the MMB0. Connect all other analog supplies as necessary to J14 on the MMB0 (referenced to the ground terminal).

6.3 Software – Running DXP

Install DXP on a laptop or personal computer running Windows XP as per the detailed instruction in the DXP User's Guide (SBAU146). Run the DXP program by clicking on the DXP icon on your desktop or by browsing to your installation directory.

Before you can use DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the ***DAC*** menu. Choose the DAC configuration file for the DAC9881 EVM as shown in Figure 11.

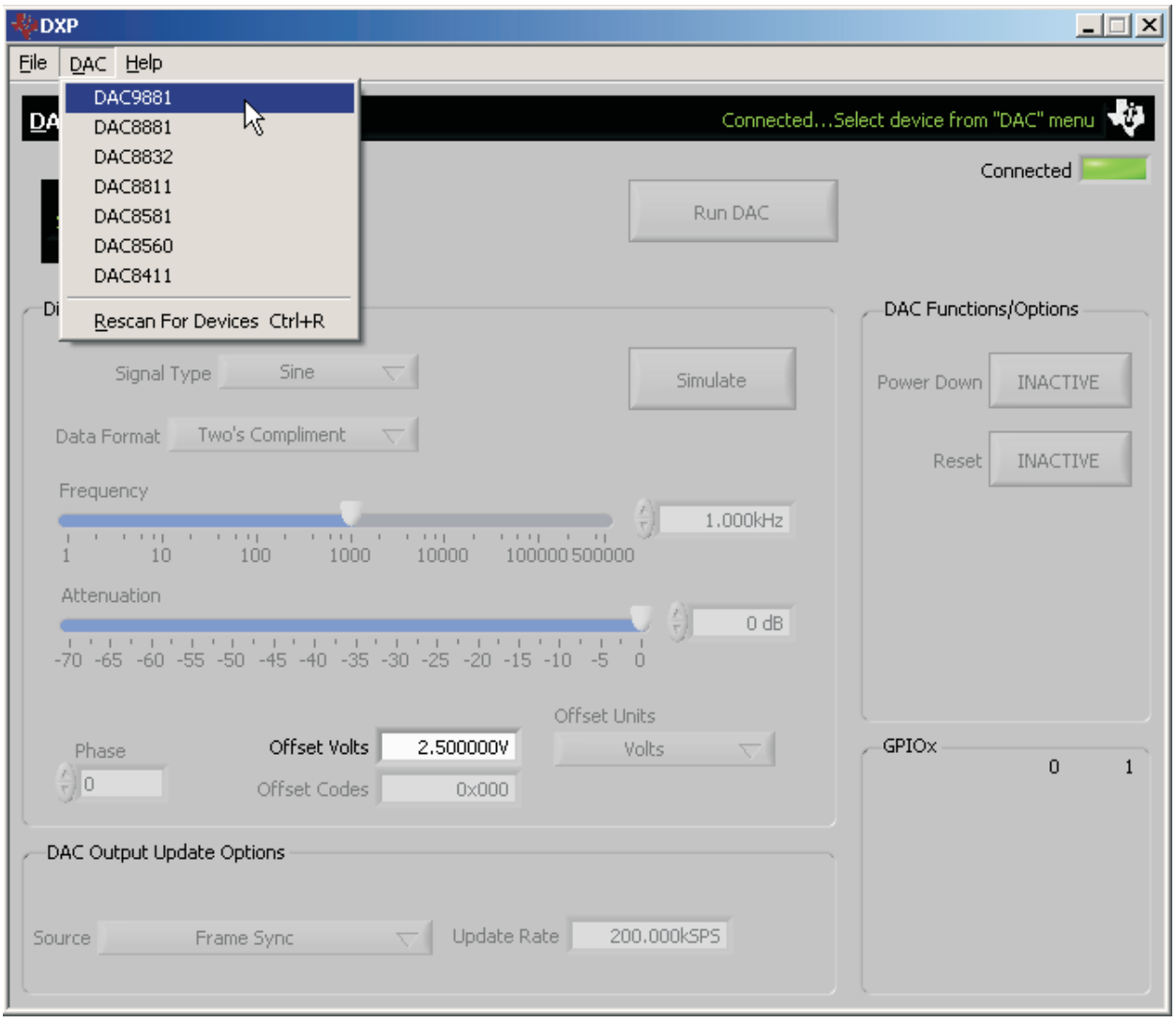


Figure 11. Loading the DAC9881EVM INI File

The DXP software defaults to output a 1-kHz sine wave from the DAC, other waveform options include Square, Saw tooth, Triangle, and DC output options as described in the DXP User's Guide. GPIO options are available on the DAC9881EVM which active either the RESET or power-down functions of the DAC9881. These are shown inFigure 12 on the right side of the screen labeled GPIO-controlled DAC Functions. Pressing the Reset button resets the DAC9881 outputs as described in the device data sheet. Pressing the Power-Down button places the DAC9881 in low-power mode.

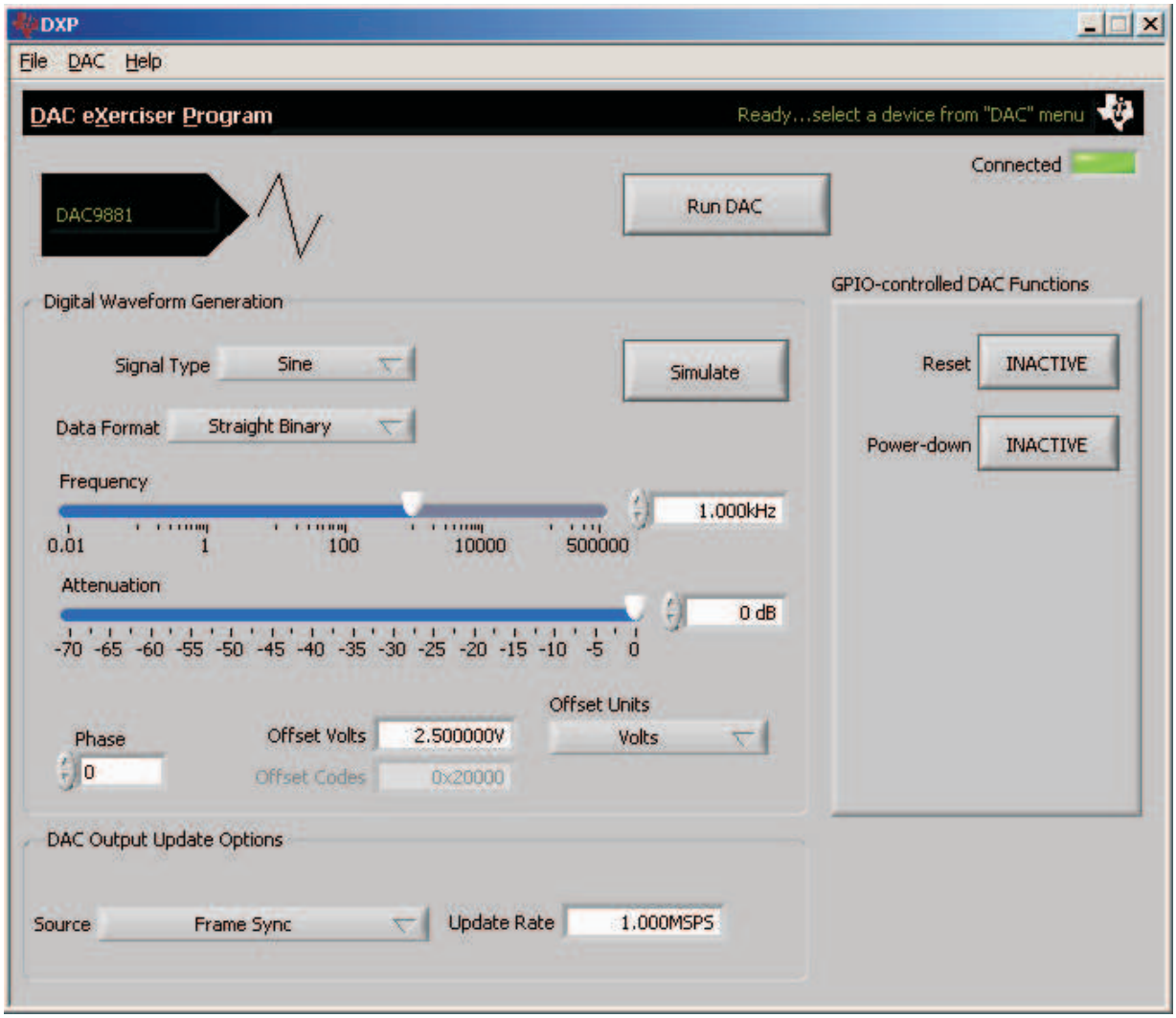


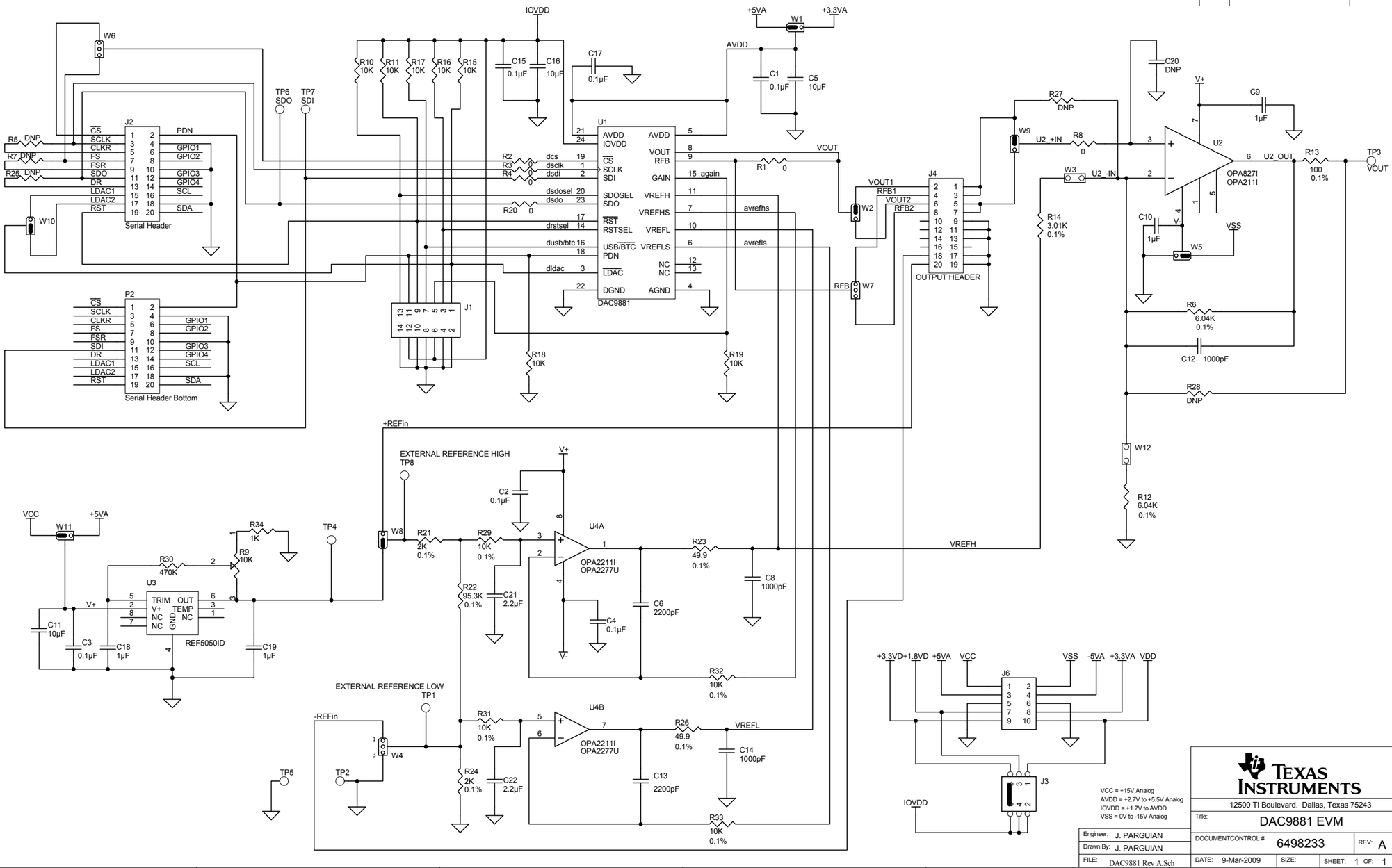
Figure 12. DAC9881 – Frequency/Amplitude and GPIO Control Options

7 Related Documentation From Texas Instruments

1. *DAC9881, 18-Bit, Single-Channel, Low-Noise, Voltage-Output Digital-to-Analog Converter* data sheet (SBAS438)
2. *REF02, +5V Precision Voltage Reference* data sheet (SBVS003)
3. *REF5050, Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet (SBOS410)
4. *OPA211, 1.1nV/ √Hz Noise, Low Power, Precision Operational Amplifier in Small DFN-8 Package* data sheet (SBOS377)
5. *OPA827, Low-Noise, High-Precision, JFET-Input Operational Amplifier* data sheet (SBOS376)
6. *OPA277, OPA2277, OPA4277, High Precision Operational Amplifiers* data sheet (SBOS079)
7. *OPA227, High Precision, Low Noise Operational Amplifiers* data sheet (SBOS110)

If you have questions about this or other Texas Instruments Data Converter evaluation modules, send an e-mail to the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product with which you have questions or concerns.

Revision History		
REV	ECN Number	Approved
A	Release to production	JLP



TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title:	DAC9881 EVM
Engineer:	J. PARGUIAN
Drawn By:	J. PARGUIAN
FILE:	DAC9881 Rev A.Sch
DOCUMENTCONTROL #	6498233
REV:	A
DATE:	9-Mar-2009
SIZE:	
SHEET:	1 OF: 1

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -15 V to +15 V and the output voltage range of -15 V to +15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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