

TPS65162EVM-278

The TPS65162EVM-278 evaluation module operates from a 8-V to 14-V input rail and provides the three bias-supply voltages (Vs, VGH, and VGL) and a logic-supply voltage (3.3 V) that are required for television and monitor TFT-LCD panels. This device also provides two operational amplifiers to generate the VCOM supply rail. The TPS65162EVM-278 has one boost converter with an integrated low-side FET, one negative charge-pump controller requiring external Schottky diodes, and one fully integrated positive charge pump for TFT-LCD bias supply. External passive components to support the boost converter include rectifying diode, inductors, and capacitors. External components for the charge pumps include capacitors and switching diodes. One nonsynchronous buck converter with external Schottky diode make up the logic supply.

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1 Introduction

This section contains background information for the TPS65162EVM-278 evaluation module (EVM).

1.1 Specification

[Table 1](#) provides a summary of the TPS65162EVM-278 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Voltage Range (V)			Current Range (mA)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
VIN	8	12	14		1500	
Vs	14.7	15	15.3		500	
VGL	-5.15	-5	-4.85		33	
VGH	25.0	27 ⁽¹⁾	29.0		50	
Vlogic		3.3			1500	

⁽¹⁾ Assumes that SUP = V_S.

1.2 Modifications

The primary goal of this EVM is to facilitate user evaluation of the TPS65162 in a power-supply application for a typical large TFT display. To facilitate user customization of the EVM, the board was designed with devices having 0805 or larger footprints. A production-optimized implementation would likely occupy less total board space.

1.2.1 Customizing Power Supply

The user can change each rail's regulated output voltage by changing the appropriate feedback resistors per the device data sheet ([SLVS771](#)). The user is responsible for not exceeding each output's maximum voltage specifications. In addition, alternate capacitors, inductors, and/or diodes can be used. When using alternate capacitors, ensure that at least the minimum recommended capacitance per the data sheet is used, and that the capacitor voltage rating is appropriate for the application. The switching converters are designed to be used with ceramic output capacitors. Using nonceramic output capacitors with significantly large equivalent series resistances (ESR) can result in larger output ripple or unstable operation of the inductive switching converters. Each charge pump's flying and output capacitors must be ceramic capacitors. When selecting an alternate inductor, use the data-sheet design equations to ensure that an appropriate inductance value is selected, and that the inductor current rating is appropriate for the desired output current. Using an inductor with larger dc resistance results in lower efficiency. When using alternate diodes, ensure that the diode is rated for both the expected peak current and expected power per the data-sheet design equations.

Enable 1 (J6) turns on the Vlogic converter. When the power-good threshold of this converter is reached, DLY1, set by C14, controls the delay time to turn off the negative charge-pump VGL. C14 can be changed to adjust this delay. Enable 2 (J7) turns on the positive charge-pump VGH. DLY2, set by C24, controls the delay time to turn on the positive charge pump from the Vlogic-good threshold or EN2 high. C24 can be changed to adjust the delay.

1.2.2 Input to Output Isolation

The nonsynchronous boost converter has a path from input to output, VIN to Vs, through the external switching diode D3. Transistor Q2 acts as an isolation switch for this path once the device is turned off.

2 Setup and Test Results

This section explains the input, output, and jumper connections of the TPS65162EVM-278. It also describes how to set up test equipment for evaluating the EVM and provides test results.

2.1 Connections and Jumpers

The DEFAULT jumper settings are required for the EVM to operate within the specifications of [Table 1](#).

Table 2. Default Jumper Settings

Jumper	Default Setting
J6 – Enable 1	(OFF) GND
J7 – Enable 2	(OFF) GND
J8 – Freq Control	(750 khz) Vin
J9 – Enable Gate Voltage Shaping	(ON) Vin
J10 – Control Gate Voltage Shaping	(ON) Vin

J1-VIN/GND:	Input power supply and ground connection, Vin range 8 V to 14 V
J2-Vs/GND:	Output connection for the main boost converter and ground return connection
J3-VLOGIC/GND:	Output voltage for 3.3-V buck converter and ground return connection
J4-VGH/GND:	Output connection for the internal high-voltage switch and ground return connection
J5-VGL/GND:	Output voltage for negative charge pump and ground return connection
J6–Enable 1:	Enable for VLOGIC converter, GND = OFF, VIN = ON
J7–Enable 2:	Enable for positive charge pump, GND = OFF, VIN=ON
J8–Freq Control:	Frequency Selection, GND = 750 kHz, Vin = 500 kHz
J9–Enable Gate Voltage Shaping:	Gate Voltage Shaping, GND = OFF, VIN = ON
J10–Control Gate Voltage Shaping:	Control Voltage Shaping, GND = OFF, VIN = ON
J11-OPAMP 1:	Opamp 1 input, output, gnd, and VS connection
J12-OPAMP 2:	Opamp 2 input, output, gnd, and VS connection
J13-NEG1:	Opamp 1 connection negative input and output
J14-NEG2:	Opamp 2 connection negative input and output
J15-GND/REFERENCE :	VGL reference voltage and ground return
J16-VS test point:	Test point for VS
J17-VGH test point:	Test point for VGH
J18-VGL test point:	Test point for VGL
J19-VLOGIC test point:	Test point for VLOGIC

2.2 Recommended Test Setup

Before turning on the power supply, ensure that jumpers J6--J10 are in their default positions.

Connect a power supply rated at 3 A or more to provide 8 V to 14 V to J1. Do not exceed 14 V on J1. In order to avoid voltage drop through the input power supply line, connect heavy-gauge, twisted-pair wire to J1. The output voltages can be monitored by voltmeters and/or an oscilloscope with standard high-impedance voltage probes.

The output voltages reach their respective regulation voltages per [Table 1](#) after the appropriate soft-start times and relative delays. Resistive or electronic loads can be attached to output J2 for Vs and J3 for Vlogic. Only resistive loads can be attached to outputs J4 for VGH and J5 for VGL. Exceeding an output load specified in [Table 1](#) results in the output voltage falling out of regulation.

Use EN1 (J6) to turn on the buck converter (VLOGIC) and negative charge pump (VGL). EN2 is used to turn on the boost converter (Vs) and positive charge pump (VGH). With EN2 (J7) set to the on position, EN1 controls on/off for all voltages.

2.3 Test Results

Test results using the TPS65162EVM-278 are shown in [Figure 1](#).

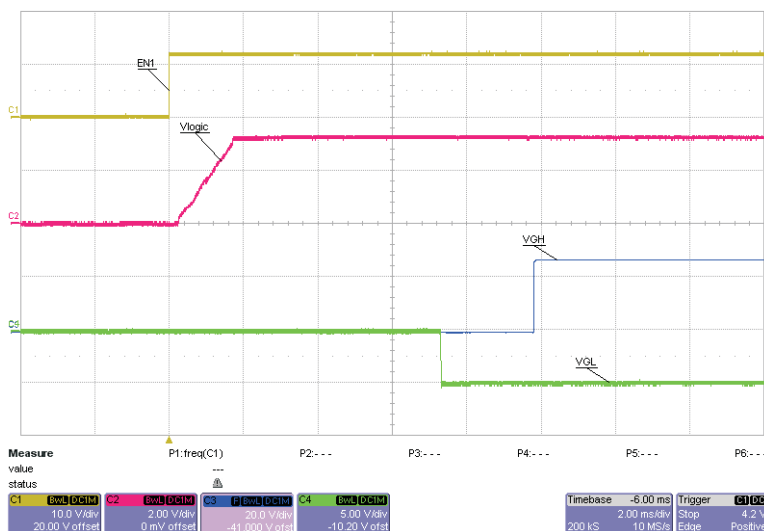


Figure 1. Start-up Waveform

3 Board Layout

This section provides board layout recommendations as well as illustrations of the EVM board layers.

3.1 Board Layout Recommendations

For information regarding PC board layout, see the TPS65162 data sheet ([SLVS760](#)).

3.2 Board Layers

The following illustrations show the top assembly and top and bottom layers of the TPS65162EVM-278.

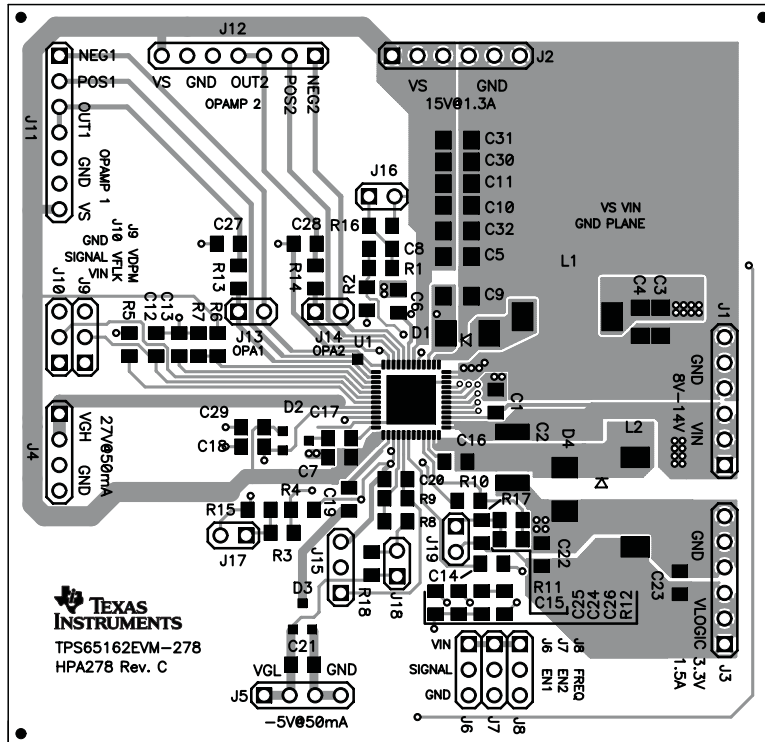


Figure 2. Top Assembly

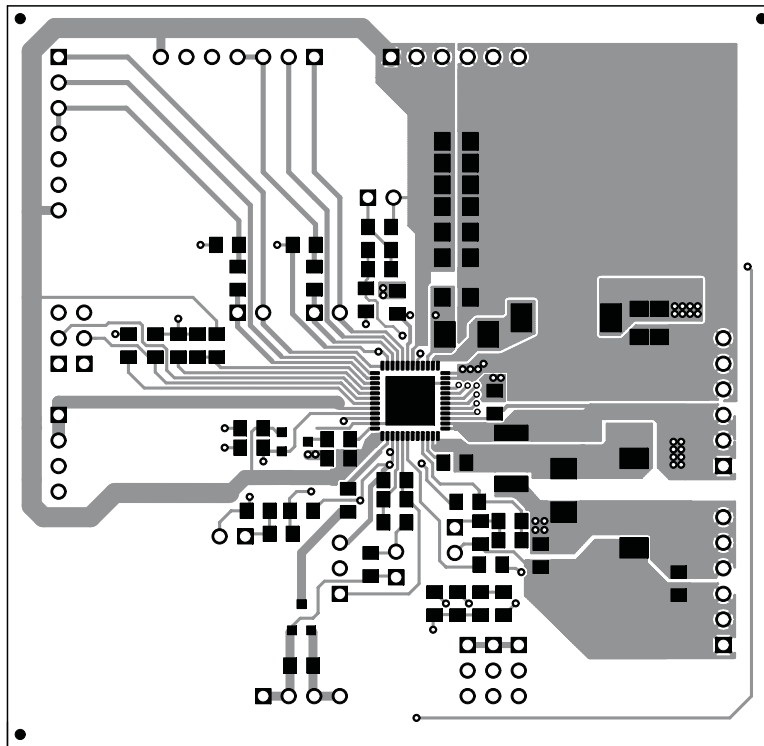


Figure 3. Top Layer

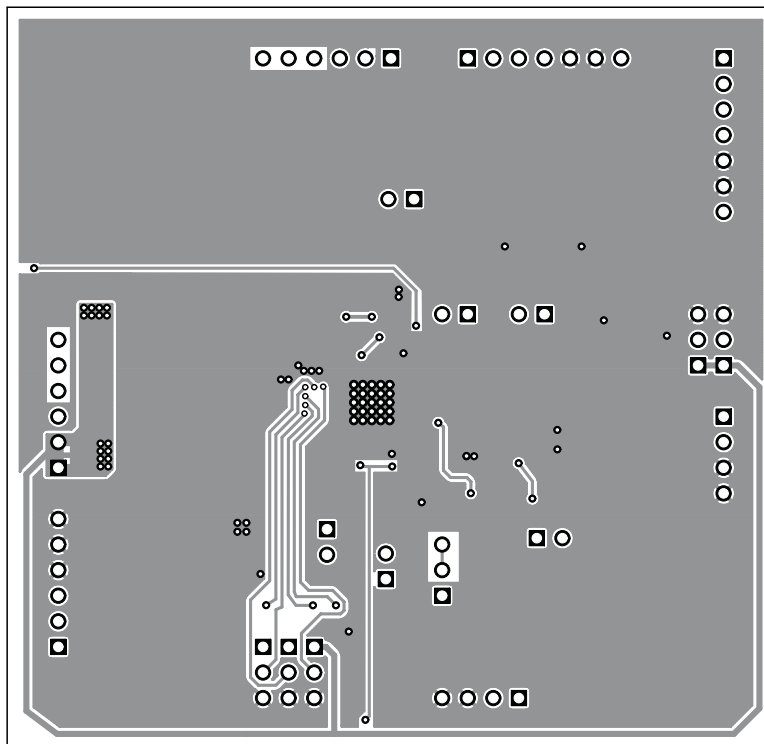


Figure 4. Bottom Layer

4 Schematic and Bill of Materials

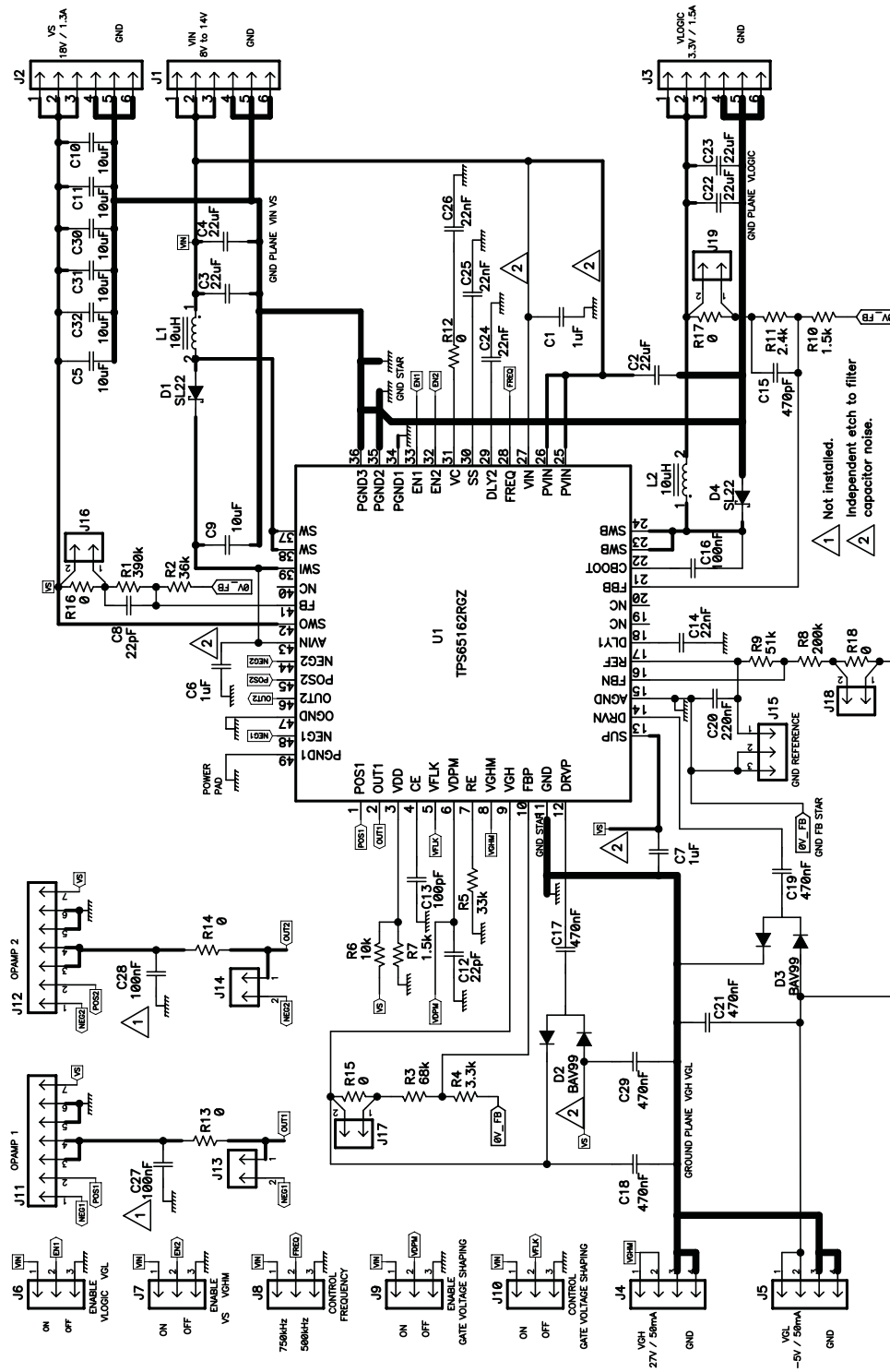


Table 3. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
3	C1, C6, C7	1 μ F	Capacitor, Ceramic, 25V, X5R, 10%	0805	GRM216R61E105KA12D	Murata	10560
1	C2	22 μ F	Capacitor, Ceramic, 25V, X5S, 20%	1812	GRM43EB11C226ME01B	Murata	43,360
2	C3, C4	22 μ F	Capacitor, Ceramic, 16V, X5R, 20%	1206	GRM31CR61C226KE15L	Murata	15390
7	C5, C9–C11, C30–C32	10 μ F	Capacitor, Ceramic, 25V, X5R, 10%	1206	GRM31CR71E106KA12L	Murata	15390
2	C8, C12	22pF	Capacitor, Ceramic, 50V, C0G, 5%	0805	GRM2165C1H220JZ01D	Murata	10560
1	C13	100pF	Capacitor, Ceramic, 50V, COG, 5%	0805	GRM2165C1H101JA01D	Murata	10560
4	C14, C24–C26	22nF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM216R71H223KA01D	Murata	10560
1	C15	470pF	Capacitor, Ceramic, 50V, C0G, 5%	0805	GRM2165C1H471JA01D	Murata	10560
3	C16, C27, C28	100nF	Capacitor, Ceramic, 25V, X7R, 10%	0805	GRM21BR71E104KA01L	Murata	10560
3	C17, C18, C29	470nF	Capacitor, Ceramic, 50V, X5R, 10%	0805	GRM21BR71H474KA88L	Murata	10560
2	C19, C21	470nF	Capacitor, Ceramic, 25V, X5R, 10%	0805	GRM219R71E474KA88D	Murata	10560
1	C20	220nF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM21BR71H224KA01L	Murata	10560
2	C22, C23	22 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	GRM219R60J106KE19D	Murata	10560
2	D1	SL22	Diode, Schottky Rectifier, 2A, 20 V	DO-214AA	SL22	Vishay	32472
2	D2, D3	BAV99	Diode, Dual Ultra Fast, Series, 200-mA, 70-V	SOT23	BAV99	Fairchild	14105
	D4	SL22	Diode, Schottky Rectifier, 2A, 20 V	DO-214AA	SL22	Vishay	32472
3	J1–J3	PTC36SAAN	Header, 6-pin, 100mil spacing, (36-pin strip)	0.100 in \times 6	PTC36SAAN	Sullins	0.82 in
2	J4, J5	PTC36SAAN	Header, 4-pin, 100mil spacing, (36-pin strip)	0.100 in \times 4	PTC36SAAN	Sullins	
6	J6–J10, J15	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 in \times 3	PTC36SAAN	Sullins	0.043 in
2	J11, J12	PTC36SAAN	Header, 7-pin, 100mil spacing, (36-pin strip)	0.100 in \times 8	PTC36SAAN	Sullins	80000
6	J13, J14, J16–J19	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 in \times 2	PTC36SAAN	Sullins	
2	L1, L2	10 μ H	Inductor, SMT, 3.2A, 36milliohm	0.327 \times 0.327 in	CDRH8D43-100	Sumida	165,600
1	R1	390k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R2	36k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R3	68k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R4	3.3k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R5	33k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R6	10k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
2	R7, 10	1.5k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R8	200k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R9	51k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
1	R11	2.4k	Resistor, Chip, 1/10W, 1%	0805	Std	Std	15300
6	R12–R18	0	Resistor, Chip, 1/10W, 0 Ohm, 1%	0805	Std	Std	15300
1	U1	TPS65162RGZ	IC, Compact LCD Bias Supply	QFN-48	TPS65162RGZ	TI	116964
1	—		PCB, 3.0 In \times 2.9 In \times 0.062 In		HPA278	Any	
5	—		Shunt, 100 mil, Black	0.100	929950-00	3M	

- Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 25 V to 29 V (VGH).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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