

TPS5450EVM-254 5-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS5450 as well as support documentation for the TPS5450EVM-254 evaluation module (HPA254). Also included are the performance specifications, the schematic, and the bill of materials for the TPS5450EVM-254.

1.1 Background

The TPS5450 dc/dc converter is designed to provide up to a 5-A output from an input voltage source of 5.5 V to 36 V. Rated input voltage and output current range for the evaluation module is given in [Table 1](#). This evaluation module is designed to demonstrate a typical printed-circuit-board application using the TPS5450 regulator and does not reflect the full range of possible input and output voltages that may be used when designing with this part. The switching frequency is internally set at a nominal 500 kHz. The

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high-side MOSFET is incorporated inside the TPS5450 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS5450 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided internal to the integrated circuit (IC), whereas an external divider allows for an adjustable output voltage. Additionally, the TPS5450 provides an enable input. The absolute maximum input voltage for the TPS5450 is 40 V.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS5450EVM-254	V _{IN} = 10 V to 31 V	0 A to 5 A

1.2 Performance Specification Summary

A summary of the TPS5450EVM-254 performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 5 V, unless otherwise specified. The TPS5450EVM-254 is designed and tested for V_{IN} = 10 V to 31 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. Maximum operating input voltage for the TPS5450EVM-254 is 36 V.

Table 2. TPS5450EVM-254 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN} voltage range			10		31	V
Output voltage set point				5.0		V
Output current range			0		5	A
Line regulation		I _O = 2.5 A, V _{IN} = 10 V - 31 V		±0.04%		
Load regulation		V _{IN} = 15 V, I _O = 0 A to 5 A		-0.02% +0.11%		
Load transient response	Voltage change	I _O = 1.25 A to 3.75 A		-60		mV
	Recovery time			160		ms
	Voltage change	I _O = 3.75 A to 1.25 A		60		mV
	Recovery time			160		ms
Loop bandwidth		V _{IN} = 25 V, I _O = 2.5 A		17.0		kHz
Phase margin		V _{IN} = 25 V, I _O = 2.5 A		58		°
Input ripple voltage		I _O = 5 A		400		mV _{PP}
Output ripple voltage		I _O = 5 A		30		mV _{PP}
Output rise time				7		ms
Operating frequency				500		kHz
Max efficiency		V _{IN} = 10 V, V _O = 5 V, I _O = 1 A		93.4%		

1.3 Modifications

The TPS5450EVM-254 is designed to demonstrate the small size that can be attained when designing with the TPS5450. A few changes can be made to this module.

1.3.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage above 1.25 V. The value of R2 for a specific output voltage can be calculated using [Equation 1](#).

$$R2 = 10 \text{ k}\Omega \times \frac{1.221 \text{ V}}{V_O - 1.221 \text{ V}} \quad (1)$$

Table 3 lists the R2 values for some common output voltages. Note that VIN must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R ₂ Value (kΩ)
1.8	21.5
2.5	9.53
3.3	5.90
5	3.16

1.3.2 Input Voltage Range

The EVM is designed to operate from a nominal 10 to 31 V input voltage range. The TPS5450 is specified to operate over an input voltage range of 5.5 V to 36 V.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5450EVM-254 evaluation module. The section also includes test results typical for the TPS5450EVM-254 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input / Output Connections

The TPS5450EVM-254 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 5 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J3 through a pair of 20 AWG wires. The maximum load current capability should be 5 A. Wire lengths should be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN, 12 V nominal, 10 V to 31 V
J2	OUT, 5 V at 5 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	VIN test point at VIN connector
TP2	GND test point at VIN
TP3	Output voltage test point at OUT connector
TP4	GND test point at OUT connector
TP5	Test point between voltage divider network and R3. Used for loop response measurements.
TP6	PH test point

2.2 Efficiency

The TPS5450EVM-254 efficiency peaks at load current of about 1 to 2 A, depending on the input voltage, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS5450EVM-254 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

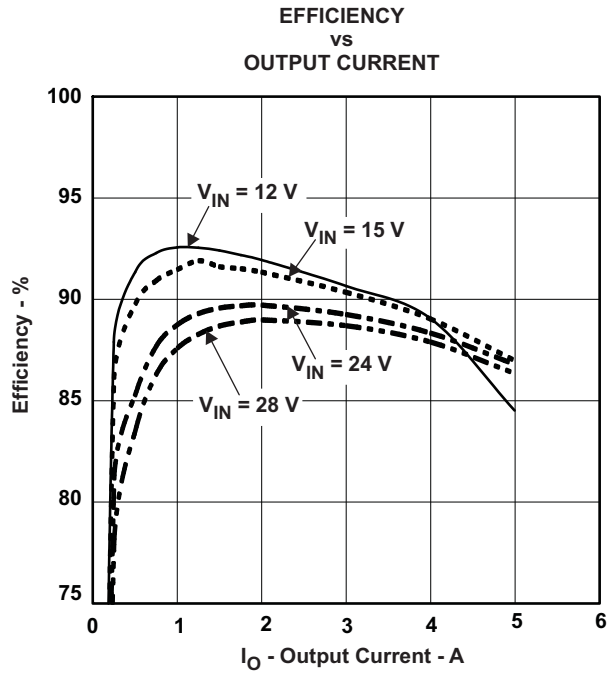


Figure 1. Measured Efficiency, TPS5450

2.3 Output Voltage Regulation

The output voltage load regulation of the TPS5450EVM-254 is shown in Figure 2 for an input voltage of 15 V; the output voltage line regulation is shown in Figure 3. Measurements are given for an ambient temperature of 25°C.

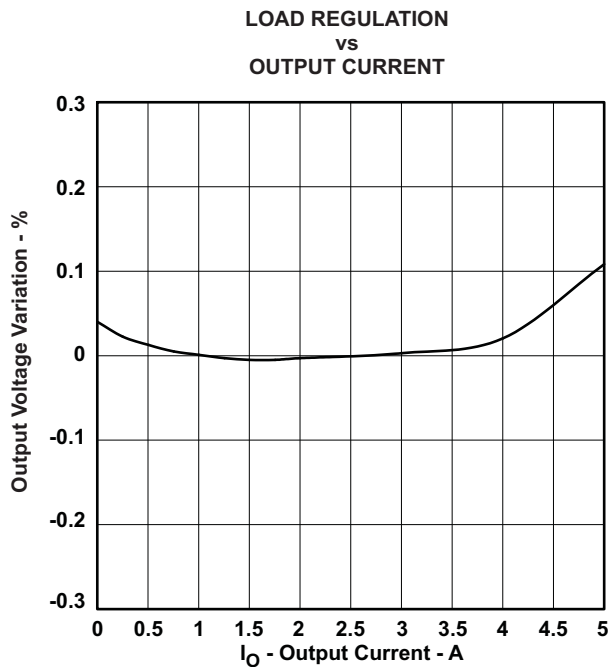


Figure 2. Load Regulation

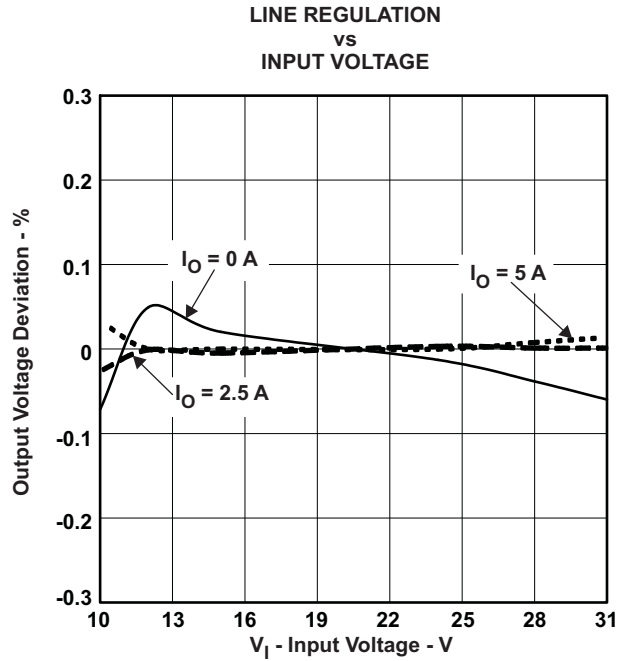


Figure 3. Line Regulation

2.4 Load Transients

The TPS5450EVM-254 response to load transients is shown in Figure 4. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

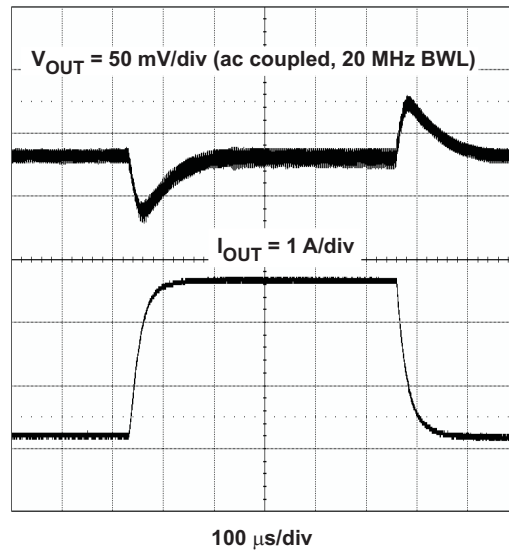


Figure 4. Load Transient Response, TPS5450

2.5 Loop Characteristics

The TPS5450EVM-254 loop-response characteristics are shown in Figure 5. The gain and phase plot is shown for a VIN voltage of 25 V.

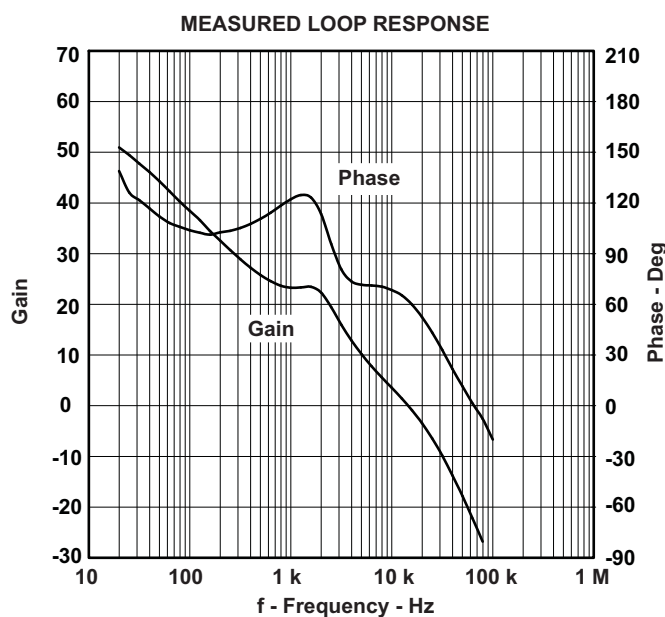


Figure 5. Measured Loop Response, TPS5450, VIN = 25 V

2.6 Output Voltage Ripple

The TPS5450EVM-254 output voltage ripple is shown in Figure 6. The input voltage is VIN = 25 V for the TPS5450. Output current is the rated full load of 5 A. Voltage is measured directly across output capacitors.

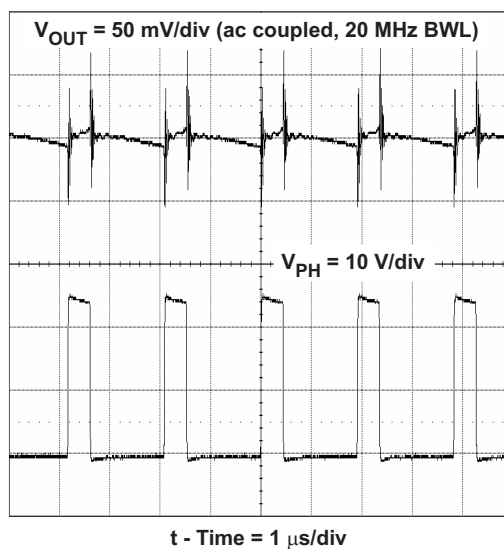


Figure 6. Measured Output Voltage Ripple, TPS5450

2.7 Input Voltage Ripple

The TPS5450EVM-254 output voltage ripple is shown in [Figure 7](#). The input voltage is $V_{IN} = 25\text{ V}$ for the TPS5450. Output current for each device is at full rated load of 5 A.

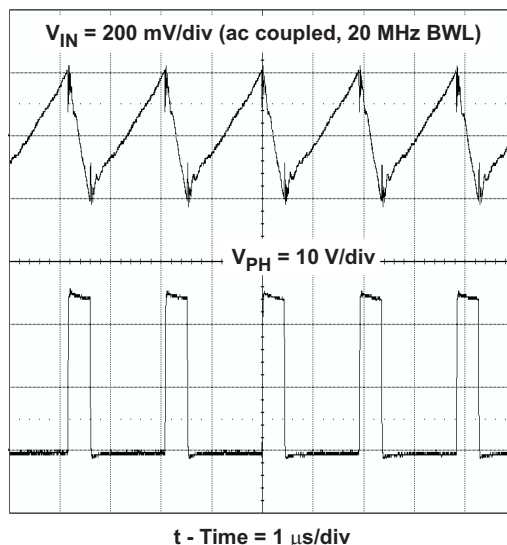


Figure 7. Input Voltage Ripple, TPS5450

2.8 Enable Control

The output may be inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released and the slow-start voltage begins to ramp up at the internally set rate. When the EN voltage reaches the enable-threshold voltage (1.3 V max), the start-up sequence begins.

3 Board Layout

This section provides a description of the TPS5450EVM-254 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS5450EVM-254 is shown in [Figure 8](#) through [Figure 12](#). The topside layer of the TPS5450EVM-254 is laid out in a manner typical of a user application. The all four layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN} connection to the IC, V_{OUT} , and V_{PHASE} . Also on the top layer are connections for the remaining pins of the TPS5450 and a large area filled with ground. The internal layer 2 and bottom layers contain dedicated ground planes. The internal layer 3 is mostly ground and also contains the V_{IN} connection from the edge connector J1, the EN trace to JP1, and the voltage sense trace. The bottom and internal ground traces are primarily used for thermal dissipation are connected to the top layer ground with four vias directly under the TPS5450 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C1, C4 and C5) and bootstrap capacitor (C2) are all located as close to the IC as possible. In addition, the voltage set point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the V_{OUT} connection of the output connector J2.

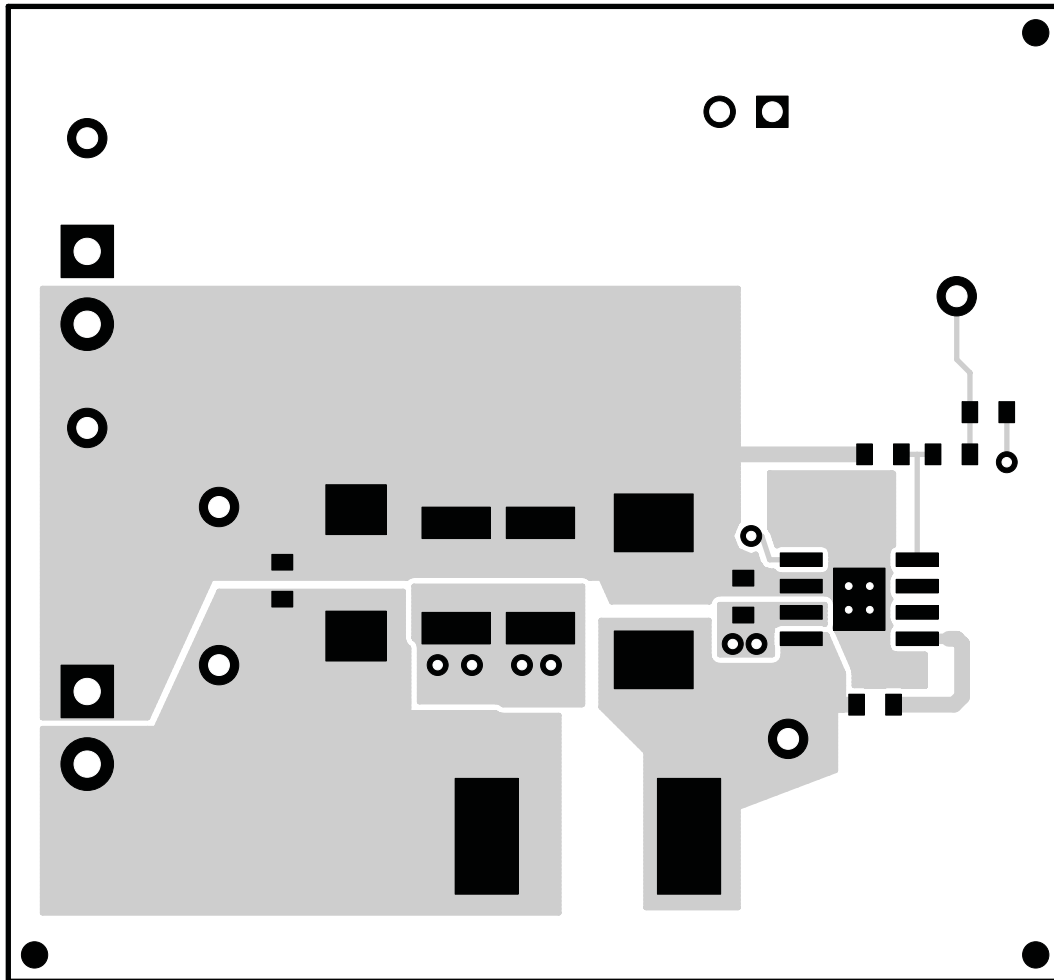


Figure 8. Top-Side Layout

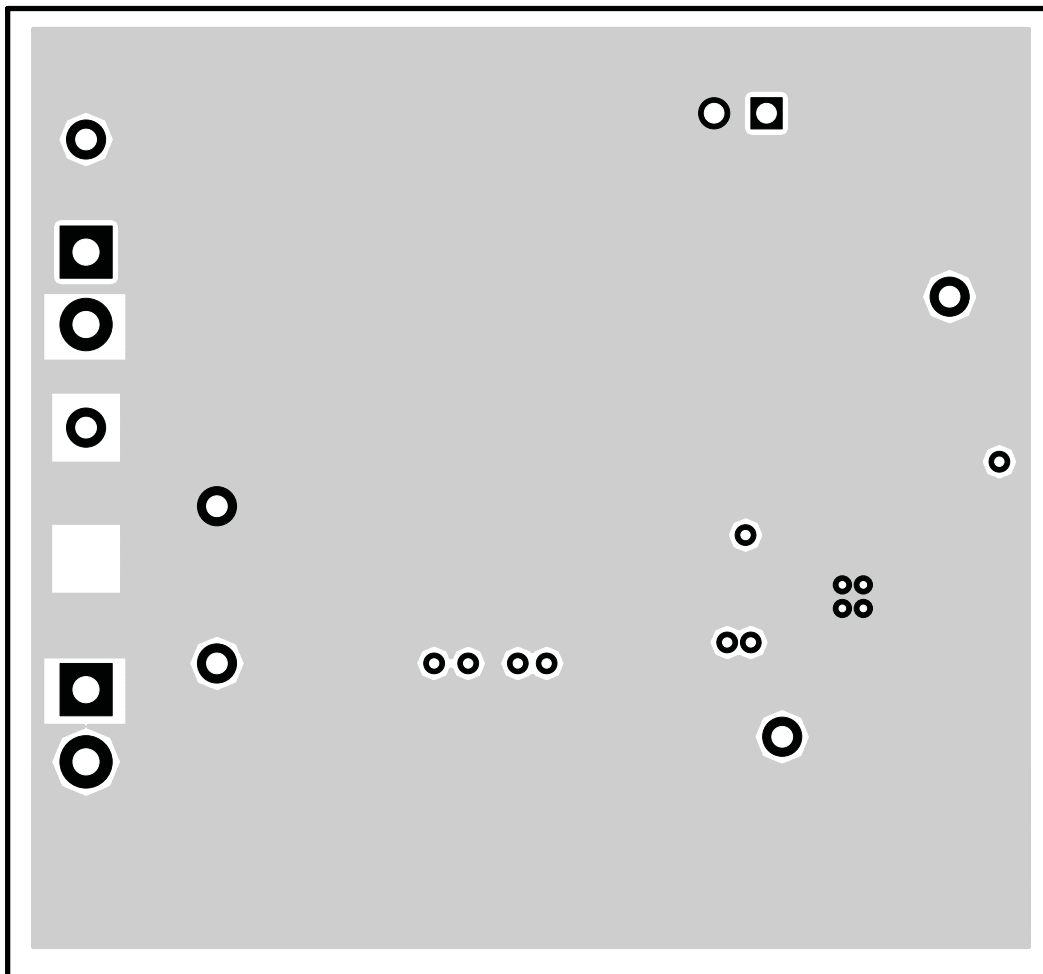


Figure 9. Internal Layer 2

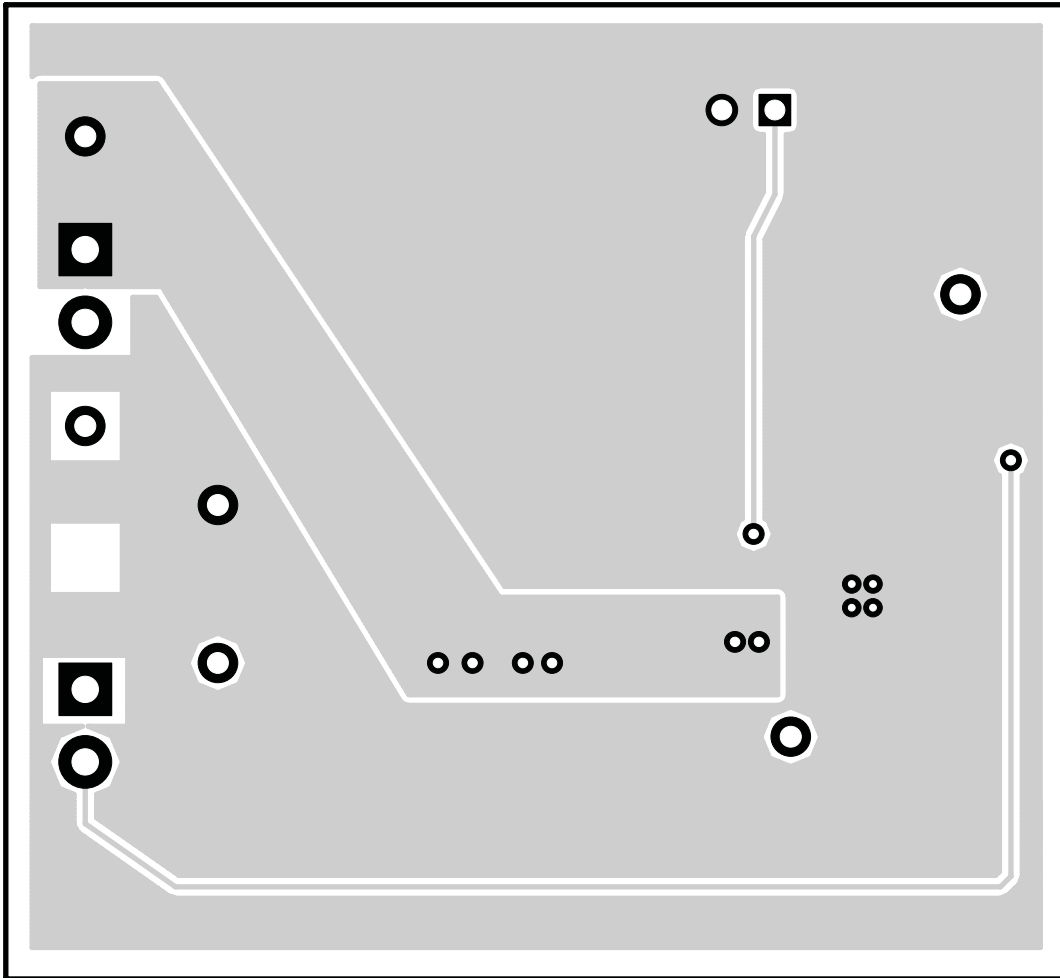


Figure 10. Internal Layer 3

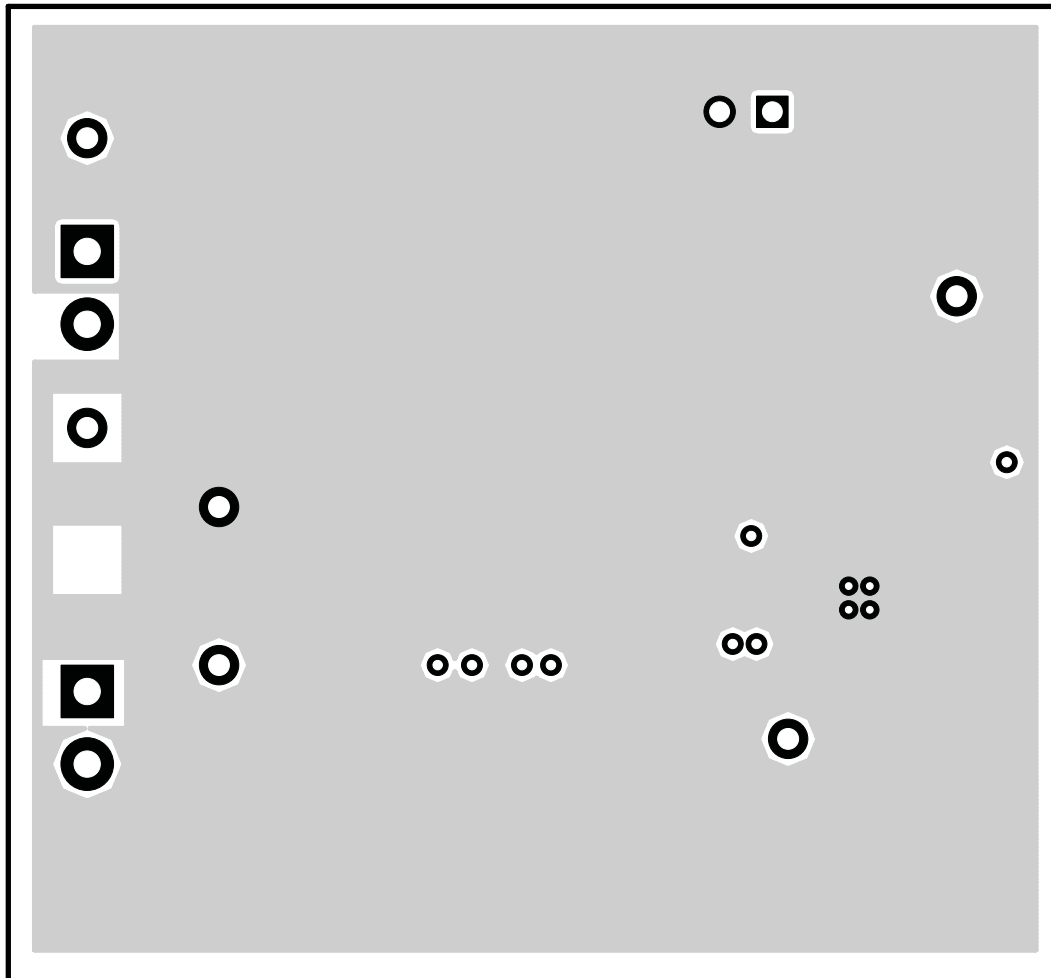


Figure 11. Bottom-Side Layout (Looking From Top Side)

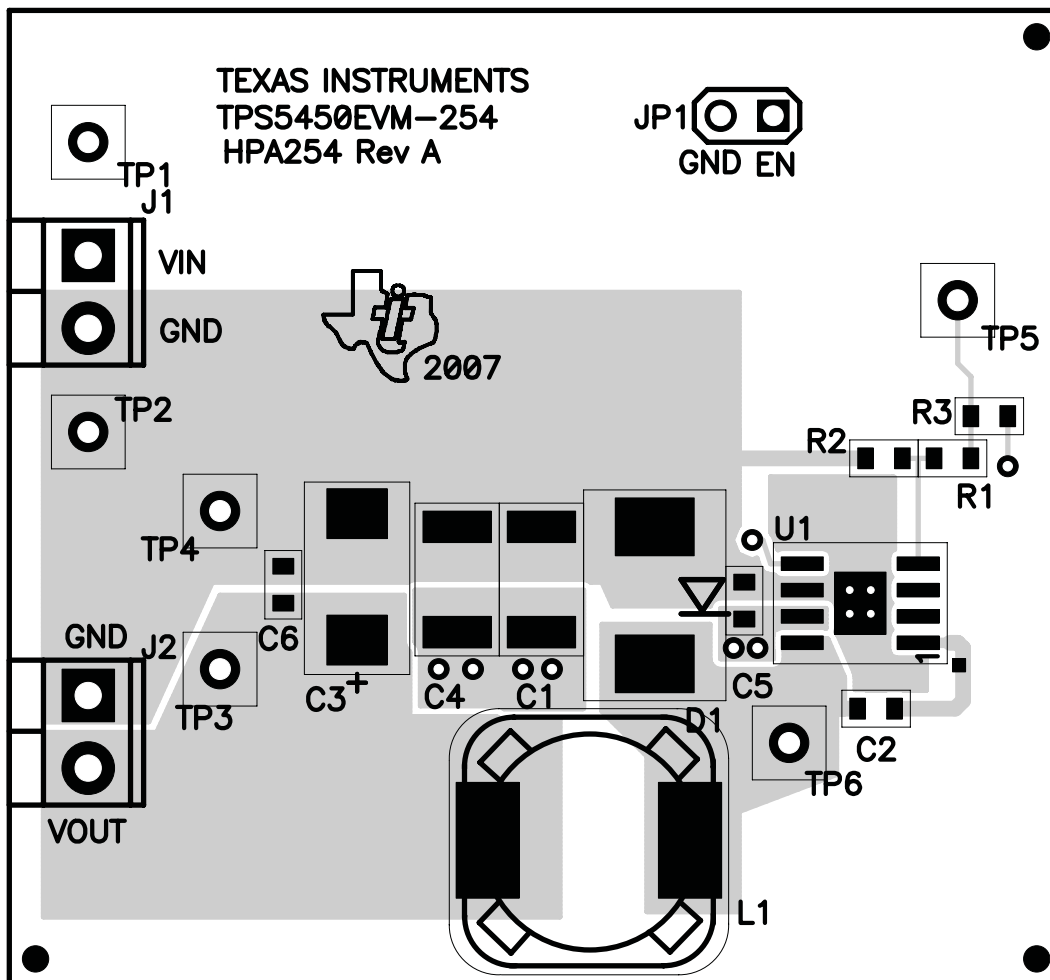


Figure 12. Top-Side Assembly

4 Schematic and Bill of Materials

The TPS5450EVM-254 schematic and bill of materials are presented in this section.

4.1 Schematic

The schematic for the TPS5450EVM-254 is shown in [Figure 13](#).

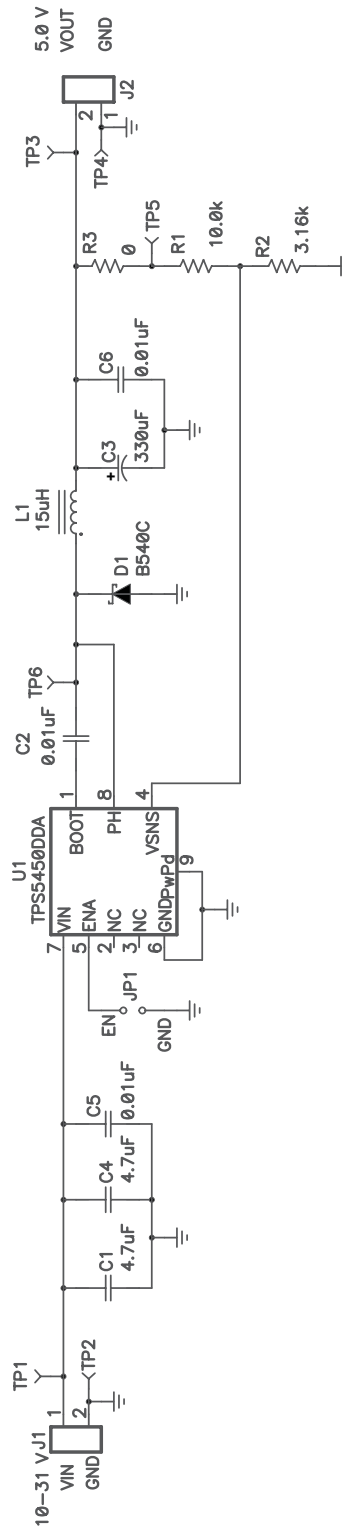


Figure 13. TPS5450EVM-254 Schematic

4.2 Bill of Materials

The bill of materials for the TPS5450EVM-254 is given by [Table 5](#).

Table 5. TPS5450EVM-254 Bill of Materials

Count	REF DES	Value	Description	Size	Part Number	MFR
2	C1, C4	4 μ F	Capacitor, Ceramic, 50V, X5R,20%	1812	C4532X5R1H475MT	TDK
3	C2, C5, C6	0.01 μ F	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H103K	TDK
1	C3	330 μ F	Capacitor, POSCAP, 10V, 35milliohm, 20%	7343(D)	10TPB330M	Sanyo
1	D1		Diode, Schottky, 5A, 40V	SMC	B540C-13-F	Diodes Inc
2	J1, J2		Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25	ED1514	OST
1	JP1		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	L1	15 μ H	Inductor, SMT, 5.65A, 26.4milliohm	0.405 sq inch	CDRH127/LD-150	Sumida
1	R1	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	3.24 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
4	TP1, TP3, TP5, TP6		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
2	TP2, TP4		Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100	5001	Keystone
1	U1		IC, Switching Step-Down Regulator, 5.5V-36V, 5A	SO8[DDA]	TPS5450DDA	TI
1	–		PCB, 2 In x 1.85 In x 0.062 In		HPA254	Any
1	–		Shunt, 100mil, Black	0.100	3M	929950-00

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10 V to 31 V and the output voltage range of 1.8 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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