
Table of Contents

| | |
|---|---|
| General Description..... | 2 |
| Installation | 2 |
| Typical Application Schematic..... | 3 |
| Efficiency and Output Ripple/Noise Measurement..... | 4 |
| Schematic | 5 |
| Bill of Materials | 6 |
| Printed Circuit Board Layer | 7 |

List of Figures

| | |
|--|---|
| Evaluation Board of POL Module..... | 2 |
| Quick Start..... | 3 |
| Quick Start Schematic..... | 3 |
| Wide Input Range Schematic..... | 3 |
| Efficiency Measurement Schematic | 4 |
| Equipment Setup for Efficiency Measurement | 4 |
| Output Ripple/Noise Measurement Method | 4 |
| Schematic | 5 |
| Top-Over Layer (Component Location)..... | 7 |
| Top Layer (Component Side) | 7 |
| Middle-1 Layer..... | 8 |
| Middle-2 Layer..... | 8 |
| Bottom Layer (Component Side)..... | 9 |
| Bottom-Over Layer (Component Location) | 9 |

List of Tables

| | |
|--|---|
| Test Equipment List..... | 2 |
| Recommended Operating Specifications | 2 |
| Typical Output Voltage Setting for each Resistance | 2 |
| Bill of Materials | 6 |

General Description

This app note covers the ISL8201MEVAL1Z, ISL8204MEVAL1Z, ISL8206MEVAL1Z evaluation boards. Since the modules are a pin for pin drop in with all necessary unique circuitry integrated in the module, the only difference in the BOM is the ISL8201M, ISL8206M, or ISL8204M POL modules. We will refer to a generic eval board, ISL820xMEVAL1Z to cover all three power modules.

The ISL820xMEVAL1Z POL module evaluation board is shown in Figure 1. The user can use it to evaluate the performance of the Intersil ISL8201M, ISL8206M, or ISL8204M POL modules. This board consists of power and load connectors for source and load side, switches for PVCC bias selection and On/Off option, and other passive components.

The input voltage range is from 1V to 20V, and the output voltage range is from 0.6V to 5V 5V for the ISL8201M or 0.6V to 6V for the ISL8204M and ISL8206M. Additional PVCC bias source is not required when using an input voltage of 5V or 12V. It can connect to the input side directly. However, in wider input ranges, which are above 14V or below 5V, the PVCC bias needs to add an external source, which provides operation bias of the module. The output voltage is initially set at 1.5V for typical evaluation. The user can easily set the output voltage by changing the value of R₁ (refer to Figure 8).

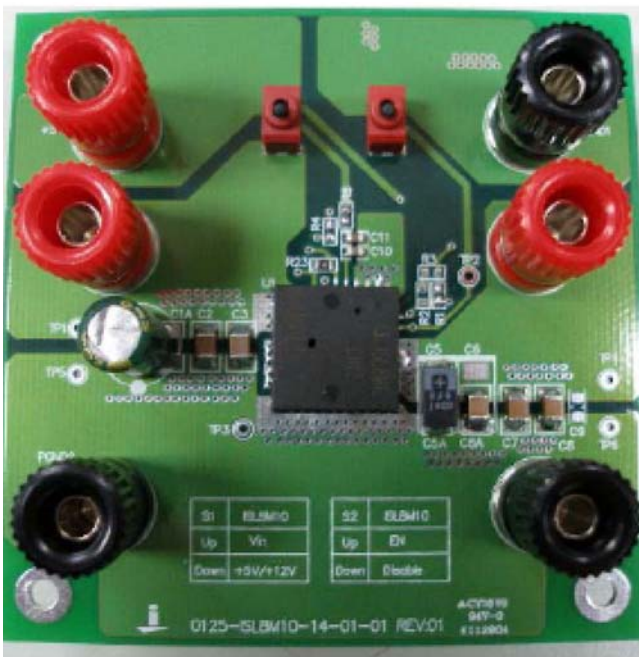


FIGURE 1. EVALUATION BOARD OF POL MODULE

Installation

TABLE 1. TEST EQUIPMENT LIST

| EQUIPMENT | PART NUMBER |
|--|--------------------------------------|
| An adjustable DC Power Supply 30V, 15A, with current limit | GW GPC-3060D |
| An electronic load, capable of sinking 20A | Chroma 63030/63010 |
| Four channel oscilloscope and probes | Tektronix TDS3014 Tektronix P3010 |
| High Precision Digital Voltage Meter | ESCORT 3136A |
| High Precision Digital Current Meter | ESCORT 3136A |

Recommended Operating Specification

The recommended operating specification for input/output and PVCC bias range is shown as Table 2.

TABLE 2. RECOMMENDED OPERATING SPECIFICATIONS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|------|------|------|
| Input Voltage Range (V _{IN}) | | 1 | - | 20 | V |
| Supply Voltage Range (PVCC) | Fixed +5V Supply | 4.5 | 5.0 | 5.5 | V |
| | Fixed +12V Supply | 9.6 | 12.0 | 14.4 | V |
| | Wide Range Supply | 6.5 | - | 14.4 | V |
| Output Voltage Range (V _{OUT}) | ISL8201M | 0.6 | - | 5 | V |
| | ISL8204M and ISL8206M | 0.6 | - | 6 | V |
| Current Setting for V _{OUT} | R1 = 6.49kΩ | - | 1.5 | - | V |
| Output Current (Load Current) | ISL8201M | - | - | 10 | A |
| | ISL8206M | - | - | 6 | A |
| | ISL8204M | - | - | 4 | A |
| Current Limit (PVCC = 12V) | ISL8201M R _{SEN-IN} = 3.57kΩ | - | 17 | - | A |
| | ISL8206M R _{SEN-IN} = 4.12kΩ | - | 8.8 | - | A |
| | ISL8204M R _{SEN-IN} = 2.87kΩ | - | 6.6 | - | A |

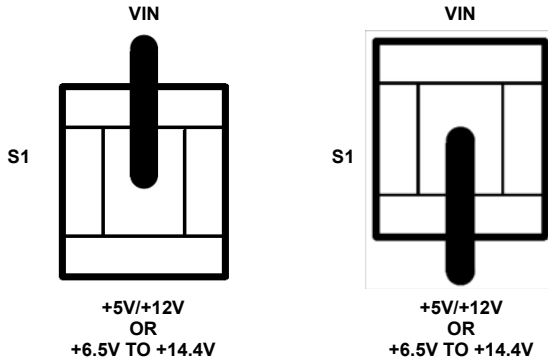
Table 3 lists the typical application's various output voltages and its corresponding resistance.

TABLE 3. TYPICAL OUTPUT VOLTAGE SETTING FOR EACH RESISTANCE

| V _{OUT} | 0.6V | 1.05V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V |
|------------------|------|-------|-------|-------|-------|-------|-------|-------|
| R ₁ | Open | 13k | 9.76k | 6.49k | 4.87k | 3.09k | 2.16k | 1.33k |

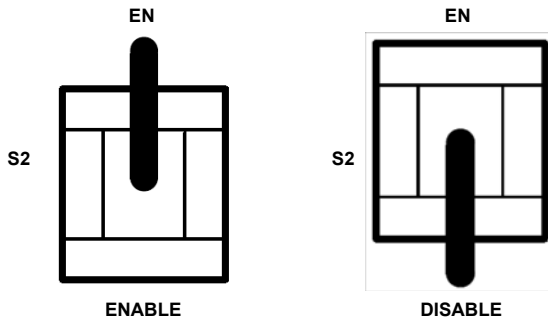
Selecting Switches

Switch S1 selects PVCC bias supply from V_{IN} or an additional supply source. When S1 is pushed up, the PVCC bias connects to the input power side. When S1 is pushed down, the PVCC bias connects to the additional power supply. For typical applications, the PVCC bias voltage is +5V ($\pm 10\%$) or +12V ($\pm 20\%$). It can also supply a wider range from +6.5V to +14.4V.



| SWITCH | UP | DOWN |
|--------|----------|-----------------------------|
| S1 | V_{IN} | +5V/+12V or +6.5V to +14.4V |

Switch S2 selects module Enable (On) or Disable (Off). When S2 is pushed up, the COMP/EN pin of the module is enabled and the module starts initialization and operation. When S2 is pushed down, the COMP/EN pin of the module connects to ground and the module will be shut down.



| SWITCH | UP | DOWN |
|--------|----|---------|
| S2 | EN | Disable |

Quick Start

The evaluation board can be evaluated simply, as shown in Figure 2. The power connection of the evaluation board supplies the input voltage from the DC Power Supply, and the load connection of the evaluation board delivers power to the Electronic Load. If the input voltage is +5V or +12V, the PVCC bias does not require additional supply and it can connect to the input side directly by pushing switch S1 to the up state.

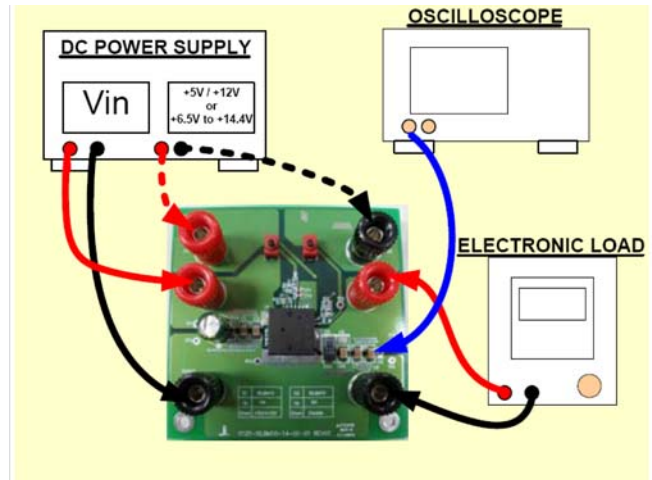


FIGURE 2. QUICK START FOR EVALUATION BOARD

Figure 3 shows the ISL820xMEVAL1Z application schematic for +5V or +12V input voltage. The PVCC pin can connect to the input supply directly.

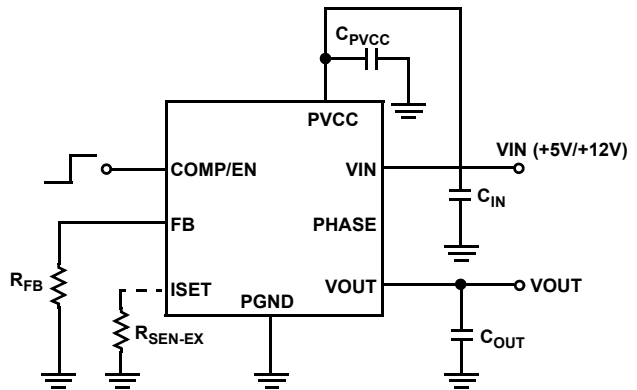


FIGURE 3. QUICK START SCHEMATIC

Typical Application Schematic

Typical Application with Separated Power Supply

Figure 4 shows the ISL820xMEVAL1Z application schematic for a wide input voltage from +1V to +20V. The PVCC supply can source +5V/+12V or +6.5V to +14.4V.

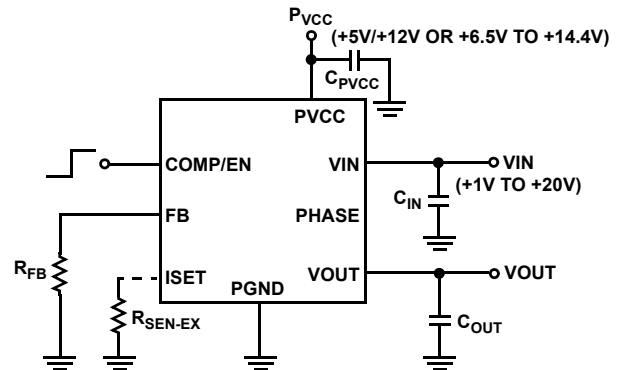


FIGURE 4. WIDE INPUT RANGE SCHEMATIC

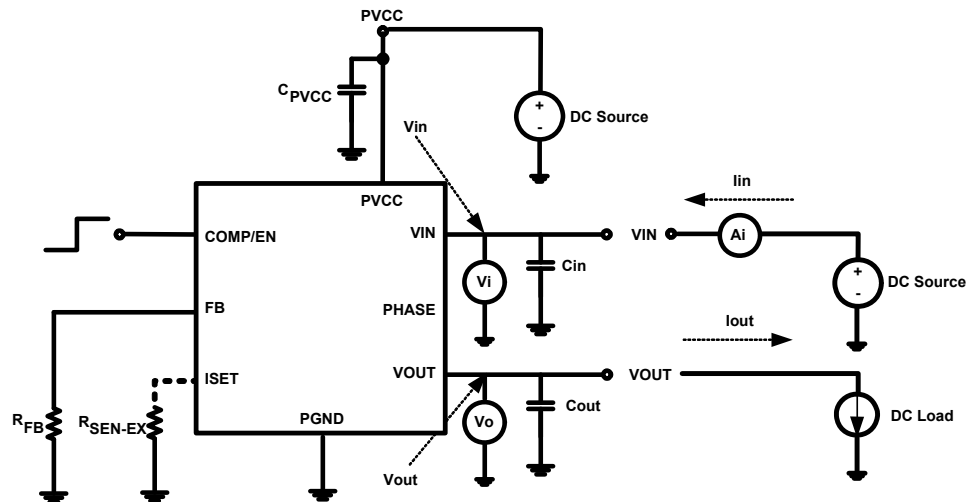


FIGURE 5. EFFICIENCY MEASUREMENT SCHEMATIC

Efficiency and Output Ripple/Noise Measurement

Figure 5 shows the efficiency measurement schematic for the ISL820xMEVAL1Z POL module. The voltage and current meter can be used to measure input/output voltage and current. In order to obtain an accurate measurement and prevent the voltage drop of PCB or wire trace, the voltage meter must be close to the input/output pin of the POL module.

The efficiency equation is shown in Equation 1:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{(V_{\text{OUT}} \cdot I_{\text{OUT}})}{(V_{\text{IN}} \cdot I_{\text{IN}})} \quad (\text{EQ. 1})$$

The equipment setup for the efficiency measurement on the evaluation board is shown in Figure 6. The measuring point for the input voltage meter is at the C₃ terminal, and the measuring point for the output voltage meter is at the C₈ terminal (refer to Figure 9).

Output Ripple/Noise Measurement Method

The total noise is equal to the sum of the ripple and noise components. Simple steps should be taken to assure that there is minimum pickup noise due to the high frequency events, which can be magnified by the large ground loop formed by the oscilloscope probe ground. This means that even a few inches of ground wire on the oscilloscope probe may result in hundreds of millivolts of noise spikes when improperly routed or terminated. This effect can be overcome by using the short loop measurement method to minimize the measurement loop area for reducing the pickup noise. The short loop measurement method is shown in Figure 7. For ISL820xMEVAL1Z evaluation board, the output ripple/noise measurement point is located at the C₈ terminal (refer to Figure 9).

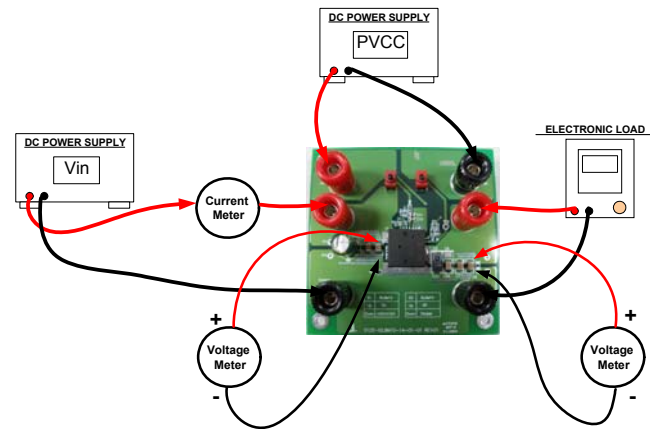


FIGURE 6. EQUIPMENT SETUP FOR EFFICIENCY MEASUREMENT

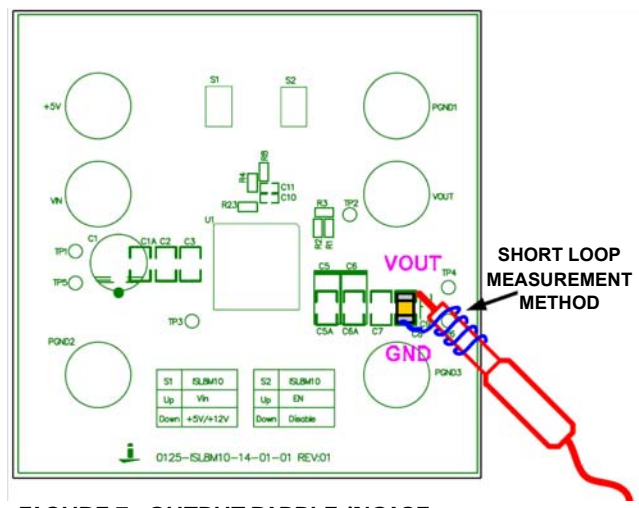


FIGURE 7. OUTPUT RIPPLE/NOISE MEASUREMENT METHOD

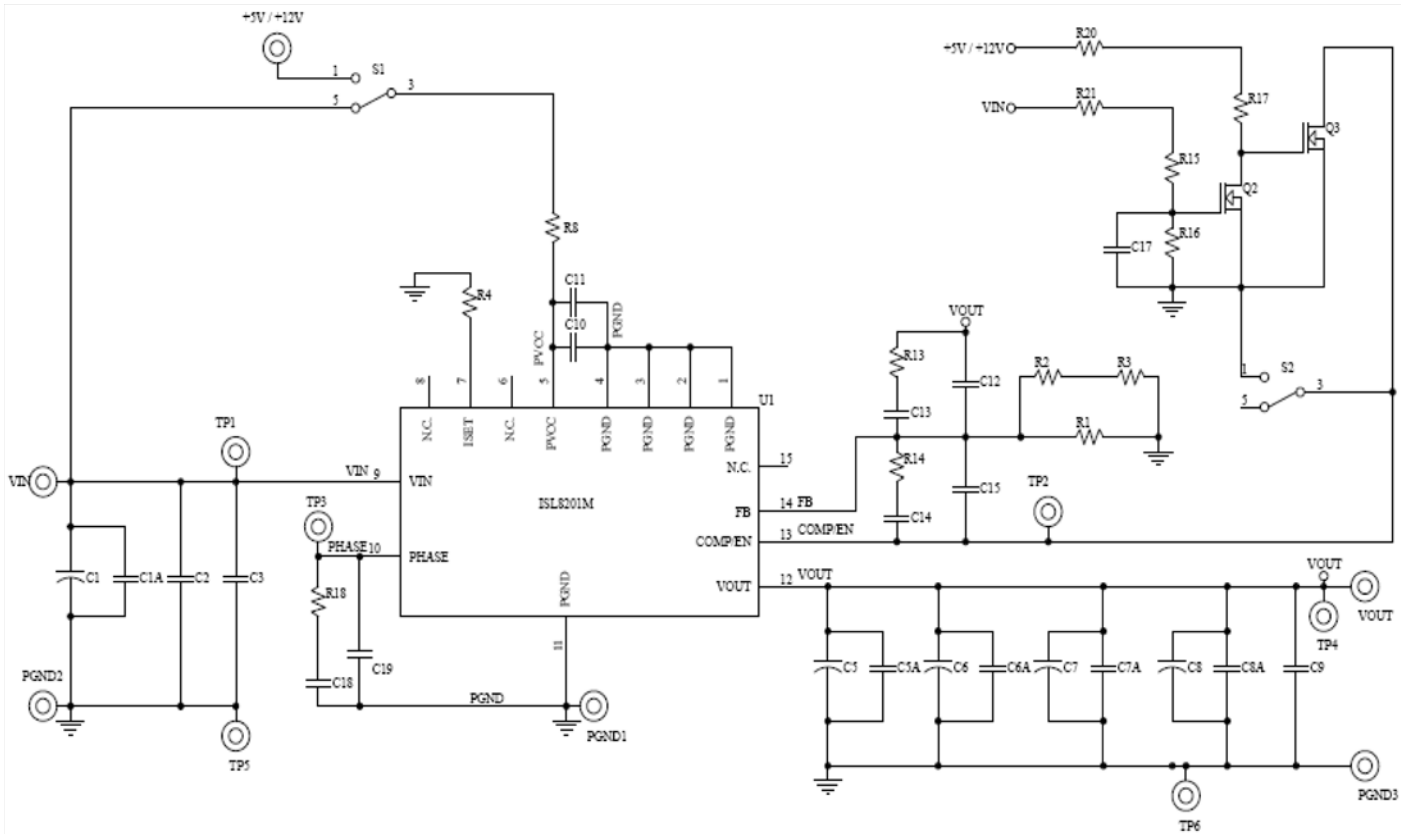


FIGURE 8. SCHEMATIC

NOTES:

1. R₁ is used to set the output voltage of ISL820xMEVAL1Z. Initial setting is 6.49kΩ for 1.5V output voltage.
2. R₂ and R₃, paralleling with R₁, are used to adjust the output voltage of ISL820xMEVAL1Z.
3. R₄ is used to set the overcurrent trip level of ISL820xMEVAL1Z. The ISL8201MEVAL1Z has integrated 3.57kΩ, ISL8206MEVAL1Z has integrated 4.12kΩ, and ISL8204MEVAL1Z has integrated 2.87kΩ
4. R₁₈, C₁₈ and C₁₉ are the snubber network, which can reduce the stress for internal semiconductor.
5. R₁₃, R₁₄, C₁₂, C₁₃, C₁₄ and C₁₅ are the external compensation network. The ISL820xMEVAL1Z has integrated the type 3 compensation network inside the module for typical applications.
6. R₁₅, R₁₆, R₁₇, R₂₀, R₂₁, C₁₇, Q₂ and Q₃ are the power-up sequence circuit. In case of PVCC bias, power-up first, then input voltage. This circuit has to be implemented.

TABLE 4. BILL OF MATERIALS

| SYMBOL | COMPONENTS | DESCRIPTION | SUPPLIER |
|--------|------------|----------------------------------|------------|
| R1 | Resistor | Chip Resistor 6.49k Ω | Generic |
| R2 | Resistor | Not installed | - |
| R3 | Resistor | Not installed | - |
| R4 | Resistor | Not installed | - |
| R8 | Resistor | Chip Resistor 10 Ω | Generic |
| R13 | Resistor | Not installed | - |
| R14 | Resistor | Not installed | - |
| R15 | Resistor | Not installed | - |
| R16 | Resistor | Not installed | - |
| R17 | Resistor | Not installed | - |
| R18 | Resistor | Not installed | - |
| R20 | Resistor | Not installed | - |
| R21 | Resistor | Not installed | - |
| C1 | Capacitor | AL Capacitor 220 μ F/35V | SANYO |
| C1A | Capacitor | Not installed | - |
| C2 | Capacitor | Ceramic Capacitor 10 μ F/25V | MURATA/TDK |
| C3 | Capacitor | Ceramic Capacitor 10 μ F/25V | MURATA/TDK |
| C5 | Capacitor | POS Capacitor 330 μ F/6.3V | SANYO |
| C5A | Capacitor | Not installed | - |
| C6 | Capacitor | Not installed | - |
| C6A | Capacitor | Ceramic Capacitor 22 μ F/10V | MURATA/TDK |
| C7 | Capacitor | Ceramic Capacitor 22 μ F/10V | MURATA/TDK |
| C7A | Capacitor | Not installed | MURATA/TDK |
| C8 | Capacitor | Ceramic Capacitor 22 μ F/10V | MURATA/TDK |
| C8A | Capacitor | Not installed | - |
| C9 | Capacitor | Not installed | - |
| C10 | Capacitor | Ceramic Capacitor 1 μ F/25V | YAGEO |
| C11 | Capacitor | Ceramic Capacitor 1 μ F/25V | YAGEO |
| C12 | Capacitor | Not installed | - |
| C13 | Capacitor | Not installed | - |
| C14 | Capacitor | Not installed | - |
| C15 | Capacitor | Not installed | - |
| C17 | Capacitor | Not installed | - |
| C18 | Capacitor | Not installed | - |
| C19 | Capacitor | Not installed | - |
| S1 | Switch | UT Switch | SH |
| S2 | Switch | UT Switch | SH |
| Q2 | MOSFET | Not installed | - |
| Q3 | MOSFET | Not installed | - |
| U1 | Module | ISL8201M, ISL8206M, or ISL8204M | Intersil |

Printed Circuit Board Layers

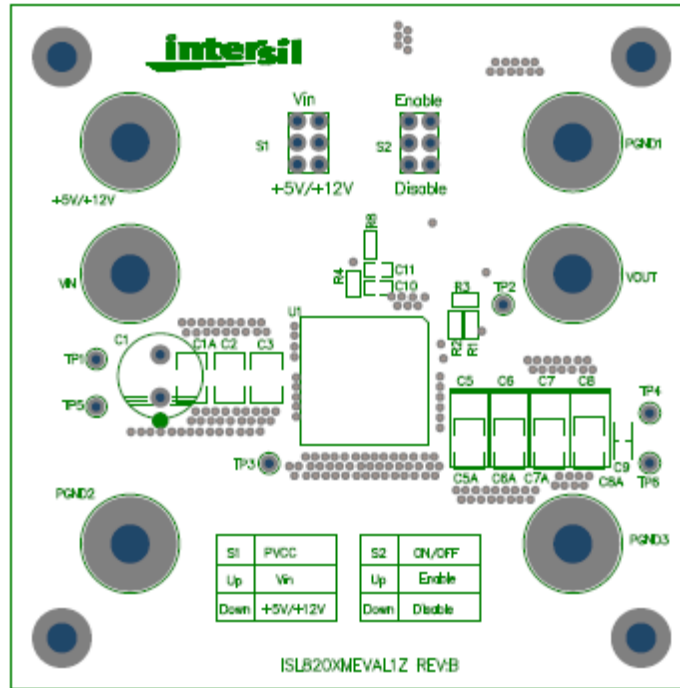


FIGURE 9. TOP-OVER LAYER (COMPONENT LOCATION)

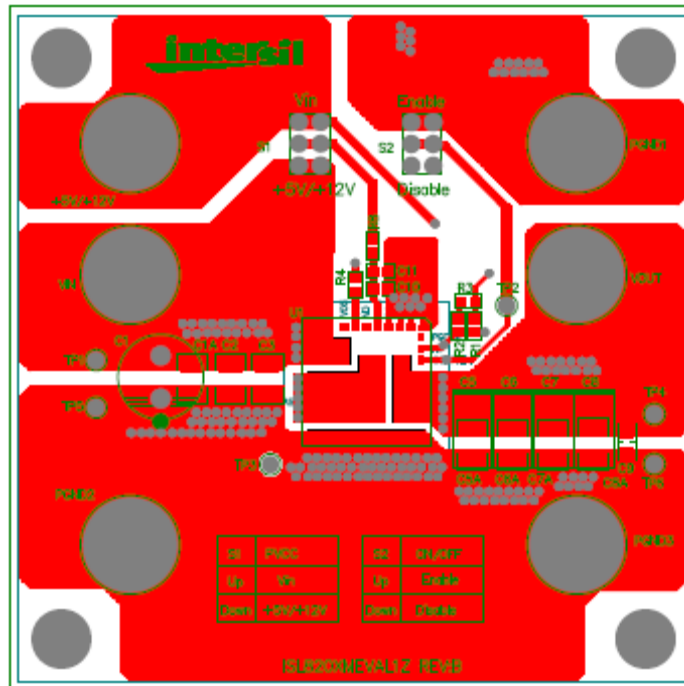


FIGURE 10. TOP LAYER (COMPONENT SIDE)

Printed Circuit Board Layers (Continued)

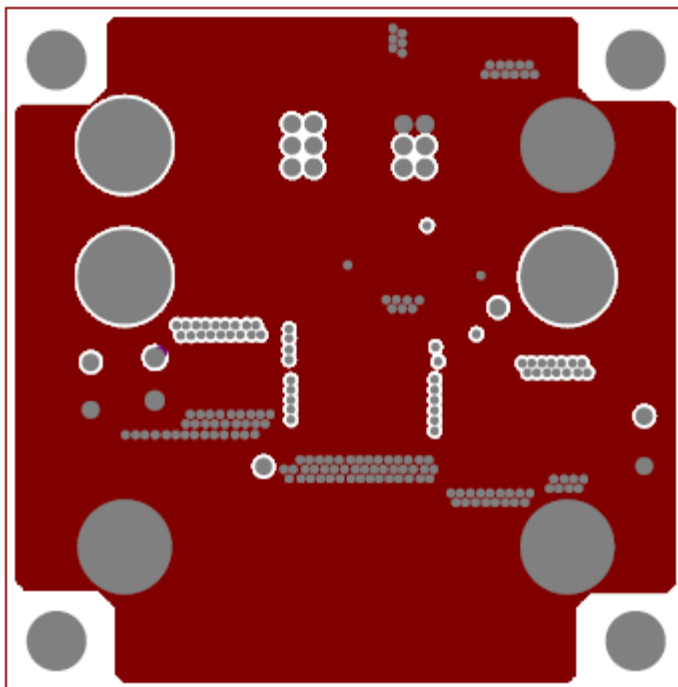


FIGURE 11. MIDDLE-1 LAYER

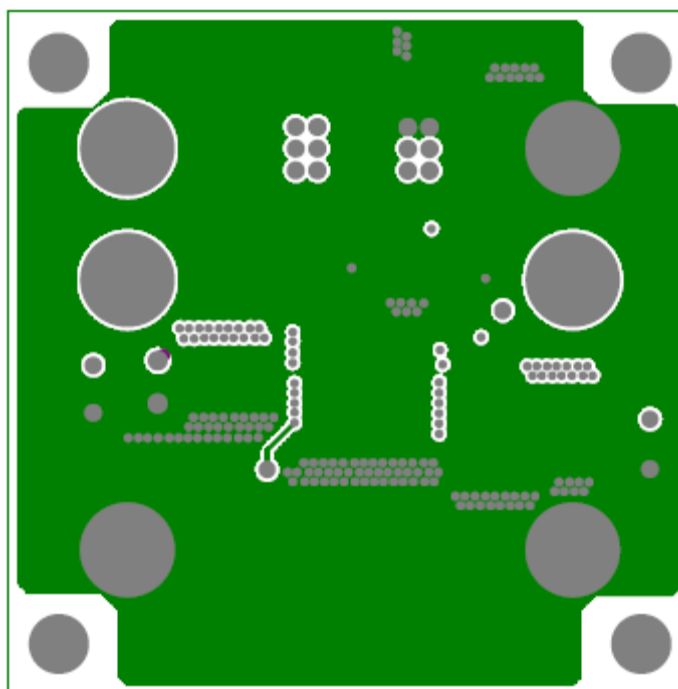


FIGURE 12. ISL820xMEVAL1Z, MIDDLE-2 LAYER

Printed Circuit Board Layers (Continued)

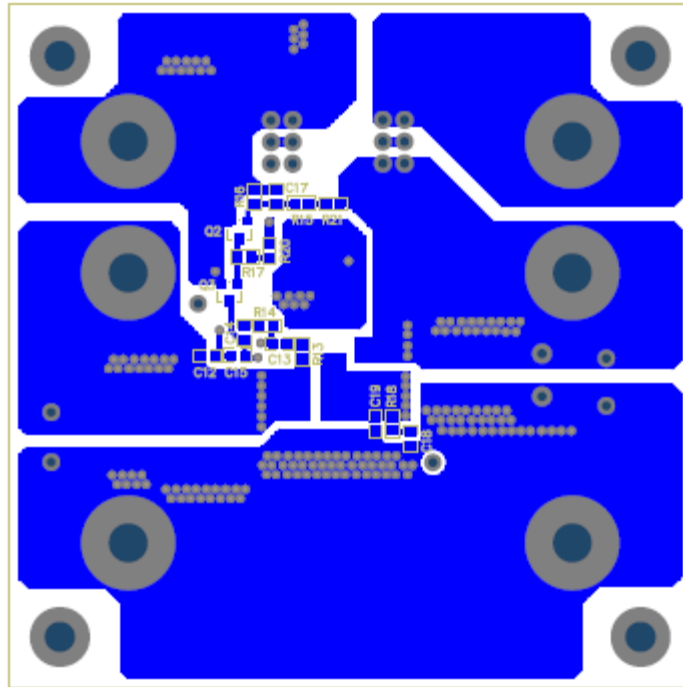


FIGURE 13. BOTTOM LAYER (COMPONENT SIDE MIRRORED)

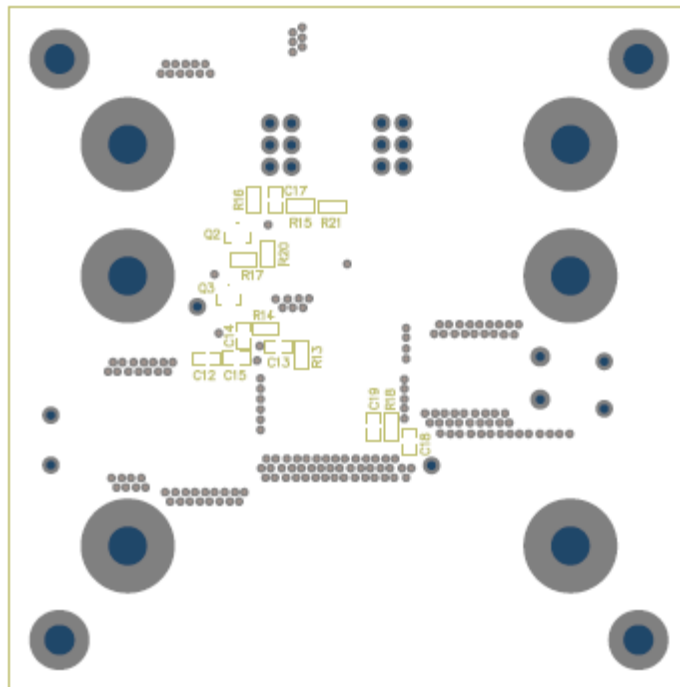


FIGURE 14. BOTTOM-OVER LAYER (COMPONENT LOCATION MIRRORED)

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