

FEATURES

Ultrawideband frequency range: 100 MHz to 44 GHz

Nonreflective 50 Ω design

Low insertion loss

1.8 dB up to 18 GHz

2.8 dB up to 40 GHz

3.2 dB up to 44 GHz

High isolation

50 dB up to 18 GHz

39 dB up to 40 GHz

35 dB up to 44 GHz

High input linearity

P0.1dB: 26 dBm typical

IP3: 47 dBm typical

High power handling

24 dBm through path

24 dBm terminated path

All off state control

Logic select control

No low frequency spurs

Settling time (0.1 dB final RF output): 30 ns

24-terminal, 3 mm \times 3 mm land grid array (LGA) package

Pin compatible with [ADRF5043](#), low frequency cutoff version

APPLICATIONS

Industrial scanners

Test instrumentation

Cellular infrastructure—millimeterwave (mmWave) 5G

Military radios, radars, electronic counter measures (ECMs)

Microwave radios and very small aperture terminals (VSATs)

GENERAL DESCRIPTION

The ADRF5042 is a nonreflective SP4T switch manufactured in the silicon on insulator (SOI) process.

The ADRF5042 operates from 100 MHz to 44 GHz with an insertion loss of lower than 3.2 dB and an isolation of higher than 35 dB. The device has a RF input power handling capability of 24 dBm for both through and terminated paths.

The ADRF5042 requires a dual-supply voltage of +3.3 V and -3.3 V. The device employs CMOS- and low voltage transistor to transistor logic (LVTTL)-compatible controls.

FUNCTIONAL BLOCK DIAGRAM

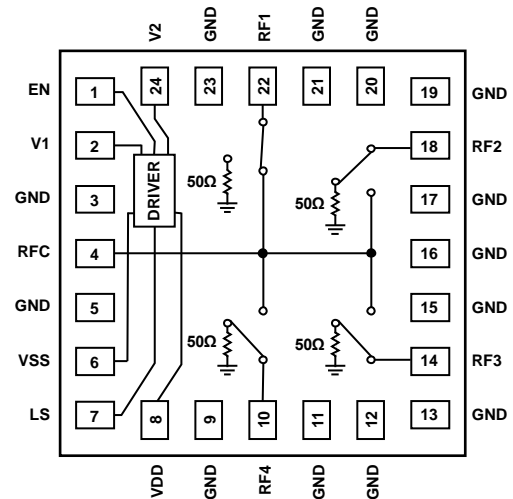


Figure 1.

23793-001

The ADRF5042 has enable and logic select controls to feature all off state and port mirroring, respectively.

The ADRF5042 is pin compatible with the [ADRF5043](#) low frequency cutoff version, which operates from 9 kHz to 44 GHz.

The ADRF5042 comes in a 24-terminal, 3 mm \times 3 mm, RoHS compliant, land grid array (LGA) package and can operate from -40°C to +105°C.

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REVISION HISTORY

7/2020—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = 3.3 V, negative supply voltage (V_{SS}) = -3.3 V, V1 pin voltage (V_1) = 0 V or 3.3 V, V2 pin voltage (V_2) = 0 V or 3.3 V, LS = 0 V or 3.3 V, EN = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4. V_{CTL} is the digital control inputs voltage.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------|----------------------|---|-----|------|--------|---------|
| FREQUENCY RANGE | f | | 100 | | 44,000 | MHz |
| INSERTION LOSS | | | | | | |
| Between RFC and RFx (On) | | 100 MHz to 18 GHz | | 1.8 | | dB |
| | | 18 GHz to 26 GHz | | 2.2 | | dB |
| | | 26 GHz to 35 GHz | | 2.5 | | dB |
| | | 35 GHz to 40 GHz | | 2.8 | | dB |
| | | 40 GHz to 44 GHz | | 3.2 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RFx (Off) | | 100 MHz to 18 GHz | | 50 | | dB |
| | | 18 GHz to 26 GHz | | 46 | | dB |
| | | 26 GHz to 35 GHz | | 41 | | dB |
| | | 35 GHz to 40 GHz | | 39 | | dB |
| | | 40 GHz to 44 GHz | | 35 | | dB |
| RETURN LOSS | | | | | | |
| RFC and RFx (On) | | 100 MHz to 18 GHz | | 16 | | dB |
| | | 18 GHz to 26 GHz | | 14 | | dB |
| | | 26 GHz to 35 GHz | | 13 | | dB |
| | | 35 GHz to 40 GHz | | 13 | | dB |
| | | 40 GHz to 44 GHz | | 14 | | dB |
| RFx (Off) | | 100 MHz to 18 GHz | | 24 | | dB |
| | | 18 GHz to 26 GHz | | 22 | | dB |
| | | 26 GHz to 35 GHz | | 15 | | dB |
| | | 35 GHz to 40 GHz | | 12 | | dB |
| | | 40 GHz to 44 GHz | | 10 | | dB |
| SWITCHING | | | | | | |
| Rise and Fall Time | t_{RISE}, t_{FALL} | 10% to 90% of RF output | | 3 | | ns |
| On and Off Time | t_{ON}, t_{OFF} | 50% V_{CTL} to 90% of RF output | | 14 | | ns |
| Settling Time | | | | | | |
| 0.1 dB | | 50% V_{CTL} to 0.1 dB of final RF output | | 30 | | ns |
| 0.05 dB | | 50% V_{CTL} to 0.05 dB of final RF output | | 36 | | ns |
| INPUT LINEARITY ¹ | | | | | | |
| 0.1 dB Power Compression | P0.1dB | f = 500 MHz to 40 GHz | | 26 | | dBm |
| 1 dB Power Compression | P1dB | f = 500 MHz to 40 GHz | | 27 | | dBm |
| Third-Order Intercept | IP3 | Two-tone input power = 15 dBm each tone, f = 500 MHz to 40 GHz, Δf = 1 MHz | | 47 | | dBm |
| Second-Order Intercept | IP2 | Two-tone input power = 15 dBm each tone, f = 10 GHz, Δf = 1 MHz | | 120 | | dBm |
| VIDEO FEEDTHROUGH ² | | | | 60 | | mV p-p |
| SUPPLY CURRENT | | VDD, VSS pins | | | | |
| Positive Supply Current | I_{DD} | | | 370 | | μA |
| Negative Supply Current | I_{SS} | | | -100 | | μA |
| DIGITAL CONTROL INPUTS | | V1, V2, EN, LS pins | | | | |
| Voltage | | | | | | |
| Low | V_{INL} | | 0 | | 0.8 | V |
| High | V_{INH} | | 1.2 | | 3.3 | V |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------------|------------|---|-------|-----|----------|-------------|
| Current | | | | | | |
| Low | I_{INL} | | | 3 | | μA |
| High | I_{INH} | | | 6 | | μA |
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | V_{DD} | | 3.15 | | 3.45 | V |
| Negative | V_{SS} | | -3.45 | | -3.15 | V |
| Digital Control Inputs Voltage | V_{CTL} | | 0 | | V_{DD} | V |
| RFx Input Power ³ | P_{IN} | $f = 500 \text{ MHz to } 44 \text{ GHz, } T_{CASE} = 85^{\circ}C^4$ | | | | |
| Through Path | | Average | | | 24 | dBm |
| | | Peak | | | 24 | dBm |
| Terminated Path | | Average | | | 24 | dBm |
| | | Peak | | | 24 | dBm |
| Hot Switching | | Average | | | 24 | dBm |
| | | Peak | | | 24 | dBm |
| Case Temperature | T_{CASE} | | -40 | | +105 | $^{\circ}C$ |

¹ For input linearity performance over frequency, see Figure 18 to Figure 21.

² Video feedthrough is the spurious dc transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

³ For power derating over frequency, see Figure 2.

⁴ For 105 $^{\circ}C$ operation, the power handling degrades from the $T_{CASE} = 85^{\circ}C$ specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

| Parameter | Rating |
|--|---|
| Supply Voltage | |
| Positive | -0.3 V to +3.6 V |
| Negative | -3.6 V to +0.3 V |
| Digital Control Inputs ¹ | -0.3 V to V _{DD} + 0.3 V or 3.3 mA, whichever occurs first |
| RFx Input Power (f ² = 500 MHz to 44 GHz, T _{CASE} = 85°C ³) | |
| Through Path | |
| Average | 26 dBm |
| Peak | 26 dBm |
| Terminated Path | |
| Average | 25 dBm |
| Peak | 25 dBm |
| Hot Switching | |
| Average | 25 dBm |
| Peak | 25 dBm |
| Temperature | |
| Junction, T _J | 135°C |
| Storage Range | -65°C to +150°C |
| Reflow | 260°C |

¹ Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

² For power derating over frequency, see Figure 2.

³ For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

| Package Type | θ _{JC} ¹ | Unit |
|-----------------|------------------------------|------|
| CC-24-12 | | |
| Through Path | 468 | °C/W |
| Terminated Path | 200 | °C/W |

¹ θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5042

Table 4. ADRF5042, 24-Terminal LGA

| ESD Model | Withstand Threshold (V) |
|---------------------------------|-------------------------|
| HBM | |
| RFx Pins | 375 |
| Supply and Digital Control Pins | 2000 |

POWER DERATING CURVES

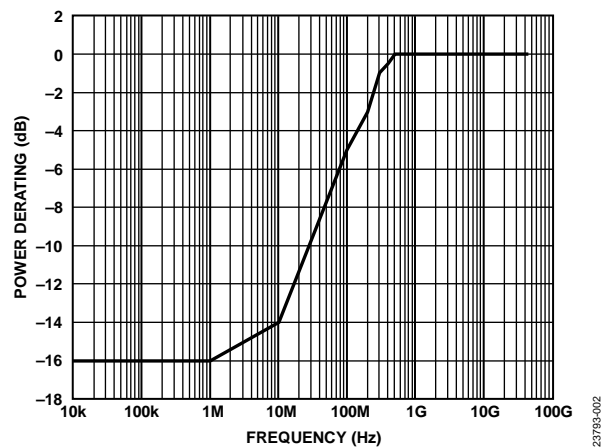


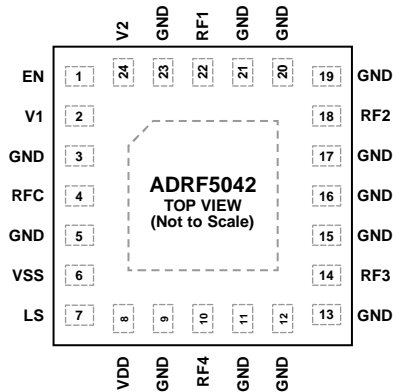
Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD MUST BE CONNECTED TO THE RF AND DC GROUND.

23793-003

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|----------|---|
| 1 | EN | Enable Input. See Table 6 for the truth table. See Figure 5 for the interface schematic. |
| 2 | V1 | Control Input 1. See Table 6 for the truth table. See Figure 5 for the interface schematic. |
| 3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23 | GND | Ground. The GND pins must be connected to the RF and dc ground of the PCB. |
| 4 | RFC | RF Common Port. RFC is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic. |
| 6 | VSS | Negative Supply Voltage. |
| 7 | LS | Logic Select Input. See Table 6 for the truth table. See Figure 5 for the interface schematic. |
| 8 | VDD | Positive Supply Voltage. |
| 10 | RF4 | RF Throw Port 4. RF4 is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic. |
| 14 | RF3 | RF Throw Port 3. RF3 is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic. |
| 18 | RF2 | RF Throw Port 2. RF2 is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic. |
| 22 | RF1 | RF Throw Port 1. RF1 is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. |
| 24 | V2 | Control Input 2. See Table 6 for the truth table. See Figure 5 for the interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground. |

INTERFACE SCHEMATICS

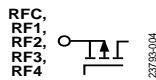


Figure 4. RFC and RF1 to RF4 Pin Interface Schematic

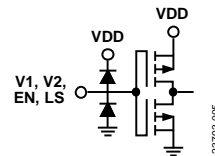


Figure 5. V1, V2, EN, and LS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTL} = 0\text{ V}$ or 3.3 V , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted. Measured on the evaluation board.

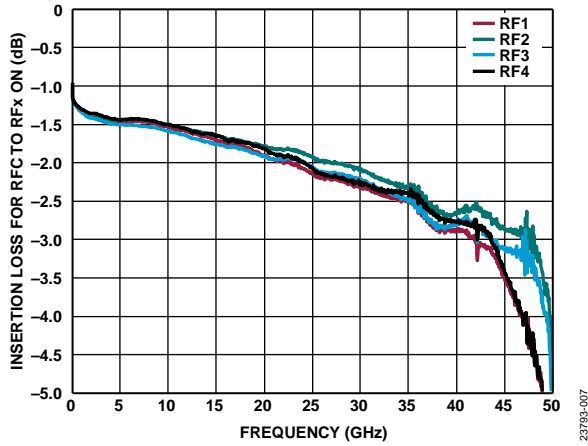


Figure 6. Insertion Loss for RFC to RFX On vs. Frequency

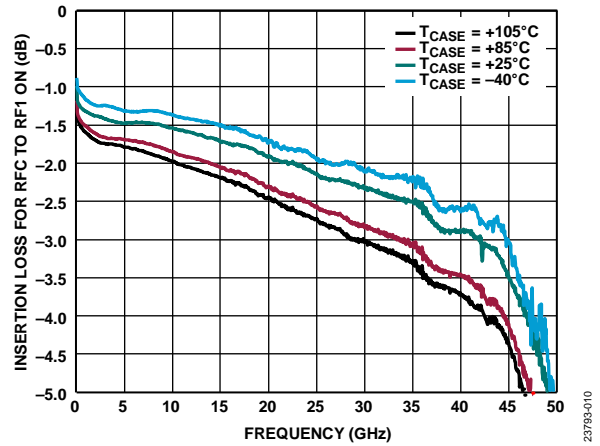


Figure 9. Insertion Loss for RFC to RF1 On vs. Frequency over Various Temperatures

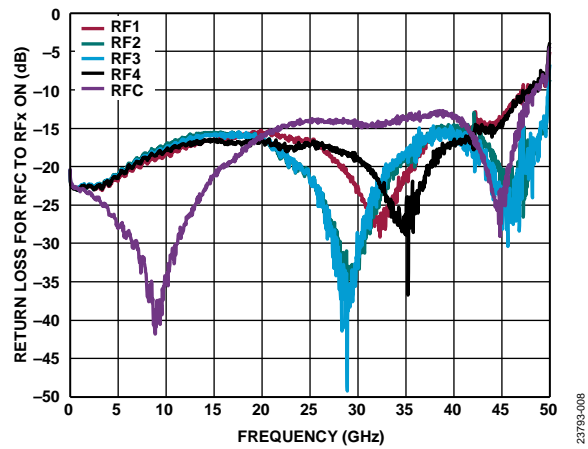


Figure 7. Return Loss for RFC and RFX On vs. Frequency

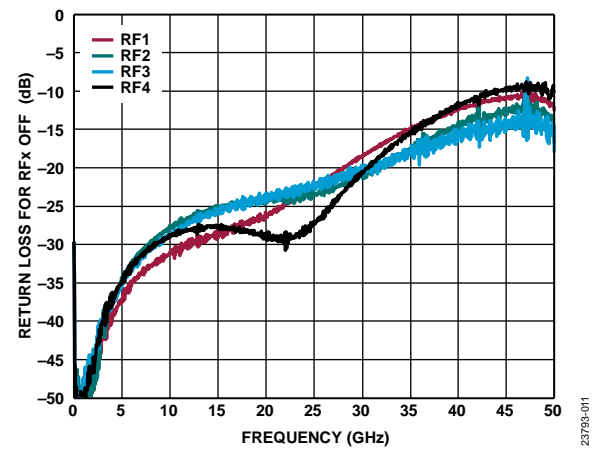


Figure 10. Return Loss for RFX Off vs. Frequency

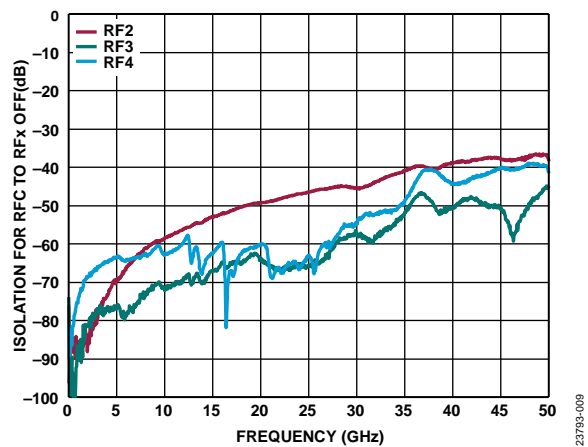


Figure 8. Isolation for RFC to RFX Off vs. Frequency, RFC to RF1 Path On

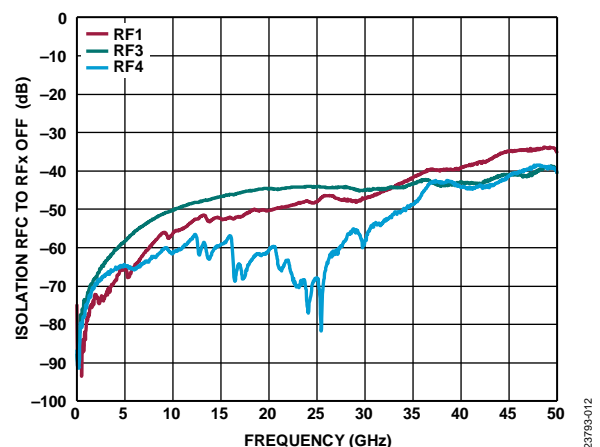


Figure 11. Isolation for RFC to RFX Off vs. Frequency, RFC to RF2 Path On

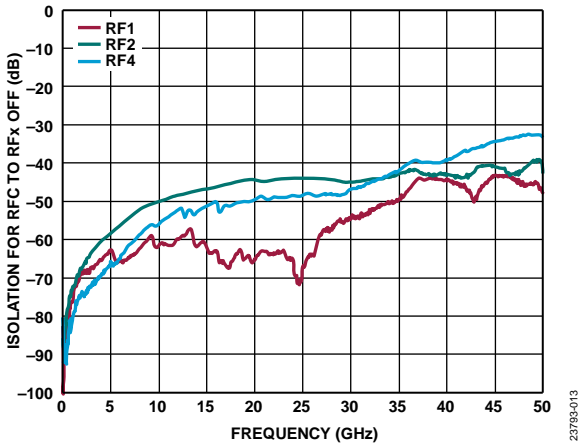


Figure 12. Isolation for RFC to RFx Off vs. Frequency, RFC to RF3 Path On

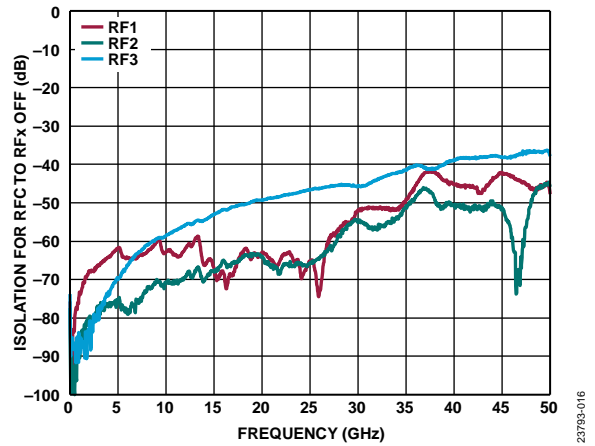


Figure 15. Isolation for RFC to RFx Off vs. Frequency, RFC to RF4 Path On

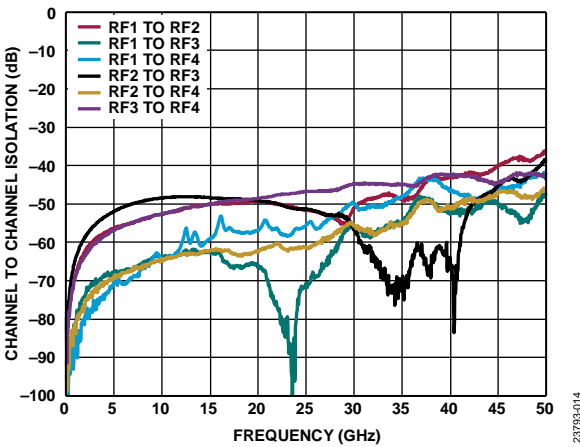


Figure 13. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path On

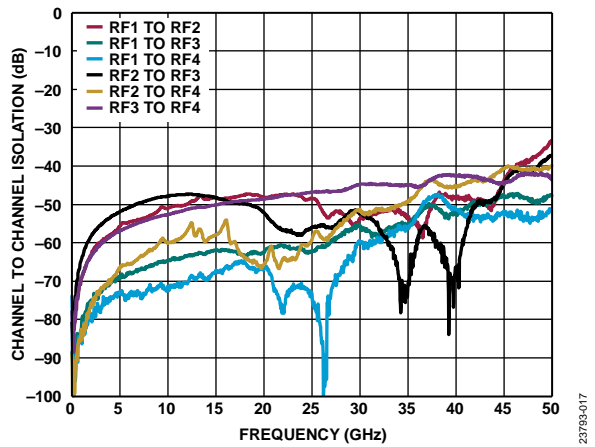


Figure 16. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path On

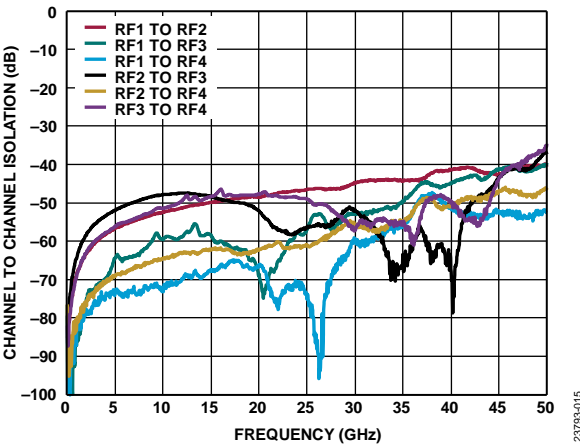


Figure 14. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path On

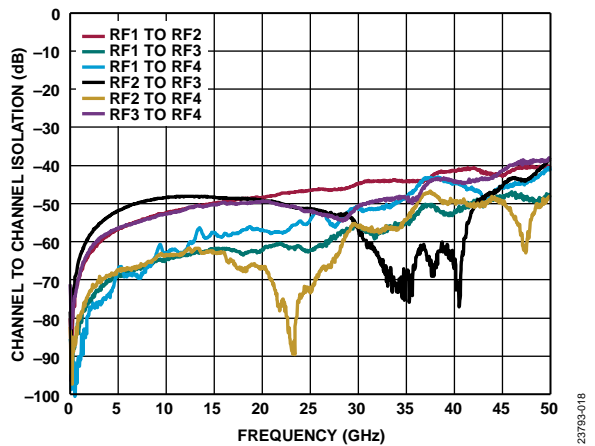


Figure 17. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path On

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTL} = 0\text{ V}$ or 3.3 V , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted. Measured on the evaluation board.

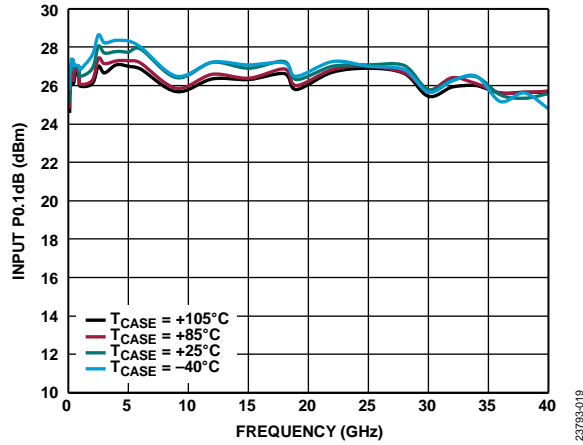


Figure 18. Input P0.1dB vs. Frequency over Various Temperatures

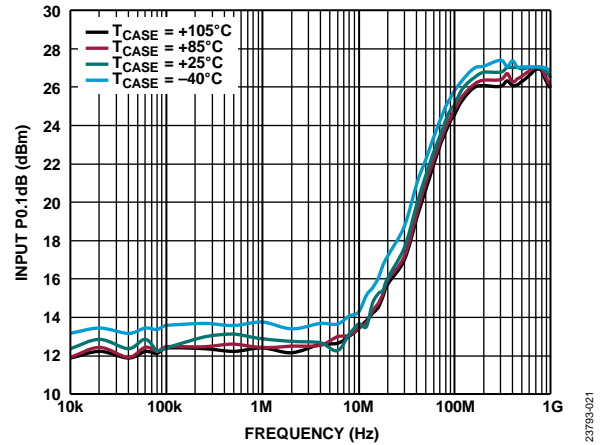


Figure 20. Input P0.1dB vs. Frequency, Low Frequency Detail over Various Temperatures

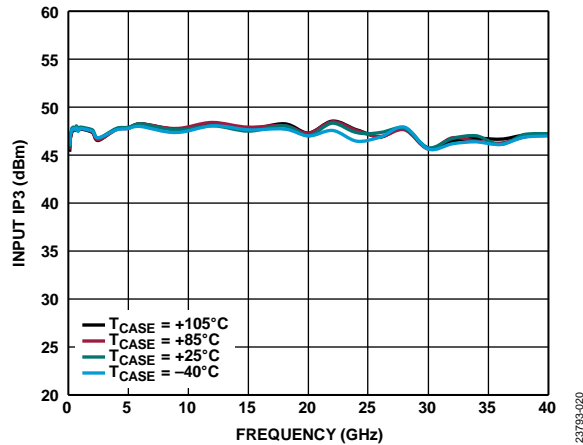


Figure 19. Input IP3 vs. Frequency over Various Temperatures

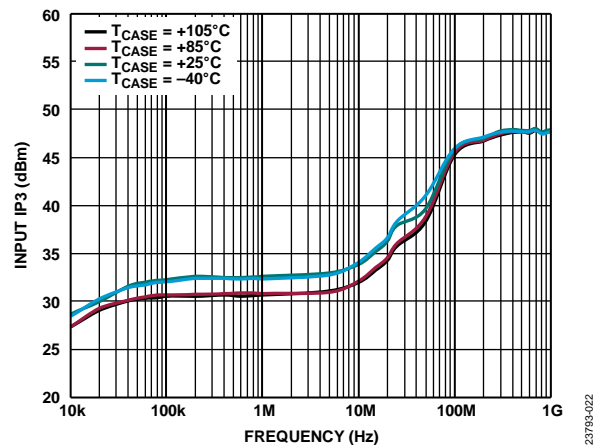


Figure 21. Input IP3 vs. Frequency, Low Frequency Detail over Various Temperatures

THEORY OF OPERATION

The ADRF5042 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

All of the RF ports (RFC, RF1 to RF4) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5042 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS-/LVTTTL-compatible control interface. The driver features four digital control input pins (EN, LS, V1, and V2) that control the state of the RFx paths (see Table 6).

The logic select input (LS) allows the user to define the control input logic sequence for the RF path selections. The logic level applied to the V1 and V2 pins determines which RFx port is in the insertion loss state while the other three paths are in the isolation state.

When the EN pin is logic high, all four RFx paths are in isolation state regardless of the logic state of LS, V1, V2. RFx ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports that are terminated to internal 50 Ω resistors.

The ideal power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.
3. Apply a control voltage to the digital control inputs (EN, LS, V1, and V2). Applying a control voltage to the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. Use a series 1 kΩ resistor to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, controller output is in high impedance state) after VDD is powered up, it is recommended to use a pull-up or pull-down resistor.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

| Digital Control Inputs | | | | RFx Paths | | | |
|------------------------|-------------|-------------|-------------|---------------------|---------------------|---------------------|---------------------|
| EN | LS | V1 | V2 | RFC to RF1 | RFC to RF2 | RFC to RF3 | RFC to RF4 |
| Low | Low | Low | Low | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| Low | Low | High | Low | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| Low | Low | Low | High | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| Low | Low | High | High | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |
| Low | High | Low | Low | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |
| Low | High | High | Low | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| Low | High | Low | High | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| Low | High | High | High | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| High | Low or high | Low or high | Low or high | Isolation (off) | Isolation (off) | Isolation (off) | Isolation (off) |

APPLICATION INFORMATION

EVALUATION BOARD

All measurements in this data sheet are measured on the [ADRF5042-EVALZ](#) evaluation board. Figure 24 shows the simplified application circuit for [ADRF5042-EVALZ](#) evaluation board. See the [ADRF5042-EVALZ](#) user guide for more information on using the evaluation board.

The design of the [ADRF5042-EVALZ](#) board serves as a layout recommendation. The Gerber files of the [ADRF5042-EVALZ](#) evaluation board are available at www.analog.com/EVAL-ADRF5042.

The [ADRF5042-EVALZ](#) is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. Figure 22 shows the cross sectional view of the evaluation board stackup.

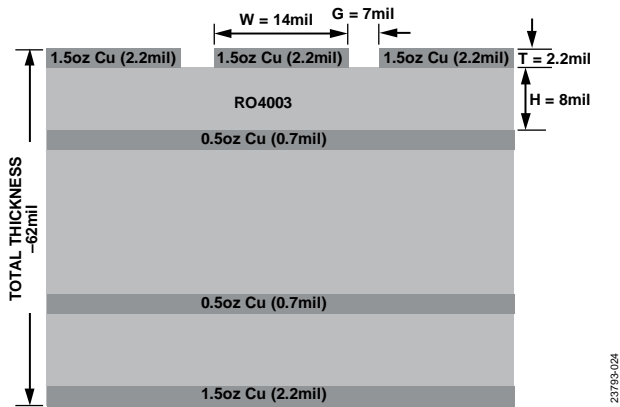


Figure 22. Evaluation Board Stackup, Cross Sectional View

All RF traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with a trace width of 14 mil and a ground clearance of 7 mil to have a characteristic impedance of 50 Ω. The RF transmission lines are tapered at the RFC or RFx pin transition, as shown in Figure 23. For optimal RF and thermal grounding, arrange as many plated through vias as possible around the transmission lines and under the exposed pad of the package.

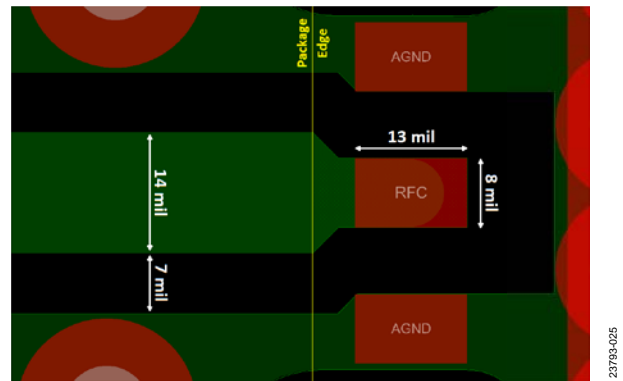


Figure 23. RF Transmission Lines

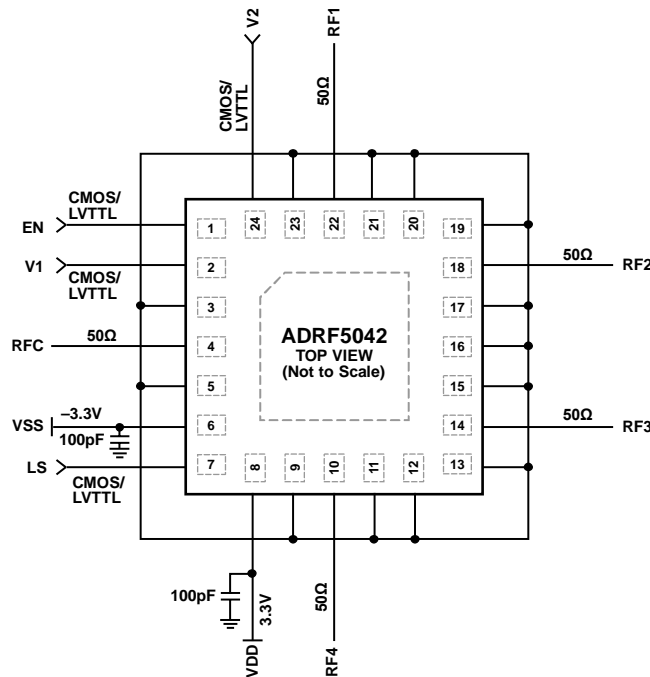


Figure 24. Application Circuit

OUTLINE DIMENSIONS

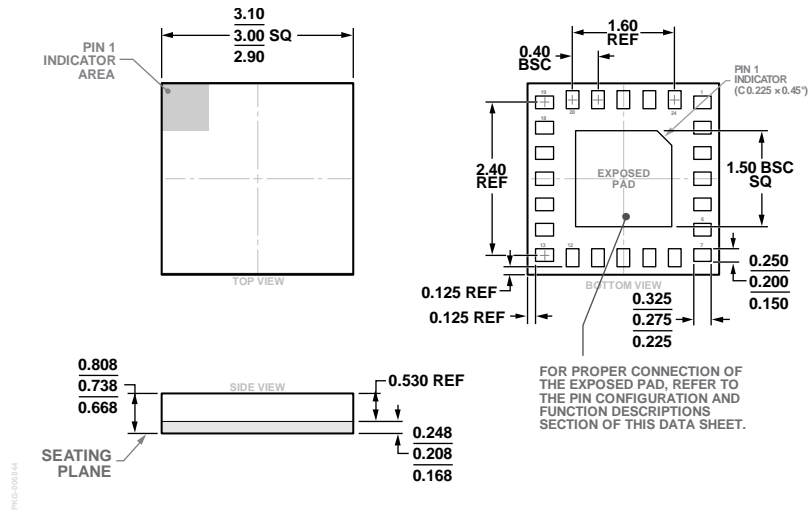


Figure 25. 24-Terminal Land Grid Array [LGA]
 3 mm x 3 mm Body and 0.738 mm Package Height
 (CC-24-12)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Marking Code |
|--------------------|-------------------|-----------------------------------|----------------|--------------|
| ADRF5042BCCZN | -40°C to +105°C | 24-Terminal Land Grid Array [LGA] | CC-24-12 | 042 |
| ADRF5042BCCZN-R7 | -40°C to +105°C | 24-Terminal Land Grid Array [LGA] | CC-24-12 | 042 |
| ADRF5042-EVALZ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.